(1) Explain universal Synchronous Bus
(2) write about Dired memory axis?
(3) what is an interface circuit & explain serial port & parallel po

DIRECT MEMORY ACCESS

- *Direct Memory Access refers to that data transfer, when large blocks of data are to be transferred at high speeds between I/O devices and main memory, without involving the processor.*
- *In order to perform DMA transfer, an additional interface circuitry is required known as DMA controller.*
- To initiate the transfer, the processor sends the starting address of the block, the number of words in the block, the direction of transfer – to or from memory.
- For each word transferred, it provides the memory address. The DMA controller must increment the memory address for successive words and keep track of number of transfers.
- On receiving this information, the DMA controller performs the requested transfer. When the entire block has been transferred, the controller informs the processor by raising the interrupt signal.
- While DMA transfer is taking place, the program that requested the transfer cannot continue and the processor can be used to execute another program.
- After the DMA transfer is completed, the processor can return to the program that requested the transfer.

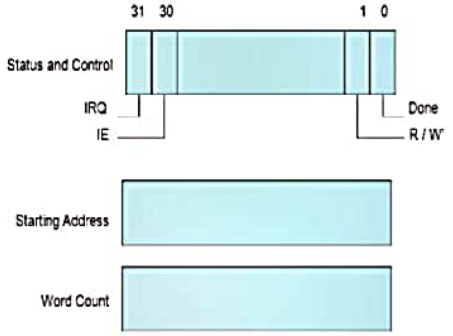
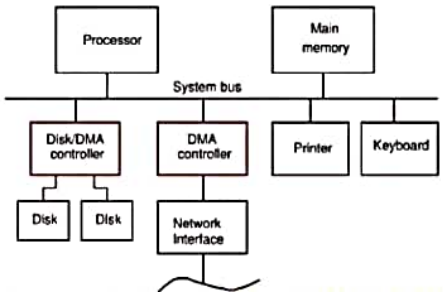


Fig: Registers in a DMA interface

- *Two registers are used for storing the starting address and the word count. The third register contains status and control flags.*
- *The bit determines the direction of the transfer. When this bit is set to 1 by a program instruction, the controller performs a read operation i.e. it transfers data from memory to I/O device. Otherwise, it performs write operation.*
- *When the controller has completed transferring a block of data and is ready to receive another command, it sets the Done flag to 1.*
- *Bit 30 is the interrupt-enable-flag (IE). When this flag is set to 1, it causes the controller to raise an interrupt after it has completed transferring a block of data.*
- *The controller sets the IRQ bit to 1 when it has requested an interrupt.*



- *DMA controller connects a high-speed network to the computer bus.*
- *Disk controller, which controls two disks also has DMA capability and provides two DMA channels.*
- *It can perform two independent DMA operations, as if each disk had its own DMA controller.*
- *The registers needed to store the memory address, word count, status and so on are duplicated.*
- *To start a DMA transfer of a block of data from main memory to one of the disk, a program writes the address and word count information into the register of the corresponding channel of the disk controller.*
- *When the DMA transfer is completed, it records in the status and control register of DMA by setting the Done bit. At the same time, if the IE bit is set, the controller sends an interrupt request to the processor and sets the IRQ bit.*

- *The I/O devices initiate the DMA transfer by sending a DMA request signal to the Processor when it is ready to perform a transfer. There are three methods by which DMA transfer is initiated and operated:*
  - *Burst mode or Block transfer DMA*
  - *Cycle steal and Single byte transfer DMA*
  - *Transparent or Hidden DMA*
- *The DMA controller access to the main memory to transfer block of data without interruption. This is known as block or burst mode.*
- *In cycle steal mode, only one byte of data is transferred at a time. After transferring one byte, it disables 'HOLD' signal and enters in to slave mode. Since the processor originates most memory access cycles, the DMA controller can be said to be "steal" memory cycles from the processor.*
- *A conflict may arise if both the processor and a DMA controller (or) two DMA controllers try to use the bus at the same time to access the main memory. To resolve these conflicts, an arbitration procedure is implemented on the bus to coordinate the activities of all devices requesting memory transfers.*

Advantages of DMA:

- *Data in large volumes can be moved by utilizing system bus.*
- *DMA module transfers the entire block to and from the memory and informs the processor.*

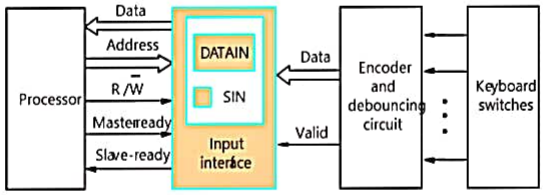
Disadvantages of DMA:

- *For transferring the data, DMA module needs the total control of the system bus.*
- *Processor must wait when it urgently needs the system bus.*
- *Processor cannot indulge in other task while waiting for the bus.*

INTERFACE CIRCUITS

- *I/O interface consists of the circuitry required to connect an I/O device to a computer bus.*
- *Side of the interface which connects to the computer has bus signals for:*
  - *Address,*
  - *Data*
  - *Control*
- *Side of the interface which connects to the I/O device has:*
  - *Data path and associated controls to transfer data between the interface and the I/O device is called as a "port".*
- *Ports can be classified into two:*
  - *Parallel port*
  - *Serial port.*
- *Parallel port transfers data in the form of a number of bits, normally 8 or 16 to or from the device.*
- *Serial port transfers and receives data one bit at a time.*
- *Processor communicates with the bus in the same way, whether it is a parallel port or a serial port.*
  - *Conversion from the parallel to serial and vice versa takes place inside the interface circuit.*

Parallel Port



- *Keyboard is connected to a processor using a parallel port.*
- *Processor is 32-bits and uses memory-mapped I/O and the asynchronous bus protocol.*
- *On the processor side of the interface we have:*
  - *Data lines.*
  - *Address lines*
  - *Control or R/W line*
  - *Master-ready signal and*
  - *Slave-ready signal*
- *On the keyboard side of the interface:*
  - *Encoder circuit which generates a code for the key pressed.*
  - *Debouncing circuit which eliminates the effect of a key bounce (a single key stroke may appear as multiple events to a processor).*
  - *Data lines contain the code for the key.*
  - *Valid line changes from 0 to 1 when the key is pressed. This causes the code to be loaded into DATAIN and SIN to be set to 1.*

Serial Port

- *Serial port is used to connect the processor to I/O devices that require transmission of data one bit at a time.*
- *Serial port communicates in a bit-serial fashion on the device side and bit parallel fashion on the bus side.*
  - *Transformation between the parallel and serial formats is achieved with shift registers that have parallel access capability.*

- *Serial interfaces require fewer wires, and hence serial transmission is convenient for connecting devices that are physically distant from the computer.*
- *Speed of transmission of the data over a serial interface is known as the "bit rate".*
  - *Bit rate depends on the nature of the devices connected.*
- *In order to accommodate devices with a range of speeds, a serial interface must be able to use a range of clock speeds.*
- *Several standard serial interfaces have been developed:*
  - *Universal Asynchronous Receiver Transmitter (UART) for low-speed serial devices.*
  - *RS-232-C for connection to communication links.*

SYNCHRONOUS BUS

- *In a synchronous bus, all devices derive timing information from a common clock line. Equally spaced pulses on this line define equal time intervals.*
- *The address and data lines are shown as high and low at the same time. This is a common line indicating that some lines are high and some low depending on the particular address or data pattern being transmitted.*
- *The crossing points indicate the times at which these pattern changes.*
- *Let us consider the sequence of events during an input (read) operation.*
- *At time to, the matter places the device address on address lines and sends an appropriate command on control lines.*
- *The command will indicate an input operation and specify the length of the operand to be read, if necessary.*
- *It allows all devices to decode the address and control signals so that the addressed devices (slave) can respond at time t1.*
- *The addressed slave places the requested input data on the data lines at time t1.*
- *At the end of the clock cycle, at time t2 the master strobes the data on the data lines into its input buffer. "Strobe" means to capture the data at a given instant and store them in to a buffer.*
- *A similar procedure is followed for an output operation. The master places the output data on the data lines when it transmits the address and command information. At time t2, the addressed device strobes the data lines and loads the data into its data buffer.*