## READING AND RESEARCH ASSIGNMENT

A) [15] [Max 1 page] Read the paper labeled R3 and comment on it. Make sure to specifically address these points: What is Virtualization? What are some of the main implementation issues and challenges? What techniques can be used to address them? What role do you think VMs will play in the future?

B) [15] Search the web for the following four memory technologies, DDR4 SDRAM, GDDR5 SDRAM, MRAM, and ZRAM and present your findings such as their speed, size, access time, and availability and cost in a table.

## EXERCISES

1) [45] Consider a 2-way set associative cache that has 32 blocks and 16 bytes per block. Assume a 32 bit address.

   a) How many bits are needed to store the tag in the cache?

   b) For the above cache, assume LRU is used for cache replacement. Given the following address access sequence (data are shown in hexadecimal). For each memory access, identify its block offset, set index, and tag, decide whether it is a cache hit or cache miss. If it is a cache miss, also mark whether it is compulsory miss, conflict miss or capacity

| Address | Tag | Index | Offset | Hit/Miss? | Type of miss |
|---|---|---|---|---|---|
| 0x100 | | | | | |
| 0x104 | | | | | |
| 0x108 | | | | | |
| 0x200 | | | | | |
| 0x204 | | | | | |
| 0x410 | | | | | |
| 0x100 | | | | | |
| 0x108 | | | | | |
| 0x40C | | | | | |
| 0x408 | | | | | |
| 0x300 | | | | | |
| 0x284 | | | | | |
| 0x280 | | | | | |
| 0x304 | | | | | |

   c) Calculate the miss rate for this memory access sequence.

   d) Assume that the cache is initially empty. After the above memory access sequence, how many cache blocks are occupied?

   e) If the same cache is direct mapped, how wide is the tag field?

2) [10] Consider a 64-byte direct mapped cache with 8 byte blocks. Virtual addresses are 16 bits. Each page is 128 bytes. The cache is physically tagged. The processor has 1 KB of physical memory. Assume pages 0-4 of the physical memory have been occupied.

   a) How large would a single-level page table be, given that each page requires 4 protection bits, and entries must be an integral number of bytes.

   b) Assume the cache is initialized empty, the CPU needs to access memory with the following virtual address sequence: $004_8$, $010_8$, $200_8$, $204_8$, $208_8$, $004_8$, $010_8$, and $200_8$. For each memory access, decide whether it is a page hit or page fault, and whether it is a cache hit or cache miss

3) [15] The memory architecture of a computer is summarized as Virtual Address: 54 bits; Page Size: 16 K-bytes; PTE (Page Table Entry) Size as 4 bytes.

   a) How large would a single-level page table be, given that each page requires 4 protection bits, and entries must be an integral number of bytes.

   b) Assume that there are 8 bits reserved for the operating system functions (protection, replacement, valid, modified, and Hit/Miss - All overhead bits) other than required by the hardware translation algorithm. Derive the largest physical memory size (in bytes) allowed by this PTE format. Make sure you consider all the fields required by the translation algorithm.

   c) Assuming one application exists in the system and the maximum physical memory is devoted to the process, how much physical space (in bytes) is there for the application's data and code?