RESEARCH AND READING ASSIGNMENT

A) [10] [Max 1 page] Read and briefly summarize the two papers labeled with **R1**. Comment on which of the cited features listed for IBM 360 are still used in today's instruction sets? List some of the arguments made for and against RISC and explain if these arguments still hold true today.

B) [10] [Max 1 page] Visit the Intel on-line microprocessor museum[1], and determine the rate of increase in transistor counts and clock frequencies in the 70's, 80's, 90's, 00's, and this decade. Also, create a plot of the number of transistors versus technology feature size using an MS Excel spreadsheet.

EXERCISES

1) [10] Table below shows relevant chip statistics that influence the cost of several processors. Explore the effect of different possible design decisions for the Processor A and answer the below questions.

Chip	Die size	Estimated defect rate (per cm^2)	Manufacturing size (nm)	Transistors (millions)
Processor A	400	0.30	130	276
Processor B	380	0.75	90	279
Processor C	199	0.75	90	233

a) What is the die yield for Processor A? (Assume wafer yield is 100%, process-complexity factor is 5 for 130 nm technology)

b) What might be the reasons that Processor A has a lower defect rate than the others?

2 [10] One challenge for architects is that the design created today will require several years of implementation, verification, and testing before appearing on the market. This means that the architect must project what the technology will be like several years in advance. Sometimes, this is difficult to do. According to the trend in device scaling observed by Moore's law, the number of transistors on a chip in 2025 should be how many times the number in 2015?

3 [10] When parallelizing an application, the ideal speedup is speeding up by the number of processors. This is limited by two things: percentage of the application that

[1] http://www.intel.com/content/www/us/en/history/historic-timeline.html
http://www.intel.com/content/www/us/en/history/museum-transistors-to-transformations-brochure.html
http://www.intel.com/content/www/us/en/company-overview/intel-museum.html

can be parallelized and the cost of communication. Amdahl's law takes into account the former but not the latter. What is the speedup with N processors if 50% of the application is parallelizable, ignoring the cost of communication? What will be the speedup for a system with 1000 processors?

4 [10] One critical factor in powering a server farm is cooling. If heat is not removed from the computer efficiently, the fans will blow hot air back onto the computer, not cold air. Observe the effect of different design decisions on the necessary cooling, and thus the price, of a system. A cooling door for a rack costs $4,000 and dissipates 14 KW (into the room; additional cost is required to get it out of the room). How many servers with a Processor P2, 1 GB 240-pin DRAM, and a single 7,200 rpm hard drive can you cool with one cooling door? Use the table below for your power calculations.

Component Type	Product	Performance	Power
Processor	P1	1.2 GHz	72-79 W peak
	P2	2 GHz	45 – 60W
DRAM	MEM1	184-pin	3.7 W
	MEM2	240-pin	2.3 W
Hard disk drive	HDD1	5400 rpm	7.9 W read/seek, 2.9 W idle
	HDD2	7200 rpm	7.9 W read/seek, 4.0 W idle

CASE STUDIES

A) You have the following characteristics, as shown in the table below, on your company's processor for a certain benchmark, which runs at 400 MHz:

Instruction Type	Frequency (%)	Cycles
Arithmetic and logical	30	1
Load and Store	20	2
Branches	40	3
Floating Point (FP)	10	5

You are asked to consider a cheaper, lower-performance version of this processor, by removing some of the FP hardware to reduce the die size. The wafer has a diameter of 10 cm, costs $1,000, and has a defect rate of 2/(cm^2). This wafer has a 75% yield. The current chip has a die size of 12 mm^2. The new chip becomes 10 mm^2, and FP instructions will now take 13 cycles to execute.

a) [10] What are the old and new CPI (Cycles Per Instructions) and MIPS (Million Instructions Per Second) ratings running this benchmark?

b) [10] What are the old and new die yields? What are the old and new costs per (working) processor? Please comment on the overall effect of the proposed

hardware change on the cost and the performance of the processor. (Assumee process-complexity factor is 4)

c) [10] What would be the theoretical limit of the best possible overall speedup that we could ever get by only improving the FP unit, and what would be the CPI and MIPS ratings of this new processor?

B) [10] Your company produces a mobile device. To extend the battery life in the newer version of the device, you are asked to elaborate on the idea to simply reduce the processor clock speed by 20%, and make no other changes. Stating your assumptions, describe whether this is a good idea or a bad idea, and why. Make sure to address both power and energy.