Mess Simulator: New Capabilities in the Latest Release

Pouya Esmaili-Dokht[1,2], Ashkan Asgharzadeh[2], Petar Radojkovic[2], and Eduard Ayguadé[1,2]

[1]*Unversitat Politecnica de Catalunya* [2]*Barcelona Supercomputing Center*

1. Introduction

The importance of main memory in the overall system's design drives significant effort for memory system **benchmarking**, **simulation** and memory-related **application profiling**. With Mess framework, we argue that these three aspects can and should be based on a **unified view of memory system performance**. Mess framework is comprised of Mess benchmark, simulator and application profiling tool. It is developed in collaboration between Barcelona Supercomputing Center (BSC) and Micron Technology. Mess framework study has won **best paper runner-up award** at MICRO 2024 for it's "Novel methodology for memory system simulation" [1]. BSC is using Mess as standard memory system benchmarking, simulation, and memory related application profiling for high-end HPC platforms. Mess enables benchmarking and accurate simulation of standard and emerging memory technologies and is adopted by various publications from academia (e.g. for detailed benchmarking of CXL memory expander device [2]) and industry (e.g. for accurate main memory simulation of DDR5-5600 technology [3]).

In this talk, we focus on the **Mess simulator**. The Mess simulator bridges the gap between memory system performance characterization and memory system simulation. It accurately simulates emerging memory systems as soon as their bandwidth–latency curves are available from hardware characterization. This removes the current gap between a technology release and support for its detailed hardware simulation. The Mess simulator already supports **DDR4**, **DDR5**, **Optane**, **HBM2**, and **HBM2E** memory systems [4]. The Mess integration is easy, based on the standard interfaces between the CPU and external memory simulators. Initial release of **Mess simulator** is already integrated in the **ZSim**, **gem5**, and **OpenPiton Metro-MPI**. The Mess closely matches the actual memory systems performance. The simulation error for memory-intensive benchmarks is between 0.4% and 6%, which is significantly better than any other memory models we tested. Mess is also fast. When integrated with ZSim, Mess shows 13–15× simulation speedup w.r.t. the Ramulator and DRAMsim3. Also, Mess is the first simulator that models CXL memory expanders, enabling further research on these novel memory devices. The CXL simulation is based on the bandwidth–latency curves obtained from the memory manufacturer's SystemC hardware model.

We have already released open source repositories of integrating Mess simulator with well-known CPU simulators: OpenPiton [5], gem5 [6], ZSim [7]. During Mess tutorial at MICRO 2025, we are planning to provide a straightforward guideline for integrating Mess simulator with any arbitrary CPU simulator. This will be part of the new release materials.

2. New supported features

The new release includes:

- **Standalone Mess simulator**: A standalone version that enables developers to easily integrate Mess with any CPU simulator. Multiple ongoing research projects are already using this version of Mess integrated with their own CPU simulators.
- **Mess integration with ChampSim**: An open-source integration of Mess with the ChampSim simulator is available [8]. This integration was developed by Agustín Navarro under the supervision of Alberto Ros from the University of Murcia.
- **Mess integration with MUSA**: The Mess simulator is integrated with multi-level simulation approach (MUSA) [9] for performance estimations of large-scale next-generation HPC machines.
- **Support for new technologies**: Mess now supports two new memory technologies, **LPDDR5X** and **MRDIMMs**, which are not currently supported by other major memory simulators.
- **Actual CXL curves**: Mess originally supported CXL memory expanders using bandwidth–latency curves generated from Micron Technology's detailed RTL simulations. We now release the model supporting performance simulation of Micron CZ120 CXL device.

References

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