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Design and Implementation of 64-point Fast Fourier Transform Chip for OFDM-based 802.11a WLAN in 45nm Lithography

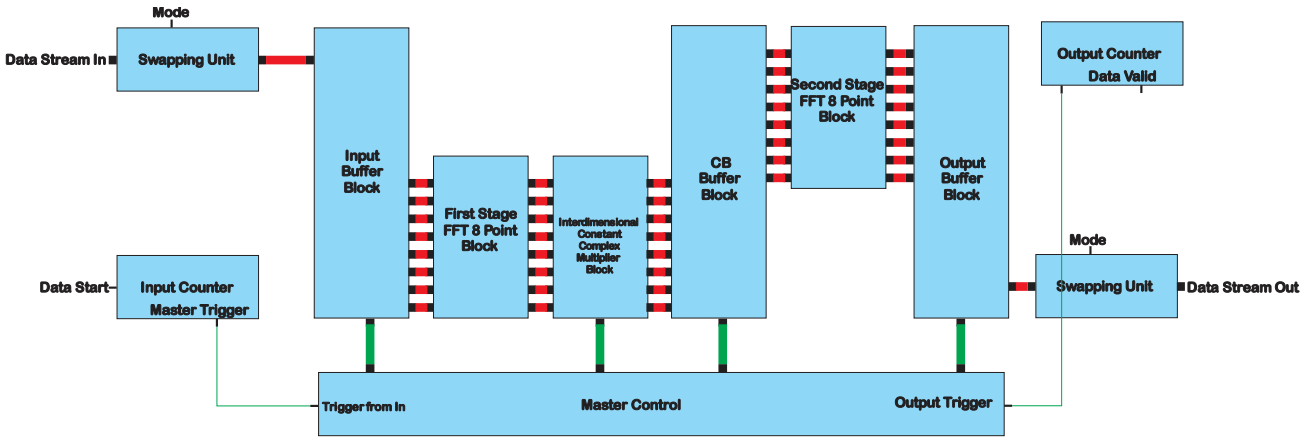
For our project, we would like to design and implement a 64-point Fast Fourier Transform (FFT) chip which will be specifically used for Wireless LAN 802.11a application. We are interested to adopt the design described by Koushik Maharatna et. al. on this following paper.

> K. Maharatna, E. Grass, and U. Jagdhold, "A 64-Point Fourier Transform Chip for High-Speed Wireless LAN Application Using OFDM," IEEE J. Solid-St. Circ., Vol. 39, No. 3, Mar. 2004, pp. 484-493.

The paper describes how to build a 64-point FFT architecture using two 8-point FFT blocks that can fullfil the requirement for Wireless LAN 802.11a where each FFT/IFFT operation must be completed under 4µs. In this paper, the chip is manufactured using 0.25µm BiCMOS technology and has area of 6.8mm² and average dynamic power consumption of 41mW at 20MHz operating frequency at 1.8V supply voltage. It would be interesting to see how the performance, power, and area of this design when it is implemented using 45nm CMOS technology as we will do in our project.

High-Level Diagram

Based on the paper, the high-level diagram for the chip is shown below. There are three arrays of DFFs, multiple Carry-Lookahead Adder, two counters, and one finite-state machine as master control.



- Input Buffer Block is used to convert serial stream of data into parallel stream of data consists of 8 streams.
- First-stage FFT 8-point Block is used to calculate 8-point Fast Fourier Transform.
- Interdimensional Multiplier block is used to multiply the output data from First-stage FFT 8-point block with interdimensional twiddle factor constant.
- CB Buffer Block is used to rearrange the data and acts as buffer.
- Second-stage FFT 8-point Block is used to calculate 8-point Fast Fourier Transform.
- Output Buffer Block is used to convert parallel data stream into serial data stream.
- Master Control Block is a finite state machine that controls the operation of whole circuit. There are two counters that help Master Control Block: Input Counter Block and Output Counter Block.

Data Format

We will use a signed 16-bit fixed-point data format in the form of Q4.12. Each data has two parts: real part and imaginary part. Therefore, each data will have 32-bit length shown below.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S	Integer			Fraction												S	Integer			Fraction											
Real Part																Imaginary Part															

With this data format, our data dynamic range and precision can be described below.

- Largest possible value : 7.9997558593750 (0b0111111111111111)
- Smallest possible value : -8.0000000000000 (0b1000000000000000)
- Precision : 0,0002441406250 (0b0000000000000001)

Mathematical Review

Discrete Fourier Transform (DFT) $A(r)$ from a series of complex data $B(k)$ consists of N data where $r, k \in \{0, 1, \dots, N-1\}$ can be written as follows.

$$A(r) = \sum_{k=0}^{N-1} B(k) W_N^{rk}$$
$$W_N = e^{-2\pi j/N}$$

For $N = MT$, $r = s + Tt$, and $k = l + Mm$ where $s, l \in \{0,1 \dots 7\}$ and $m, t \in \{0,1, \dots, T-1\}$, the equation above can be rewritten as follows.

$$A(s + Tt) = \sum_{l=0}^{M-1} W_M^{lt} \left[W_{MT}^{sl} \sum_{m=0}^{T-1} B(l + Mm) W_T^{sm} \right]$$

It means that an N-point FFT can be realized using an M-point FFT and T-point FFT in a such way that $N = MT$. Therefore, our 64-point FFT can be decomposed into two units of 8-point FFT as follows.

$$A(s + 8t) = \sum_{l=0}^{7} \left[W_{64}^{sl} \sum_{m=0}^{7} B(l + 8m) W_8^{sm} \right] W_8^{lt}$$

Project Goal and Plans

Our project consists of several steps that need to be taken care of.

- Understanding the FFT design presented in the reference paper. (Deliverable: C code / MATLAB code)
- Create RTL of the design using Verilog or VHDL. (Deliverable: Verilog / VHDL code)
- Perform functional and timing simulation on the RTL. (Deliverable: Simulation Waveform)
- RTL to Gate-Level Netlist Export. (Deliverable: Verilog Gate-Level Netlist)
- Automatic Place and Route. (Deliverable: GDS II ?)
- Post-PNR Verification and Signoff.