Sistemas Digitais - Digital Systems

Licenciatura em Engenharia Informática- Pós-Laboral

Degree in Computer Engineering

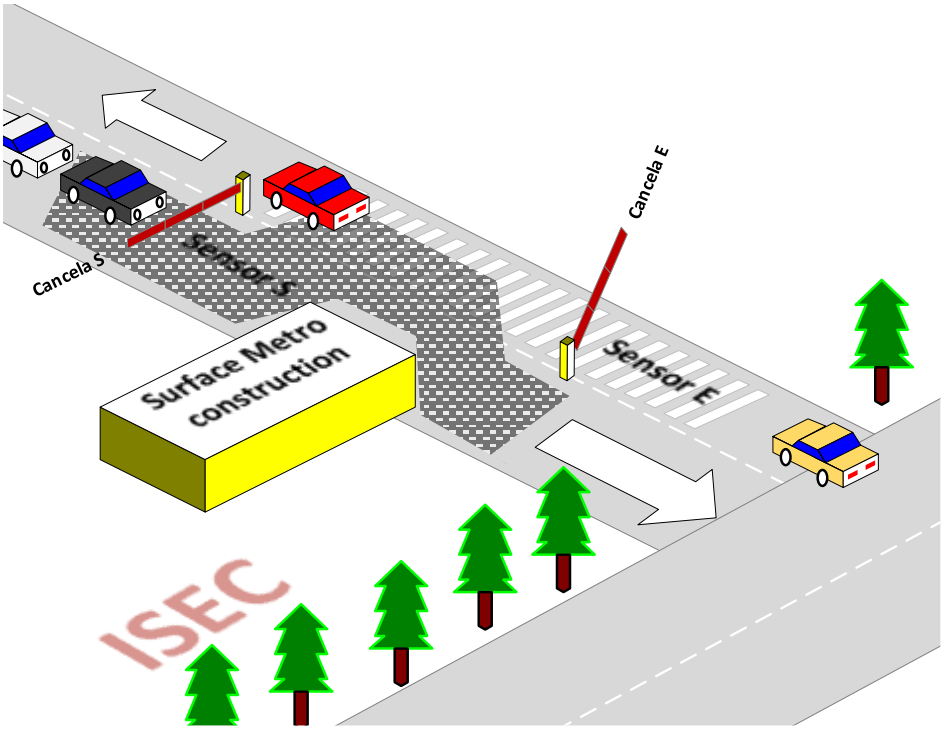
Exam – Normal Season

Total Exam Duration: 2h January 19, 2024

1) It is intended to install a new digital vehicle entry and exit control system at ISEC due to the Surface Metro construction works that will obstruct the vehicle exit lane according to the figure.

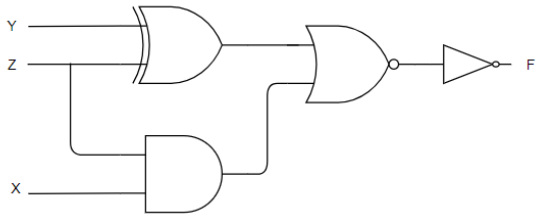
This constraint prevents the simultaneous entry and exit of vehicles, meaning circulation must be carried out alternately. The digital system to be designed must control **Cancela_E** and **Cancela_S**, which regulate the progress of vehicles entering and leaving the **ISEC** campus, respectively.

The system has two sensors (**Sensor_E** and **Sensor_S**). **Sensor_E** marked with white stripes, detects the presence of vehicles in the entry lane and **Sensor_S** marked by a darker pattern, detects the presence of vehicles in the exit lane. These two lanes are partially overlapping in the traffic constraint area near the works.



When there are no vehicles above any of the sensors, both gates (Cancela) must be closed. When one of the sensors detects the presence of vehicles, the system must immediately open the respective gate (Cancela), which must remain open as long as vehicles are traveling in that lane while the other gate (Cancela) remains closed. When there are no more vehicles in that lane, this gate (Cancela) must close and only then can the other gate (Cancela) be opened, if vehicles are already waiting to pass. Note that the sensors detect vehicles just before they reach the gates. Develop the project of the described system, presenting: a) The state diagram; b) The state transition table; c) Redundant states; d) The codification of states; e) The transition table with coded states; f) The logic diagram of the circuit.

2) Given the function F expressed in the following logic diagram



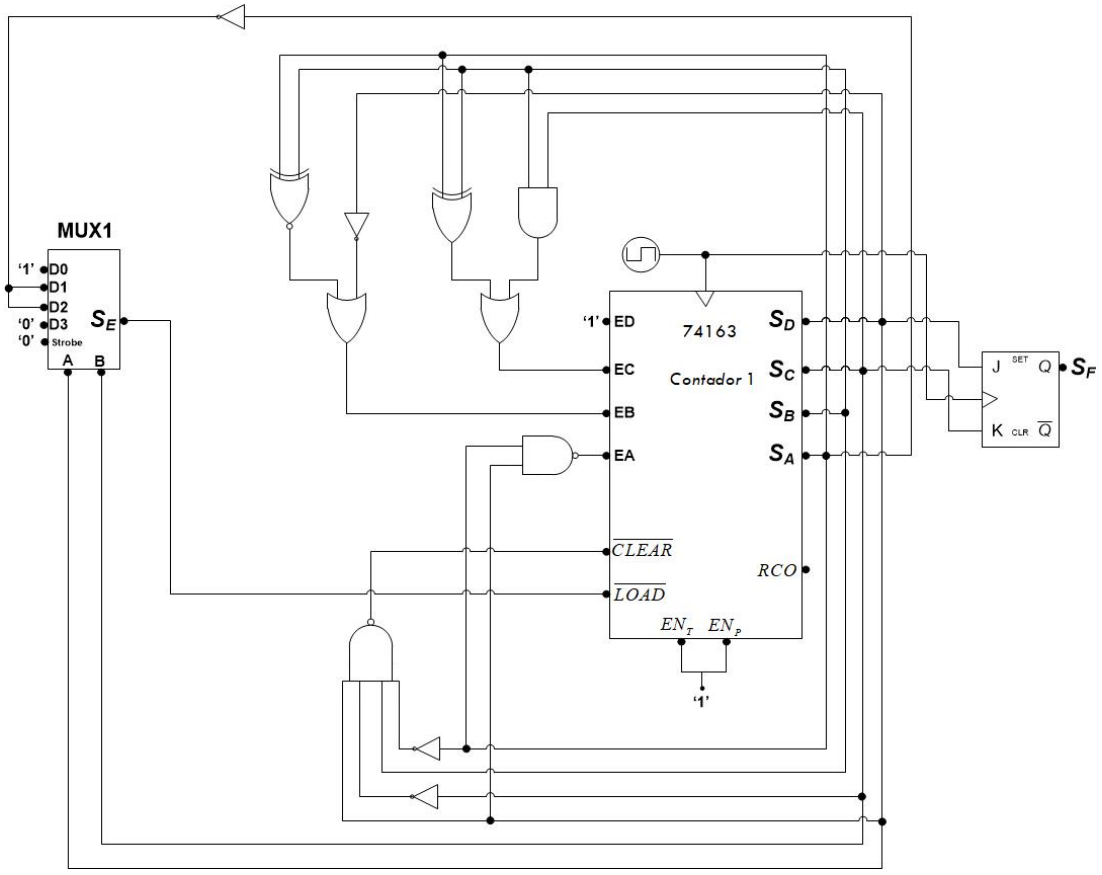
a) Implement it with two 4:1 Multiplexer and one 2:1 Multiplexer

b) Implement it with a 4:1 Multiplexer.

3) Simplify the following logical expression using the theorems and postulates of Boolean algebra. Indicate the theorems/postulates used in each simplification step.

$$X.\bar{Y} + \overline{X.\bar{W}.Z + \bar{\bar{Y}}.Z + \bar{X}.W.Z}$$

4) Consider the circuit in the following figure:



Assuming that counter 1 is in state (**$S_DS_CS_BS_A$=0000**) and the FFs is in state **01**. Fill in the table below with the data relating to the 12 subsequent clock periods. Justify the proposed solution.

Clock	FF_2	FF_1	Contador				Hexadecimal
	S_F	S_E	S_D	S_C	S_B	S_A	$S_DS_CS_BS_A$
Início	0	1	0	0	0	0	0
↓							
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Note: Consider that MUX selection input A represents the most significant input

Full name: _____ Student number:_____