



Jabil Digital DFx Content Extract  
Design For Manufacturability

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# Design For Manufacturability

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DFM > Data and Deliverables > CAD

Entry ID: 1004

## Fiducials in CAD Solderpaste Layers

### Guideline

CID: 2

Content Owner: Jabil

Content Type: Requirement

For optical alignment of the **PCB** in the **stencil** printer, the **fiducials** must be present in the **solderpaste** layer of the **CAD** data for use by the stencil manufacturer. Fiducials in the stencil will be "half etched" to prevent a solderpaste deposit on the board.

When fiducials are not present in the solderpaste layer, they may be copied from the copper layer and added to the solderpaste layers.

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## Optical Requirements in Design Drawings

### Guideline

CID: 2

Content Owner: Jabil

Content Type: Requirement

#### Design drawing requirements:

Ensure design drawings specify the location and min / max length of [optical fibers](#) while minimizing the total number of loops needed.

Document the sequence for how the loops are stacked into the clips, the most critical components go into the clips last.

Design and document the fiber layout so that the fiber lays flat, eliminating the possibility of twist.

Specify color coded fiber for applications with high fiber counts.

- These requirements may affect the cost, manufacturability and functionality of the product.

Document the fiber loop assembly jig.

- Preparing the loops in a jig prior to assembly improves manufacturability and lowers the cost of the product.

If LiNb based optical components are present in the product, specify 650nm light cannot be used for troubleshooting.

- 650nm light can destroy LiNb based components.

Ensure the max temperature the product can be subjected to is specified.

- If max temperature is exceeded, the [splice protectors](#) and fiber coating can be damaged.

Ensure the type of optical fiber coating and length tolerance is specified.

- If the type of fiber coating and length tolerance is not specified, this can result in issues at fiber routing.

**Note:** Work with the workcell, optical component suppliers, and optical connector vendors to see which [splicing](#) strategy may work best for the proposed production volumes.

### Related Entries

DFA Guideline [1726 Assembling > Assembling Requirements > Optical Fiber Routing](#)

DFM Rule [1107 Component Selection > General > Optical Fiber Connectors](#)

DFM Guideline [1108 Component Selection > General > Optical Fiber Pigtails](#)

DFA Rule [1728 Assembling > Assembling Requirements > Optical Fiber Bend Radius](#)

DFA Guideline [1729 Assembling > Assembling Requirements > Optical Fiber Clips](#)

DFM Guideline [1345 Component Selection > General > Self-Adhesive Pads and Optical Fibers](#)

DFM Guideline [1636 PCB Design > General > Optical Design Considerations](#)

DFM > Data and Deliverables > General

Entry ID: 1730

## Fab Drawing

### Guideline

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 3 | Content Owner: Jabil | Content Type: Information |
|--------|----------------------|---------------------------|

#### Introduction:

The fab drawing shows various elements of the design, tolerances, details specific to the fab that will be needed by the [PCB vendor](#).

|        |                      |                           |
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| CID: 2 | Content Owner: Jabil | Content Type: Requirement |
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Specify [soldermask](#) alignment tolerance in the fab drawing.

- Soldermask misalignment can make it more difficult to achieve proper solderpaste print release on fine pitch apertures.

Specify if soldermask repair is allowed and where in the fab drawing.

- PCB vendors may try to repair soldermask defects with manual touch up, however, this can lead to solderpaste printing and soldering defects.

Specify a matte green soldermask in the fab drawing.

- Gloss surface finishes may increase solder balls during wave soldering and some colors with a gloss finish cause issues for automated optical inspection. Certain colors such as red are troublesome for AOI, black can impact X-ray, etc. and colors other than green can cost more.

If required, specify the controlled impedance tolerance in the fab drawing.

- The PCB fabricator may not meet the tolerance required if it is not specified.

Please specify the cleanliness requirements in the fab drawing.

- If there are no specific cleanliness requirements specified, the PCBs may have debris, oils, etc. on arrival.

For rigid flex products: specify in the fab drawing if assemblies need to be baked prior to production.

- Flex cover layers may absorb moisture and delaminate when exposed to soldering temperatures.

Specify in the fab drawing that maximum PCB warpage = 0.2000mm per 25.0000mm

- Excess warpage can be an issue when solderpaste printing large BGA and fine pitch devices.

Specify the PCB material Tg (glass transition) and Td (degradation temperature) in the fab drawing.

- A higher than necessary Tg (glass transition) or Td (degradation temperature) can increase PCB cost. The recommended Tg is 135C for tin lead and 175C for lead-free.

For lead-free PCBs: indicate in the fab drawing if RoHS compliance will be in copper, silkscreen or a label.

- RoHS labeling indicates the design intent and the RoHS directive.

Specify the minimum thickness for the selected surface finish in the fab drawing.

- Insufficient surface finish thickness could result in process issues etc.

Specify the [HASL](#) surface finish thickness in the fab drawing.

- HASL surface thickness (typically 2.54 to 25.4um) can have an impact on manufacturing / solderability.

Specify the lot code and date code in the fab drawing.

- Tracking issues back to manufacturing is important for understanding field failures.

Ensure a minimum of two non-plated tooling holes are included in the hole chart.

- Tooling holes are used for precise PCB alignment purposes in many manufacturing processes. A minimum of two non-plated through holes on the PCB are necessary; provide three for large boards or as a way to prevent loading the board onto equipment backwards.

Ensure the tooling hole diameter tolerance is specified in the hole chart. See [Entry 1075](#).

- Tooling hole diameter tolerances are critical. If the diameter of the tooling hole is any less than the negative tolerance, the PCB is at risk of getting stuck on the mating tooling pin. When the hole diameter is greater than the positive tolerance, the precise alignment with mating tooling pins required for manufacturing processes could be compromised.

Ensure the center of tooling hole to center of tooling hole tolerance is specified. See [Entry 1075](#)

- Precise location of tooling holes is critical for alignment purposes in multiple manufacturing processes.

Specify soldermask touchup / rework is not allowed within 6.3500mm of [discrete 01005](#) and [discrete 0201](#) components.

- Soldermask touchup / rework could adversely affect solderpaste printing and manufacturing yield.

The minimum PCB slot width = 0.7750mm

- Narrower slots may not be manufacturable at the PCB vendor due to the smaller drill bits being more likely to break.
- The recommended slot width = 1.5500mm

## Related Entries

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[DFM Rule 1075](#) PCB Design > General > Tooling Holes

DFM > Data and Deliverables > General

Entry ID: 1731

## Assembly Drawing

### Guideline

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 2 | Content Owner: Jabil | Content Type: Information |
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#### Introduction:

The assembly drawing shows the assembly details, chemistry, quality and inspection requirements and information that will be needed to assemble the product.

|        |                      |                           |
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| CID: 3 | Content Owner: Jabil | Content Type: Requirement |
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Reference designators must be present and readable in the assembly drawing.

- Reference designators are important for test and repair processes.

Specify torque requirements for all applicable hardware and components in the assembly drawing.

- Incorrect or unspecified torque values can damage the product.

Specify attachment methods and processes in the assembly drawing.

- Not having clear instructions for application of materials such as staking, bonding, gluing, sealing, tacking etc. can adversely affect manufacturing.

Specify cleanliness requirements in the assembly drawing.

- If there are specific cleanliness requirements, verifying compatibility with existing processes is necessary for a thorough design analysis.

Identify unpopulated component locations in the assembly drawing.

- Ensuring unpopulated (no-pop) locations are identified is necessary so the [BOM](#) can be verified.

Ensure [solder ball](#) requirements do not exceed [IPC](#) requirements in the assembly drawing.

- Eliminating all solder balls is difficult or impossible and inspecting for solder balls is also difficult.

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DFM > Data and Deliverables > General

Entry ID: 1732

## Data Package

### Guideline

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 2 | Content Owner: Jabil | Content Type: Information |
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#### Introduction:

Some information is necessary prior to performing a design review. Without this information, a complete design review is not possible and there may be negative affects in manufacturing.

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| CID: 3 | Content Owner: Jabil | Content Type: Requirement |
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Referenced documents are not provided.

- Not having documents that are referenced in drawings, assembly notes etc. prevents having an understanding of customer acceptability requirements and a thorough analysis of the product.

Specify the expected product volume, manufacturing mode and manufacturing site.

- This can have a significant impact on the criticality of design elements and the level of detail required in the design review.

Specify new / atypical technologies, processes and / or assembly methods.

- Not having this information can affect the design review and feedback.

Identify packaging requirements.

- Packaging requirements need to be specified in advance to prevent issues during transport.

Specify certification requirements.

- Understanding certification requirements is necessary for performing a thorough design analysis.

Specify post assembly hardware.

- Drawings that specify the clearance, assembly process etc. are necessary for performing a thorough design analysis.

Specify if the assembly will be tested and how.

- Understanding how test may impact the design is necessary for a thorough design analysis.

Include blank label part numbers in the BOM or documentation and specify locations in the silkscreen or soldermask layer.

- This could result in the correct blank labels not being in stock or confusion around the appropriate location creating assembly delays.

Provide documentation and installation instructions for cages and light pipes.

- Not identifying cages and light pipes and how they will be installed / at what level can cause production delays.

Ensure PEM nuts and the design are compatible and provide the press requirements.

- PEM nuts can be difficult or impossible to assemble if the design is not compatible and / or the pressing requirements are not provided.

Provide press fit component datasheets, equipment and tooling requirements.

- Not having the component hole sizes based on board finish in addition to equipment and tooling requirements can adversely affect manufacturing or cause delays.

Provide documentation and / or 2D drawings for mechanical requirements such as screws, washers, heat sinks, clips, rivets, PEM nuts, mounting hardware etc.

- Not having the requirements will prevent a thorough design review.

For component under fill: please specify the material, process, cure time, inspection criteria, etc.

- Solder joints may be prone to cracking if the material, process, cure time etc. is not sufficient to maintain the stability of the part.

Specify variable use materials.

- Not having variable use materials identified can delay manufacturing and prevent a thorough design analysis.

Specify white soldermask requirements.

- The requirements need to be specified so that visual appearance is as intended.

Ensure customer solder voiding requirements do not specify less than 30%.

- Requirements for solder voiding less than 30% may be difficult or impossible to meet. Special equipment such as VRO reflow ovens, chemicals / materials (solderpaste, flux, etc.), pre-processing steps, and other manufacturing solutions may increase cost and complexity, while still not meeting this low voiding requirement. Prior to production, a study to evaluate the combination of the PCB, components, equipment, assembly processes, and chemicals / materials necessary to achieve the desired voiding percent is highly recommended.

Ensure voiding requirements for coatings adhere to IPC requirements.

- Statements requiring exceptional voiding limitations for coating materials beyond typical IPC requirements may be difficult or impossible to meet.

Specify conformal coating materials, processes and allowable areas.

- Understanding coating materials, processes, areas and keep-outs are necessary for a thorough design analysis.

DFM > Data and Deliverables > General

Entry ID: 1735

## Two Pin Component Polarity

### Guideline

CID: 2

Content Owner: Jabil

Content Type: Requirement

Verify two pin component polarity (example: diodes) against the schematic.

- Product functionality could be affected.

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DFM > Data and Deliverables > General

Entry ID: 1766

## Array Drawing

### Guideline

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 3 | Content Owner: Jabil | Content Type: Information |
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#### Introduction:

The array drawing shows various elements of the design, tolerances, details specific to the array that will be needed by the PCB vendor.

|        |                      |                           |
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| CID: 2 | Content Owner: Jabil | Content Type: Requirement |
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Ensure the array drawing contains tooling holes that meet the same requirements as tooling holes for individual PCBs. See [Entry 1075](#).

- Tooling holes on the array rails will function the same as tooling holes for each PCB in the array so all requirements apply at the array level.

Ensure the X and Y locations of each PCB in the array are clearly defined on the array drawing from the center of the array datum hole to the center of the PCB datum hole and have the correct tolerance specified. See [Entry 1075](#).

- Tooling holes require precise alignment in many manufacturing processes.

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DFM > PCB Design > General

Entry ID: 1051

## PCB / Panel Size

### Rule

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 4 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Do not exceed maximum **PCB** or **panel** size of 457.2000mm Length x 355.6000mm Width x 5.0000mm Thickness.

- Larger products will not fit onto a standard **SMT chip shooter**. The product will need to be manufactured on equipment with large PCB capability, possibly adding cost and processing time.

|        |                      |                           |
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| CID: 5 | Content Owner: Jabil | Content Type: Requirement |
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When possible, choose PCBs that are thicker than 1.0000mm

- Thin PCBs are prone to warping, potentially resulting in **solderpaste** printing, **reflow soldering**, and **SMT** placement issues.
- Thin PCBs may get caught in the transport conveyors during assembly and / or require extra tooling such as a pallet or central board support, resulting in additional cost.

### Related Entries

DFM Guideline [1558](#) PCB Design > General > Vendor Multi-PCB Panels

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## PCB Layer Stack-up

### Rule

CID: 2

Content Owner: Jabil

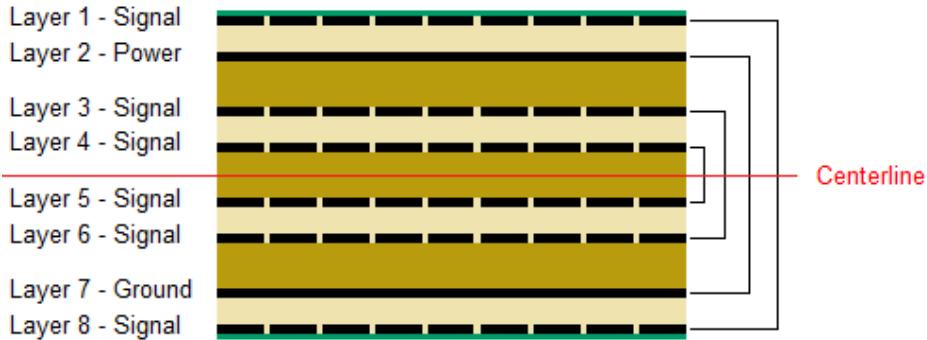
Content Type: Requirement

The [PCB layer stack-up](#) should be symmetrical in relation to the Z-axis with regard to dielectric thicknesses, copper weights, and layer design in order to minimize board warp during assembly.

- Balance inner layer thickness and copper weights.
- Balance metal distribution across each layer and through the stack-up. Cross-hatching or other relieving of the planes may aid in this balancing.

Non-symmetrical designs may result in warped boards that cannot be assembled and/or installed in product. When a multi-layer board has an odd number of layers, this will often lead to board warp problems. Adding a non-functional layer to balance the stack-up will minimize the potential for warpage. A non-functional layer may be a plane layer with the copper relieved from all holes (no interconnects), or a simulated signal layer with no connections to any holes.

Example of proper layer construction where layer 1 = layer 8, 2 = 7, 3 = 6 and 4 = 5.



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## BGA Pads and Trace Connections

### Rule

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 3 | Content Owner: Jabil | Content Type: Requirement |
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Do not connect more than one [trace](#) to each [BGA](#) component [pad](#).

- Multiple trace connections increase the solderable area which can adversely affect solder joint formation.

Utilize metal defined pads for all BGA component pins.

Do not place BGA component pads in copper fill areas.

Limit BGA trace width connections to a maximum of 60% of the pad diameter.

- Placing BGA pads in copper fill areas results in soldermask defined pads and may reduce solder joint reliability.
- Soldermask defined pads and large trace connections influence the solder joint shape and reliability.

For BGA pads, utilize a teardrop design for connecting trace widths less than or equal to 0.1500mm. See [Entry 1299](#) for additional teardrop pad design details.

- This can allow the drill to break the pad to trace connection if drilled off center or may result in trace cracking at the pad to trace junction due to thermal cycling.

Utilize the same size and shape pad for all ball locations within a single BGA component.

- Multiple sizes and shapes can make it difficult to achieve consistent soldering connections.

Avoid routing traces between the pads of BGAs with a [pitch](#) of 0.5000mm or less.

- Maintaining the minimum [copper to copper](#) spacing between the trace and pads (see [Entry 1031](#)) may not be possible, resulting in having to remove copper from the pads to maintain clearance. Pads that are not round and consistently sized with all other pads in the component, may result in soldering issues. This could also adversely affect the soldermask clearance, negatively impacting soldering.

Select round pads for BGA, [CBGA](#), [Flip Chip](#) and [CSP](#) components.

- Round pads form the strongest solder joint with components that have balls for pins.
- If X-ray is required, consider using different pad geometries for enhanced defect detection (see [Entry 1349](#)). There is an unknown impact when using another pad shape.

### Related Entries

[DFM Guideline 1299](#) PCB Design > Traces > Narrow Trace Connections to Pads

DFM > PCB Design > General

Entry ID: 1075

## Tooling Holes

### Rule

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 2 | Content Owner: Jabil | Content Type: Requirement |
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Tooling holes must be **NPTHs**.

- Plated tooling holes prevent the **PCB** from fitting onto the alignment pins some of the time due to plating thickness variation.

|         |                      |                           |
|---------|----------------------|---------------------------|
| CID: 11 | Content Owner: Jabil | Content Type: Requirement |
|---------|----------------------|---------------------------|

### Per PCB:

Provide a minimum of 2 tooling holes.

- Tooling holes are used for precise PCB alignment purposes in many manufacturing processes. Three are preferred as a way of preventing loading the PCB onto the equipment backwards.

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 3 | Content Owner: Jabil | Content Type: Requirement |
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### Per Panel:

Provide a minimum of 2 tooling holes.

- Tooling holes are used to align the PCB in multiple processes during manufacturing. Three are preferred as a way of preventing loading the panel onto the equipment backwards.
- Panel tooling hole requirements do not override the individual PCB tooling hole requirements, both are necessary.

A tooling hole within the outline of the PCB is preferred as the datum. If the PCB is too small for tooling holes, the datum should be established on a tooling hole on the panel.

- Locating the PCB datum on a tooling hole location helps to reduce the accumulation of dimension tolerance stackup error that impacts critical alignment in manufacturing.

If there is insufficient room for tooling holes within the outline of the PCB, a panel or rails are required and the tooling holes will be located on the panel or rail.

- Tooling holes are required for precise alignment purposes in many manufacturing processes.

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 4 | Content Owner: Jabil | Content Type: Requirement |
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Locate tooling holes as far apart as possible in diagonally opposed corners of the PCB or panel.

- Lack of opposing tooling holes negatively impacts alignment stability.

Offset tooling holes at different distances from their respective corners of the PCB or panel.

- The PCB / panel will not fit on the equipment backwards if the tooling holes are offset.

For products designed in Metric: center of tooling hole to center of tooling hole maximum tolerance =  $\pm 0.0250\text{mm}$

For products designed in Imperial: center of tooling hole to center of tooling hole maximum tolerance =  $\pm 0.001"$

- Precise location of tooling holes is critical for alignment purposes in multiple manufacturing processes.

CID: 20

Content Owner: Jabil

Content Type: Requirement

For products designed in Metric: tooling hole diameter =  $4.0000\text{mm} +0.0750\text{mm} -0.0000\text{mm}$

- Tooling holes need to be a standard size because they are used for critical alignment purposes for multiple processes.
- If the diameter of the tooling hole is any less than the negative tolerance, the PCB is at risk of getting stuck on the tooling pin. When the hole diameter is greater than the positive tolerance, the precise alignment required for manufacturing processes could be compromised.
- Other smaller diameters may also work but will need to be checked with process experts.

CID: 26

Content Owner: Jabil

Content Type: Requirement

For products designed in Imperial: tooling hole diameter =  $0.158" +0.003" -0.000"$

- Tooling holes need to be a standard size because they are used for critical alignment purposes for multiple processes.
- Less preferred but alternative tooling hole diameter =  $0.125" +0.003" -0.000"$ .
- If the diameter of the tooling hole is any less than the negative tolerance, the PCB is at risk of getting stuck on the tooling pin. When the hole diameter is greater than the positive tolerance, the precise alignment required for manufacturing processes could be compromised.

CID: 21

Content Owner: Jabil

Content Type: Requirement

Minimum spacing from edge of tooling hole to edge of PCB or rails =  $3.0000\text{mm}$

- Equipment clearances are required for multiple processes.

CID: 22

Content Owner: Jabil

Content Type: Requirement

Minimum clearance height over a tooling hole for features and component bodies =  $50.0000\text{mm}$

- The area above tooling holes should not be obstructed by features such as component bodies, [heat sinks](#), [light pipes](#), shields, brackets, etc.

CID: 23

Content Owner: Jabil

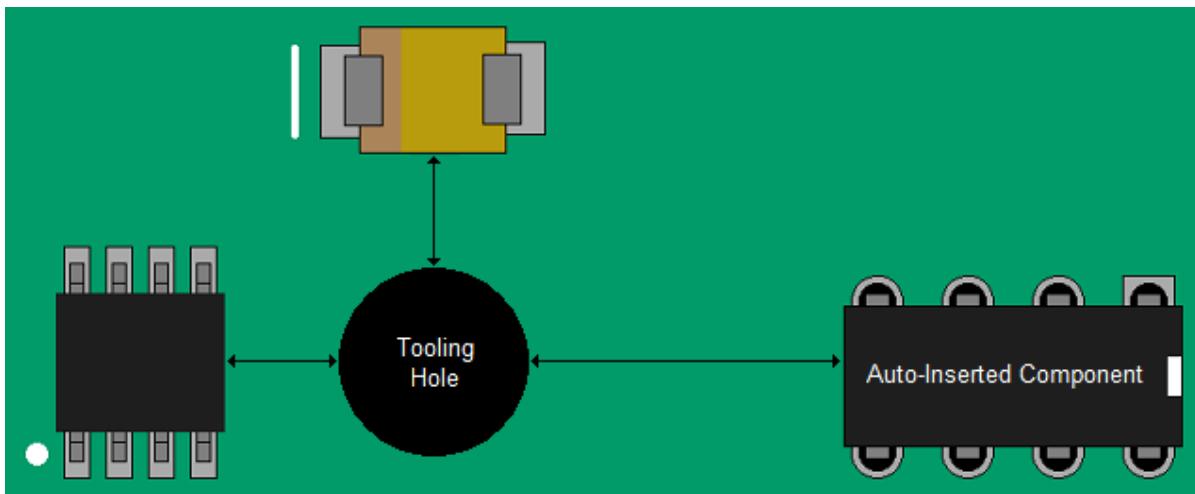
Content Type: Requirement

Minimum spacing from edge of tooling hole to component body on [primary](#) and [secondary](#) sides of the PCB =  $1.0500\text{mm}$

- Tooling hole clearances are required so that components are not damaged by making contact with the positioning pins.

Minimum spacing from edge of tooling hole to [THMT auto-inserted](#) component body on primary and secondary sides of the PCB =  $1.2500\text{mm}$ .

- Extra equipment clearances are required for the [THMT](#) auto-insertion process.
- Exceptions for THMT auto-insertion equipment types can be obtained from the equipment user guides.



CID: 24

Content Owner: Jabil

Content Type: Requirement

Minimum spacing from the edge of a [test point](#) to the edge of a tooling hole on the primary side of the PCB = 1.2500mm

- Test points within the tooling hole keep-out area interfere with special push cylinders that can be placed over tooling pins to prevent binding when the test fixture is engaged.

CID: 25

Content Owner: Jabil

Content Type: Requirement

Minimum spacing from the edge of a test point to the edge of a tooling hole on the secondary side of the PCB = 3.5000mm

- Test points within the tooling hole keep-out area interfere with special push cylinders that can be placed over tooling pins to prevent binding when the test fixture is engaged.

## Related Entries

---

[DFM Rule 1292](#) PCB Design > General > Mounting Holes

[DFM Rule 1034](#) PCB Design > Test Points > Test Points

[DFM Rule 1136](#) PCB Design > Test Points > Test Point to Component Spacing

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## Thermal Reliefs

### Rule

CID: 16

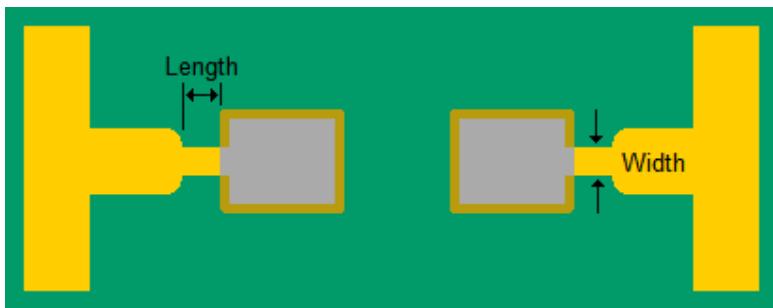
Content Owner: Jabil

Content Type: Requirement

Ensure SMT pads are thermally relieved on outer layers connected to large copper features or plane areas with a rounded neck down trace a maximum of 1/2 the pad width and a minimum of 0.1500mm in length.

- SMT pads with inadequate thermal relief can result in uneven solder reflow and can cause tombstoning or cold solder joints.

**Note:** Electrical current capacity, thermal dissipative and / or RF requirements may override the need for compliance.



CID: 19

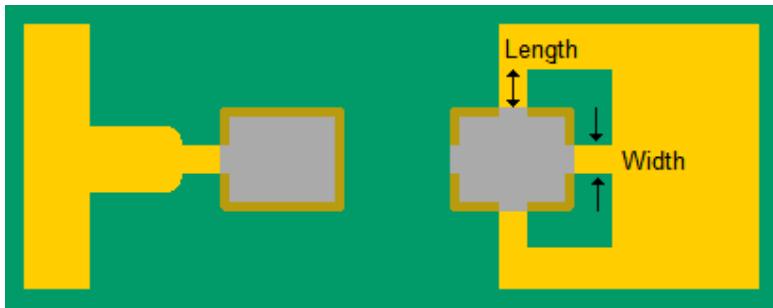
Content Owner: Jabil

Content Type: Requirement

Ensure soldermask defined SMT pads that are part of a large conductor or plane area on the outer layers are thermally relieved with traces that are a maximum of 1/2 the pad width, a minimum of 0.1500mm in length and connected at the midpoint of the pad.

- Soldermask defined pads with inadequate thermal relief can result in uneven solder reflow and can cause tombstoning or cold solder joints.

**Note:** Electrical current capacity, thermal dissipative and / or RF requirements may override the need for compliance.



CID: 24

Content Owner: Jabil

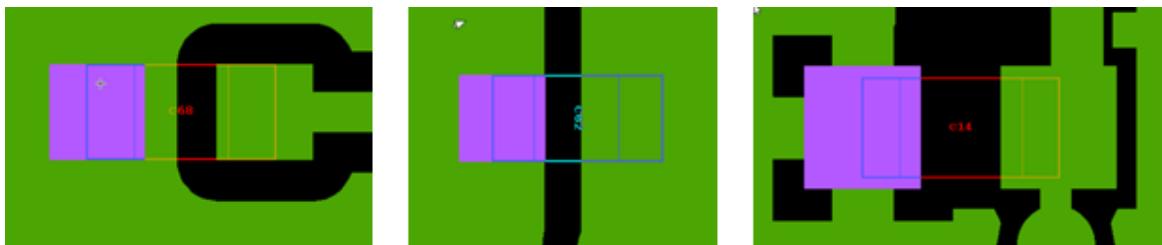
Content Type: Requirement

For 0805 and smaller discrete components, ensure the cumulative width of traces attached to the pads does not exceed a 3 to 1 ratio between one pad versus the other.

For 0805 and smaller discrete components, utilize thermal reliefs for pads contained within planes.

- This can lead to solderability issues, tombstones, etc.
- Copper imbalance between small discrete component pads may result in reduced first pass yield and tombstones.

- Thermal reliefs in the plane can be utilized to balance the copper contact area / thermal mass.
- Pads in planes are not preferred but if necessary for electrical reasons, having the same copper contact area / thermal mass on both sides of the discrete component is recommended.



One pad is defined in a plane, the opposite pad is connected to a trace



Both pads are connected to planes, thermally balanced



One pad is in a plane but has thermal reliefs, thermally balanced

CID: 4

Content Owner: Jabil

Content Type: Requirement

#### For tin lead and lead-free wave and selective soldering:

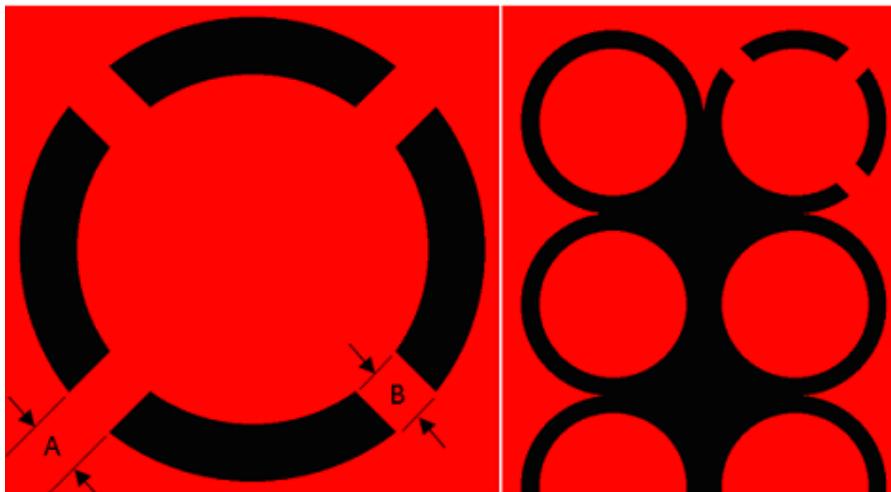
Provide thermal reliefs or clearances for all **PTH** barrels connected to power and ground layers, planes, or large copper features.

- This can cause insufficient hole fill, loss of solder fillet, and rework issues.
- Thermal reliefs or clearances are required to reduce soldering dwell time by providing thermal isolation. This makes it easier to solder and de-solder **THMT** components connected to power and ground layers, planes or large copper features.

For positive or mixed power and ground imaged layers, a maximum of four thermal relief spokes per barrel, per layer.

For positive or mixed power and ground imaged layers, the maximum thermal relief spoke width (Dimension A) = 0.2500mm

- This can cause insufficient hole fill, loss of solder fillet, and rework issues.



CID: 22

Content Owner: Jabil

Content Type: Requirement

#### For tin lead and lead-free wave and selective soldering:

A maximum of two inner layer planes can be connected to a single PTH barrel.

For signal layers or negative power and ground imaged layers, provide a maximum of four thermal relief spokes per barrel, per layer.

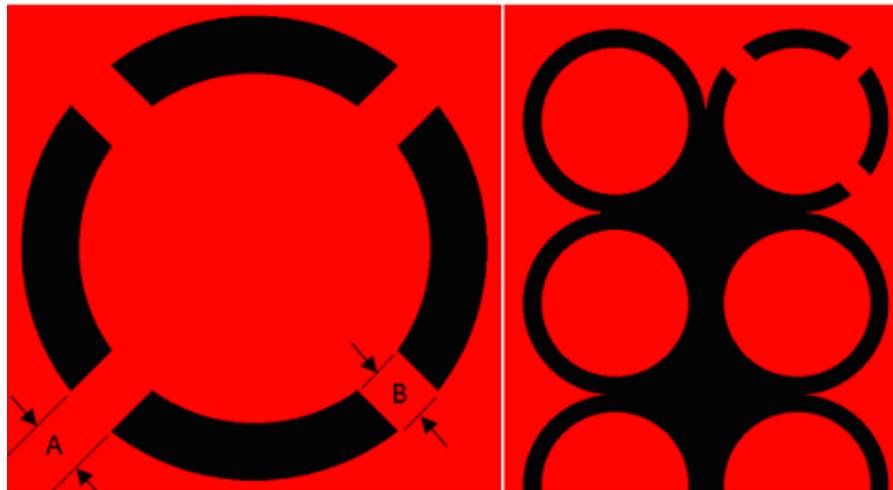
For signal layers or negative power and ground imaged layers, the maximum thermal relief spoke width (Dimension A) = 0.2500mm

Minimum spoke length (Dimension B) = 0.2500mm

- This can cause insufficient hole fill, loss of solder fillet, and rework issues.

Place thermal relief spokes at a 45° or 90° orientation to the axes of the component pin layout.

- This can result in spoke loss due to encroaching **anti-pads** from adjacent leads.



The above requirements apply for **PCBs** designed with up to 2 oz copper planes.

Contact the [Enterprise DFx Team](#) for design requirements beyond these limits or PCBs thinner than 1.5000mm or thicker than 3.0000mm.

Please reference [IPC-2221](#) and associated sectional standards for electrical implementation details.

## Related Entries

---

DFM Guideline [1039 Component Land Pattern > General > Selective and Wave Soldered THMT Component Pads](#)

DFM Rule [1077 PCB Design > General > Auto-Insertion](#)

DFM Rule [1314 Component Land Pattern > General > Selective and Wave Soldered THMT Component Hole Size](#)

## Auto-Insertion

### Rule

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 8 | Content Owner: Jabil | Content Type: Information |
|--------|----------------------|---------------------------|

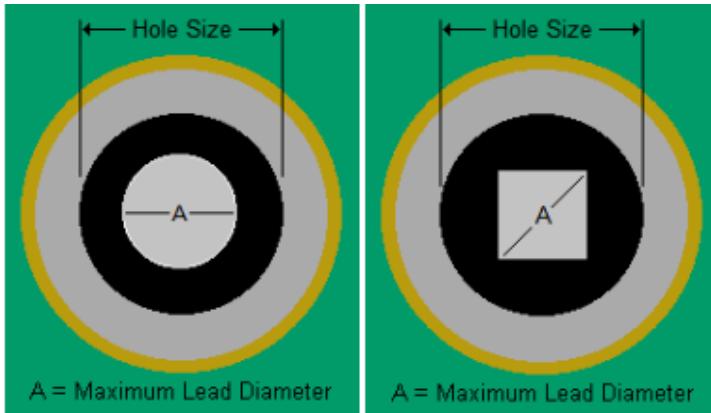
Whenever possible, **THMT auto-inserted** component variation for body size, lead tip (pointed vs. square), and lead diameter should be minimized. Unnecessary component variation can increase tooling changes and reduce production efficiency.

Whenever possible, **THMT** auto-inserted components should be placed in one axis parallel to the conveyed **PCB** edge. Unnecessary orientation differences can negatively affect programming, placement and inspection.

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 9 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

For auto-inserted **axial**, **DIP** and **radial** components: hole size = maximum lead diameter + 0.4500mm ±0.0750mm

- If the hole size is too small this can result in pin insertion issues, too large can result in component retention issues.
- The hole sizes should be checked for compatibility with the equipment in use.



### Related Entries

DFM Rule [1075](#) PCB Design > General > Tooling Holes

DFM Guideline [1082](#) Component Placement > Orientation > Wave Solder Component Orientation

DFM Guideline [1115](#) Component Selection > Through Hole Mount > DIP Component Selection

DFM Information [1398](#) PCB Design > General > Lead Span for Axial Components

DFM Guideline [1039](#) Component Land Pattern > General > Selective and Wave Soldered THMT Component Pads

## RF Circuits and Printed Filters

### Guideline

CID: 2

Content Owner: Jabil

Content Type: Requirement

For RF circuits, do not use printed filters. Printed filters may increase the possibility of scrap because they cannot be reworked. Also, the electrical characteristics of printed filters can vary due to material tolerance, temperature, etching accuracy, etc. A printed filter may also need to be tuned to meet certain rejection, insertion loss and impedance matching at its input and output.

Drop-in filters can be pre-tuned and measured outside the circuit to assure the specification is met. The filter is then installed on the populated board. The filter's outside jacket is often completely grounded, exposing only the input and output leads.

If considering the use of printed filters on a design, a trade-off between the recurring costs of the filter components versus printed filter yield, the number of scrapped boards and the troubleshooting costs need to be weighed when determining the optimum solution.

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## Automated X-ray Surface Mapping

### Guideline

CID: 2

Content Owner: Jabil

Content Type: Requirement

Provide reference points for automated X-ray surface mapping. A copper plane should be located at or near the PCB's surface (typically one of the first two layers) on the same layer across the entire PCB.

Three dimensional X-ray inspection systems must determine the PCB surfaces exact physical distance from the X-ray source in order to accurately view solder joint images. The system accomplishes this by locating and mapping the PCB's surface with a laser source at numerous locations across the PCB.

These surface map points compensate for variations in the PCB warpage and provide exact Z-axis distances from the X-ray source for all solder joints. To facilitate this step in the test development process, a laser visible copper plane provides an excellent target for the surface map laser.

Verify equipment in use, systems other than 5Dx may not require surface mapping.

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DFM > PCB Design > General

Entry ID: 1292

## Mounting Holes

### Rule

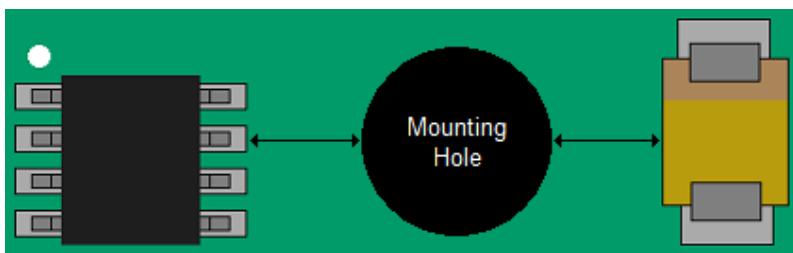
CID: 7

Content Owner: Jabil

Content Type: Requirement

Minimum spacing from edge of hardware [mounting holes](#) to component body or pad on [primary](#) and [secondary](#) sides of the [PCB](#) = 3.8000mm

- Clearance, including the screw / washer and movement within the mounting hole, is necessary to avoid damaging components and / or interference while installing the PCB in the chassis.



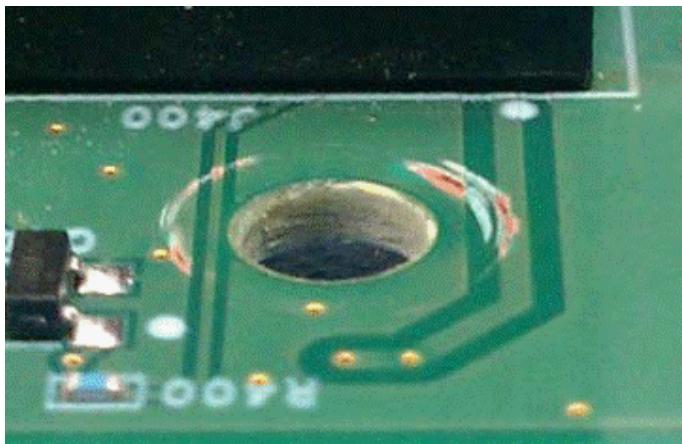
CID: 8

Content Owner: Jabil

Content Type: Requirement

Minimum clearance from edge of mounting screw / washer to [copper](#) on all layers = 1.0000mm including movement of the screw / washer within the mounting hole.

- This can cause shorting between copper features on the outer layers and compression of inner layers that can break down the dielectric, causing shorts between layers, when installing the PCB in the chassis.



CID: 10

Content Owner: Jabil

Content Type: Requirement

Maintain a copper keep-out area on the layer adjacent / below a mounting hole pad.

- A mounting hole pad can be shorted to the copper on adjacent layers when the mounting screw is tightened.

CID: 9

Content Owner: Jabil

Content Type: Requirement

Mounting holes should be [NPTHs](#).

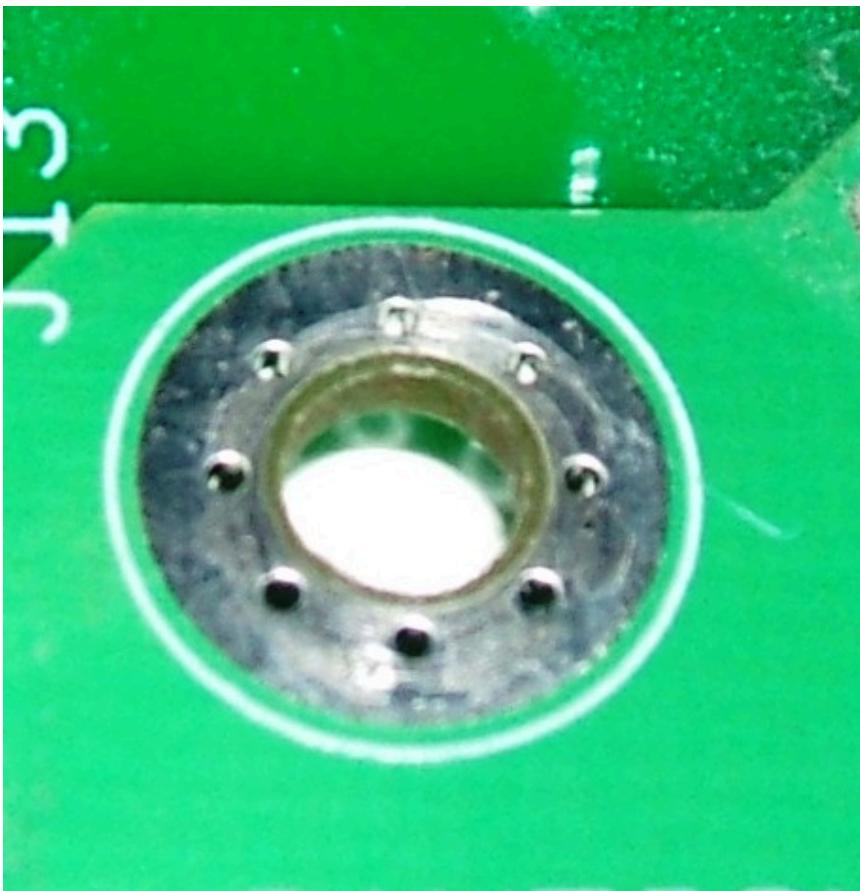
- Plated mounting holes can release metal shavings with some fastener applications, increasing the risk of electrical shorts.

If mounting holes are used for grounding: add [solderpaste](#) to the pads of [OSP](#) coated PCBs.

- Electrical conductivity may be adversely affected by OSP and related surface finishes, adding solderpaste improves conductivity.

Incorporate a copper mounting hole pad on top and bottom layers that is 1.0000mm larger than the screw / washer, including movement within the mounting hole.

- A pad minimizes compression of inner layers that can break down the dielectric, causing shorts between layers, when installing the PCB in the chassis.



## Related Entries

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[DFM Rule 1075 PCB Design > General > Tooling Holes](#)

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DFM > PCB Design > General

Entry ID: 1295

## NPTH Clearance

### Rule

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 3 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

NPTHs (with the exception of [mounting](#) and [tooling holes](#)) must be a minimum of the hole diameter from the edge of the PCB.

- NPTHs that are too close may have the material between the hole and PCB edge break away.

See [Entry 1075](#) for tooling hole requirements.

Minimum clearance from edge of NPTH drill to edge of NPTH drill = 0.5000mm

- This can cause breakout between the two holes and damage the PCB or exceed the drilling equipment's ability to drill that close.
- **Note:** Does not apply to slots or [drilled breakaway \(mouse bite\)](#) tabs.

Minimum clearance from edge of PTH drill to edge of NPTH drill = 0.6350mm

Minimum clearance from edge of via drill to edge of NPTH drill = 0.3750mm

- This can cause breakout between the two holes and damage the PCB or exceed the drilling equipment's ability to drill that close.

### Related Entries

DFM Guideline [1054](#) PCB Design > Vias > Vias and Micro-Vias

DFM Rule [1292](#) PCB Design > General > Mounting Holes

DFM Rule [1075](#) PCB Design > General > Tooling Holes

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## PTH in Pad for Components

### Guideline

CID: 2

Content Owner: Jabil

Content Type: Requirement

Do not use **PTH** in pad for any components except the thermal pads of **QFNs** or **SOTs (D-PAKs)**. If used, some form of mitigation may be required to keep solder from flowing into the PTH and away from the intended solder joint potentially causing bridging and / or insufficient solder. **Solderballs** from wicking may also cause a standoff of the stencil on the opposite side of the board.

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## Lead Span for Axial Components

### Information

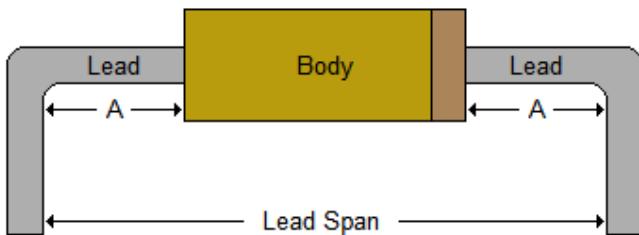
CID: 2

Content Owner: Jabil

Content Type: Information

The minimum lead span is based on "clean lead" from [axial](#) body to lead form (Dimension A):

- Dimension A = 2.0000mm
- Lead Span =  $2 \times (\text{Dimension A}) + \text{Body}$



**Note:** Dimension A = 1.9000mm is allowed but requires special attention to component selection and body centering during sequencing.

### Related Entries

DFM Rule [1077](#) PCB Design > General > Auto-Insertion

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## Surface Finish Selection

### Information

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 1 | Content Owner: Jabil | Content Type: Information |
|--------|----------------------|---------------------------|

### Surface Finish Types

| Surface Finish                   | Description   |
|----------------------------------|---|
| HASL (SnPb)                      | The PCB is immersed in a molten solder liquid then processed through a hot air stream to remove excess solder and provides the proper coating thickness on the SMT and the through holes. |
| Lead Free HASL (SnCu or SnAgCu)  | The PCB is immersed in a molten solder liquid then processed through a hot air stream to remove excess solder and provides the proper coating thickness on the SMT and the through holes. |
| OSP Copper                       | An imidazole based organic complex chemistry that selectively bonds with the copper to provide a protective layer for soldering.  |
| Imm Au (aka ENIG)                | A two metallic layer deposit: gold over nickel, plated onto the copper base by a series of chemical reaction processes.   |
| Electroplated Au (aka Hard Gold) | A two layer, gold over nickel, metallic surface finish plated onto the copper base by means of a electrolytic deposition process.   |
| Imm Ag Silver                    | A co-deposit of silver and organic compound.  |
| Imm Sn Tin                       | A co-deposit of tin and organic compound.   |

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 6 | Content Owner: Jabil | Content Type: Information |
|--------|----------------------|---------------------------|

### Advantages and Disadvantages

| Surface Finish | Advantages   | Disadvantages  |
|----------------|--|--|
| HASL (SnPb)    | <ul style="list-style-type: none"> <li>• 0.5000mm pitch capability and dependent on the technology</li> <li>• Board thickness up to 5.0000mm (horizontal process)</li> </ul> | <ul style="list-style-type: none"> <li>• Uniformity of the coating</li> <li>• Thermal shock</li> <li>• Limited capability on high density boards</li> <li>• Limited capacity to clear via holes (&gt; 6:1 aspect ratio)</li> <li>• Difficult to maintain hole size tolerance along plated edges</li> <li>• Difficult to process thin material</li> </ul> |

| Surface Finish                  | Advantages  | Disadvantages   |
|---------------------------------|---|---|
|                                 |   | <ul style="list-style-type: none"> <li>• Requires a different drill selection (<a href="#">press fit</a> connector dictates the drill)</li> <li>• This process is very dependent on the board technology</li> <li>• Intermetallic layer grows with time and heat cycle</li> <li>• Use of lead</li> </ul>  |
| Lead Free HASL (SnCu or SnAgCu) |   | <ul style="list-style-type: none"> <li>• Difficult to wet the alloy at assembly</li> <li>• Thinner deposit thus poor shelf life and poor multiple reflow capability</li> <li>• High copper erosion rate</li> <li>• More severe thermal shock (up to 270 C)</li> <li>• Difficult to apply the alloy on the PCB (requires multiple passes)</li> </ul>   |
| OSP Copper                      | <ul style="list-style-type: none"> <li>• Major advantage of OSP is cost.</li> </ul>   | <ul style="list-style-type: none"> <li>• Difficult or impossible to inspect the final product <ul style="list-style-type: none"> <li>◦ Skip plating</li> <li>◦ Residue on copper</li> <li>◦ Coating thickness</li> </ul> </li> <li>• Not compatible with <a href="#">tented / capped</a> vias.</li> <li>• Electrical test needs to take place prior to coating</li> <li>• ICT testing (at assembly)</li> <li>• Shelf life can be relatively short.</li> </ul> |
| Imm Au (aka ENIG)               | <ul style="list-style-type: none"> <li>• Excellent corrosion resistance</li> <li>• Good for aluminum wire bonding</li> <li>• Excellent flatness for fine pitch technology</li> <li>• Good contact resistance</li> </ul> | <ul style="list-style-type: none"> <li>• Narrow process window</li> <li>• Fatigue failures on large BGA packages</li> <li>• Skip plate</li> <li>• Extraneous nickel plating (nickel growth)</li> </ul>  |

| Surface Finish                      | Advantages   | Disadvantages  |
|-------------------------------------|--|--|
|                                     | <ul style="list-style-type: none"> <li>• High aspect ratio capability</li> </ul>   | <ul style="list-style-type: none"> <li>• Soldermask compatibility with the nickel bath</li> <li>• Nickel layer for RF applications (signal loss)</li> </ul>  |
| Electroplated Au<br>(aka Hard Gold) | <ul style="list-style-type: none"> <li>• Excellent corrosion resistance</li> <li>• 130 to 220 Knoop hardness</li> <li>• Excellent wear resistance, rotary switches, on-off contacts, and edge connectors</li> </ul>  | <ul style="list-style-type: none"> <li>• Solderable surface</li> <li>• Gold and nickel distribution</li> <li>• Nickel throwing power in the holes</li> <li>• Copper is exposed on the sides of the traces</li> <li>• Nickel slivers</li> <li>• Difficult to measure the true line width</li> <li>• Soldermask adhesion on gold</li> </ul>  |
| Imm Ag Silver                       | <ul style="list-style-type: none"> <li>• Very good alternative to HASL</li> <li>• Excellent for fine pitch and BGA technologies</li> <li>• High aspect ratio capability</li> <li>• Press fit connector capability</li> <li>• Multiple heat cycles during assembly process</li> <li>• Selective gold compatible</li> <li>• ICT testing capable</li> <li>• Tin copper intermetallic solder joints</li> </ul> | <ul style="list-style-type: none"> <li>• No extended thermal cycle after silver at the PCB level</li> <li>• Via cap: UV curable only</li> <li>• Handling considerations</li> <li>• Some resistance from the OEM to use Immersion Ag with press fit connectors</li> <li>• Concern around planar micro-voids in the solder joints</li> <li>• Silver discoloration during assembly</li> <li>• Silver discoloration in the field</li> <li>• Limited reworkability</li> </ul> |
| Imm Sn Tin                          | <ul style="list-style-type: none"> <li>• Back plane</li> <li>• Press fit connector technology</li> <li>• Reworkable</li> <li>• Coplanarity</li> <li>• Excellent for fine pitch and BGA technologies</li> <li>• High aspect ratio capability</li> </ul>   | <ul style="list-style-type: none"> <li>• Soldermask compatibility</li> <li>• Thiourea (TU)</li> <li>• Process controls: <ul style="list-style-type: none"> <li>◦ Tin bath high temperature</li> <li>◦ Solderability test (tin porosity)</li> <li>◦ Copper concentration</li> </ul> </li> </ul>   |

| Surface Finish | Advantages   | Disadvantages  |
|----------------|--|--|
|                | <ul style="list-style-type: none"> <li>• Press fit connector capability</li> <li>• Selective gold compatible</li> <li>• ICT testing capable</li> <li>• Tin copper intermetallic solder joints</li> </ul> | <ul style="list-style-type: none"> <li>◦ Rinsing</li> <li>◦ Tin IV</li> <li>• Intermetallic growth</li> <li>• Solderability goes down significantly with each reflow cycle</li> <li>• Tin thickness alone doesn't warrant solderability</li> </ul> |

CID: 4

Content Owner: Jabil

Content Type: Information

## Characteristics

| Surface Finish                   | RoHS Compliant (<0.1wt%Pb) | Solderability | Cost (HASL SnPb=1.0) | Shelf Life  | Typical Thickness                                       | Surface Coplanarity |
|----------------------------------|----------------------------|---------------|----------------------|-------------|---|---------------------|
| HASL (SnPb)                      | No                         | Very Good     | 1                    | 6 Months    | 100-1000u"  | 50-1500u"           |
| Lead Free HASL (SnCu or SnAgCu)  | Yes                        | Very Good     | 1.1x                 | 6 Months    | 100-1000u"  | 50-1500u"           |
| OSP Copper                       | Yes                        | Good          | 1x                   | 12 Months   | 8-20u"  | 5-20u"              |
| Imm Au (aka ENIG)                | Yes                        | Excellent     | 2x                   | 6-12 Months | 3-8u" Au<br>150-250u" Ni                                | 150-250u"           |
| Electroplated Au (aka Hard Gold) | Yes                        | Excellent     | 2-3x                 | 12 Months   | 3-12u" Au soldering<br>30-50u" Au contacts<br>>200u" Ni | Varies with design  |
| Imm Ag Silver                    | Yes                        | Good          | 1x                   | 6 Months    | 3-12u" Ag   | 3-7u"               |
| Imm Sn Tin                       | Yes                        | Good          | 1x                   | 6 Months    | 40-60u" Sn  | 30-50u"             |

CID: 5

Content Owner: Jabil

Content Type: Information

## Notes

| Surface Finish                  | Fab Note Specifications        | Pin Probeable (ICT / Flying Probe) | Historical Issues   | Additional Notes  |
|---------------------------------|--------------------------------|------------------------------------|---------------------|---|
| HASL (SnPb)                     | Specify max and min thickness. | Preferred                          | Coplanarity of pads |   |
| Lead Free HASL (SnCu or SnAgCu) | Specify max and min thickness. | Preferred                          | Coplanarity of pads | Specify same alloy as used in solderpaste, bar and wire solder. |

| Surface Finish                   | Fab Note Specifications  | Pin Probeable (ICT / Flying Probe) | Historical Issues             | Additional Notes  |
|----------------------------------|--|------------------------------------|-------------------------------|---|
| OSP Copper                       | Specify vendor and type of OSP to be used.   | Preferred                          |                               | Reduced wetting is expected on boards with OSP Cu if wave soldering after double sided SMT assembly or during rework.   |
| Imm Au (aka ENIG)                | Specify thickness of Ni and Au with tolerance.   | Alternate                          | Black pad, gold embrittlement |   |
| Electroplated Au (aka Hard Gold) | Specify thickness of Ni and Au with tolerance. Clearly identify Hard Gold on additional named CAD layer. | Alternate                          |                               |   |
| Imm Ag Silver                    | Specify vendor and type as required.   | Alternate                          | Silver sulfide dendrites      | Significant tarnishing is observed on boards with Imm Ag finish after double sided SMT assembly or rework. Fingerprints are a significant contributor, may specify gloves for handling. |
| Imm Sn Tin                       | Specify vendor and type as required.   | Alternate                          | Tin whiskers                  |   |

CID: 7

Content Owner: Jabil

Content Type: Information

## Assembly Process

| Surface Finish                   | Less Than 0.5000mm Pitch | BGA  | Hand Soldering | Wave Soldering | Paste Misprint (Auto Wash)     | Surface Finish Durability | Use In Press Fit Applications |
|----------------------------------|--------------------------|--|----------------|----------------|--------------------------------|---------------------------|-------------------------------|
| HASL (SnPb)                      | Poor                     | Good   | Excellent      | Excellent      | Normal                         | Excellent                 | Excellent                     |
| Lead Free HASL (SnCu or SnAgCu)  | Poor                     | Good   | Excellent      | Excellent      | Normal                         | Excellent                 | Acceptable                    |
| OSP Copper                       | Excellent                | Excellent                                    | Good           | Good           | Less hold time between reflows | Fragile                   | Acceptable                    |
| Imm Au (aka ENIG)                | Excellent                | Very Good                                    | Excellent      | Excellent      | Critical                       | Fragile                   | Acceptable                    |
| Electroplated Au (aka Hard Gold) | Very Good                | Very Good (thin deposits and reflow control) | Excellent      | Excellent      | Critical                       | Good                      | Acceptable                    |
| Imm Ag Silver                    | Excellent                | Excellent                                    | Excellent      | Excellent      | Normal                         | Fragile                   | Acceptable                    |
| Imm Sn Tin                       | Excellent                | Excellent                                    | Excellent      | Excellent      | Normal                         | Fragile                   | Best Alternative              |

## Related Entries

DFM Information [1326](#) PCB Design > Vias > Via Treatments

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## Vendor Multi-PCB Panels

### Guideline

CID: 4

Content Owner: Jabil

Content Type: Information

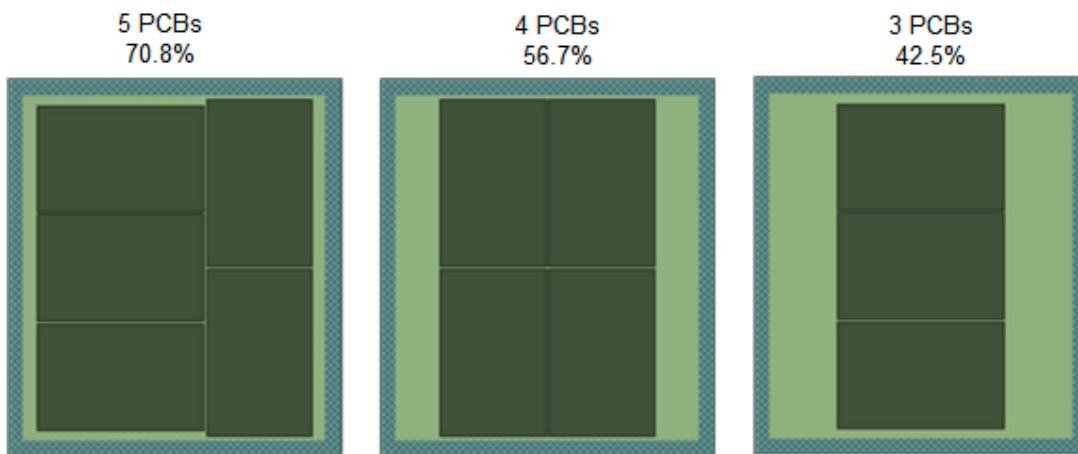
These guidelines apply to rigid **PCB** technology.

This entry specifically deals with the panels utilized by PCB vendors and does not supersede maximum factory PCB / panel size as described in [entry 1051](#). The panel may be separated by the vendor before shipping to the factory so it is possible to design a PCB vendor panel that is larger and still meet the factory maximum PCB / panel size.

Panel utilization is calculated as follows:

$$(\text{PCB Area} \times \text{Number of PCBs}) / \text{Total Panel Area}$$

There are many third party tools available to assist with this calculation and optimizing utilization, a commonly used tool is "KwickFit" by MicroMega Solutions. The below example represents a 28% increase in vendor panel utilization.



Available panel sizes must be verified with the supply chain selected PCB vendor build site before designing a panel but typically available sizes are listed in the table below for reference. Taking advantage of a larger size may be necessary to maximize the vendor panel utilization and minimize individual PCB cost.

| Width      | Length     |
|------------|------------|
| 304.8000mm | 457.2000mm |
| 406.4000mm | 457.2000mm |
| 419.1000mm | 469.9000mm |
| 406.4000mm | 533.4000mm |
| 457.2000mm | 533.4000mm |
| 457.2000mm | 609.6000mm |
| 469.9000mm | 622.3000mm |
| 469.9000mm | 698.5000mm |
| 482.6000mm | 558.8000mm |
| 508.0000mm | 609.6000mm |
| 533.4000mm | 609.6000mm |
| 546.1000mm | 622.3000mm |
| 533.4000mm | 685.8000mm |
| 546.1000mm | 698.5000mm |

| Width      | Length     |
|------------|------------|
| 609.6000mm | 609.6000mm |
| 609.6000mm | 685.8000mm |
| 622.3000mm | 698.5000mm |
| 609.6000mm | 762.0000mm |
| 609.6000mm | 914.4000mm |

CID: 2

Content Owner: Jabil

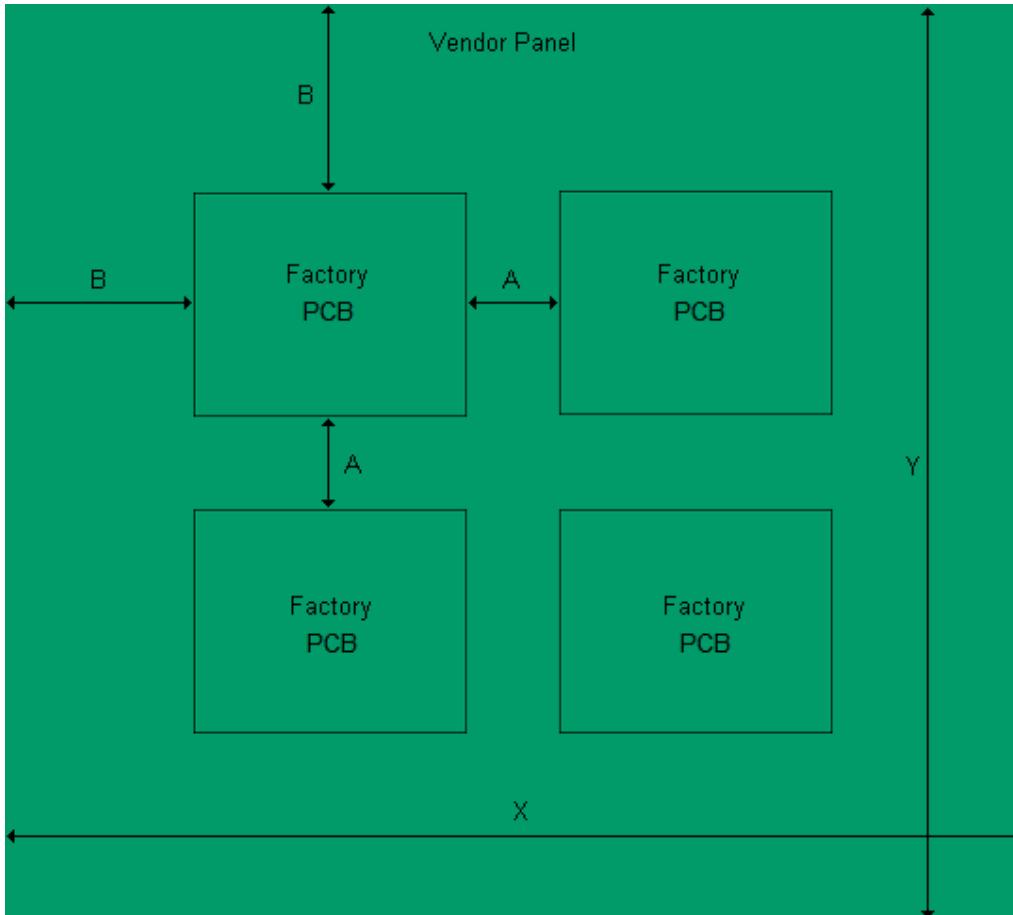
Content Type: Requirement

Achieve PCB vendor panel utilization of 80% or greater by accommodating vendor panel size and spacing requirements.

- If panel utilization is not optimal, there can be a significant individual PCB cost penalty.

There are three critical factors in determining optimal panel utilization that must be verified with the PCB vendor:

- Available PCB vendor panel sizes (X & Y).
- Minimum spacing between PCBs in a panel (A).
  - There must be enough space between PCBs in a panel so that a router can remove the material between them.
- Minimum spacing from edge of PCBs to outer edge of the panel (B).
  - A non-used border is required around the perimeter of a vendor panel.



For PCB panel arrays: choose rounded or chamfered corners.

- Rounded or chamfered corners are less likely to jam at conveyor transfer points, disrupting manufacturing.

Utilize bad board marks for multi-PCB panels.

- If bad board marks are not present in the individual PCBs in a panel, a PCB that is not functional could be built by mistake.

Utilize inner copper layers in the frame and breakaways of multi-PCB panels.

- If multi-PCB panels are not rigid enough, the panel may warp and sag during the soldering processes.

## Related Entries

---

DFM Rule [1051](#) PCB Design > General > PCB / Panel Size

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DFM > PCB Design > General

Entry ID: 1572

## Conformal Coating

### Guideline

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 3 | Content Owner: Jabil | Content Type: Information |
|--------|----------------------|---------------------------|

#### Introduction:

A study of [underfill](#) and / or [conformal coating](#) materials and their interactions with the [PCB](#) and components in accelerated life tests is highly recommended, especially in high reliability environments.

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 2 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Minimum distance between uncoated areas to conformal coating areas = 3.0000mm

- This is necessary to allow for typical material flow and / or overspray without affecting uncoated areas.
- Closer distances may require extra cost in labor, equipment, and materials.
- **Note:** closer distances may require trials to be conducted with the assembly, coating equipment, and coating material in order to determine capability.

Avoid applying conformal coating thicker than the package standoff height to bottom terminated components other than [D-Pak](#) components.

- Solder joint reliability can be severely impacted by conformal coating that is too thick, due to the coating causing a greater effective [CTE](#) relative to the PCB that increases the shear loads introduced to the solder joints, causing failure.
- **Note:** applying underfill material to the components prior to conformal coating application not only prevents the damaging effects on [TMF](#) caused by the conformal coating under the packages, but also enhances the TMF lifetimes of bottom terminated components above their baseline values without conformal coating or underfill.

[Vias](#) in a conformal coating area should be [tent](#)ed, [plugged](#) or [filled](#).

- This prevents the capillary flow of conformal coating material from one side of the PCB to the other that could result in coating unintended areas.
- In addition, this improves the consistency of coating and prevents thinning at the via edge.
- Vias used as test points may not be able to be tented, plugged or filled because that could affect electrical contact.

Specify component damming, underfill and coating materials.

- Material incompatibility can cause fractured solder joints for QFNs, BGAs and LGAs due to stress fatigue.

Specify when plugs are necessary for connectors in conformal coating areas.

- Plugs prevent coating material from coming into contact with leads and preventing electrical connectivity.

Provide a 10.0000mm x 10.0000mm copper area on the conformal coating side of the PCB.

- This area is necessary to get an accurate coating thickness measurement.

For conformal coating dip: do not select components with cavities.

- Component cavities may create flooding when the PCB / panel is flipped.

Ensure all components that will be coated are compatible with conformal coating.

- Components that are not compatible may fail during conformal coating application or during the life of the product.

Avoid applying conformal coating over labels or laser marking.

- Coating over labels or laser marking can make them difficult to read and scan.

## Related Entries

---

[DFM Information 1304 Component Selection > General > Conformal Coating Selection](#)

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## Optical Design Considerations

### Guideline

CID: 3

Content Owner: Jabil

Content Type: Requirement

#### Design Layout:

Ensure optical components with **fibers** are on a separate **PCBA** from electrical components without fibers.

- This allows the optical components to be assembled, **spliced** and tested before adding them to the main assembly.

If optical components must be on the same PCBA as electrical components, ensure all optical components are placed on the opposite side of the PCBA.

- Having the electrical components separate allows for pre-testing to ensure they are known good before adding the expensive optical components for final testing.

Ensure adequate component to component clearance for temperature sensitive optical components to electrical components.

- If adjacent components that are attached with typical solder have to be reworked, the high temperature could cause re-melting of the low temperature solder connections inside the optical component.

Ensure the serial numbers of optical components are scannable and / or human readable after final assembly.

- If there is a test or field failure, the product will require disassembly to check the serial numbers.

Ensure liquid / dispensable materials are not used near optical fibers, optical connectors and seal rings.

- Liquid / dispensable materials like epoxy or thermal grease could contaminate the fibers, connectors and seal rings.

#### Mechanical Considerations:

Ensure optical components not securely soldered to the PCBA are mechanically held in place.

- If optical components are primarily held in place by their fibers, the fibers can be stressed or broken if the components move.

Ensure optical components with thin leads are aligned and mechanically held in place using clamps, brackets, screws, etc. prior to soldering to the PCBA.

- If optical components are held in place by small solder joints, they can be stressed or broken if the components move. If the mechanical attachment occurs after soldering, this can stress the solder joints.

#### Optical Fiber Trays:

Ensure an optical fiber tray is utilized.

- Fibers can be mechanically or thermally damaged during assembly or in the field if they are not protected.

Ensure the design of the optical fiber tray allows for reverse and alternative fiber routing.

- A tray that does not allow for reverse or alternative routing severely limits rework / splicing options. If a shorter fiber cannot be re-routed, the optical component may have to be scrapped.

## Related Entries

---

DFA Guideline [1726 Assembling > Assembling Requirements > Optical Fiber Routing](#)

DFM Rule [1107 Component Selection > General > Optical Fiber Connectors](#)

DFM Guideline [1108 Component Selection > General > Optical Fiber Pigtails](#)

DFM Guideline [1124 Data and Deliverables > General > Optical Requirements in Design Drawings](#)

DFA Rule [1728 Assembling > Assembling Requirements > Optical Fiber Bend Radius](#)

DFA Guideline [1729 Assembling > Assembling Requirements > Optical Fiber Clips](#)

DFM Guideline [1345 Component Selection > General > Self-Adhesive Pads and Optical Fibers](#)

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DFM > PCB Design > General

Entry ID: 1745

## Long SMT Connectors with Dual Alignment Pins

### Guideline

CID: 2

Content Owner: Jabil

Content Type: Requirement

For **SMT** connectors 33.0000mm or longer with dual alignment pins: provide a slotted **NPTH** on one end.

- Very long SMT connectors with dual alignment pins may "pop" during heating due to thermal expansion.

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## Internal Layer Connections for Large PTHs

### Guideline

CID: 2

Content Owner: Jabil

Content Type: Requirement

Ensure large PTHs have internal copper layer connections.

- This is necessary for the mechanical stability / integrity of the barrel wall attachment during PCB copper plating.

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DFM > PCB Design > General

Entry ID: 1839

## PCB Design Practices

### Guideline

CID: 2

Content Owner: Jabil

Content Type: Requirement

Avoid duplicate drill holes of the same size, in the same location.

- Duplicate holes serve no purpose, lengthen the drilling process, and incur extra wear and tear on the drill bit.

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DFM &gt; PCB Design &gt; Test Points

Entry ID: 1034

## Test Points

### Rule

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 2 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Locate all [test points](#) on one side of the [PCB](#).

- Test points on both sides of the PCB increases the cost of the [test fixture](#). If the test points can't all be located on one side, it is acceptable to have some on the other side.

Evenly distribute test points across the entire PCB.

- This can cause localized strain on the PCB.

|         |                      |                           |
|---------|----------------------|---------------------------|
| CID: 26 | Content Owner: Jabil | Content Type: Requirement |
|---------|----------------------|---------------------------|

Minimum center of test point to center of test point spacing = 1.2700mm (0.050")

- Closer spacing requires the use of a more costly probe technology for the test fixture.

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 3 | Content Owner: Jabil | Content Type: Information |
|--------|----------------------|---------------------------|

Maximize the use of larger testpoint to testpoint spacing. This allows the use of larger test probes which are less expensive, more robust, and less prone to wear.

**Note:** Test point spacing is measured from center of test point to center of test point.

| Minimum Test Point to Test Point Spacing                      | Specification  | Cost     |
|---|--|----------|
|   | Preferred - Layout all test points with 0.085" (2.1600mm) spacing.                                       | \$       |
|   | Alternate 1 - Layout mostly 0.085" (2.1600mm) spacing with some 0.070" (1.7800mm).                       | \$       |
|   | Alternate 2 - Layout mostly 0.085" (2.1600mm) spacing with some 0.070" (1.7800mm) and 0.050" (1.2700mm). | \$\$     |
|   | Alternate 3 - Minimum number of 0.039" (1.0000mm) spacing.   | \$\$\$   |
| Requires fine pitch fixturing ( <a href="#">X-Probe X31</a> ) | Alternate 4 - Minimum number of 0.030" (0.7620mm) spacing.   | \$\$\$\$ |

**Note:** Dollar signs indicate cost and variable cost increase, not a multiplier.

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 4 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Provide [test pads](#) for all test points.

- Test pads provide the most stable and repeatable surface for good electrical contact. Alternatively, utilize [vias](#) or [TH leads](#) (least desirable).

See [Entry 1086](#) for details on TH leads used as test points.

|         |                      |                           |
|---------|----------------------|---------------------------|
| CID: 28 | Content Owner: Jabil | Content Type: Requirement |
|---------|----------------------|---------------------------|

Minimum test point diameter = 0.7620mm (0.030")

- Smaller test points may exceed available test fixture technology.

CID: 5 Content Owner: Jabil Content Type: Information

If the minimum test point diameter requirement cannot be met, below are options that have increasingly more expensive technology that is not generally used unless unavoidable.

Within this table, test points with a diameter of 0.040" (1.0160mm) provide the most reliable and repeatable contact. Use of test points below 0.035" (0.8890mm) may require specialized tooling resulting in additional fixture costs.

| Test Point Diameter | Center to Center Spacing   | Recommended Fixture Type | Cost Impact |
|---------------------|--|--------------------------|-------------|
| 0.040" (1.0160mm)   | 0.085" (2.1590mm)<br>0.070" (1.7780mm)<br>0.050" (1.2700mm)                      | Standard                 | \$          |
| 0.035" (0.8890mm)   | 0.085" (2.1590mm)<br>0.070" (1.7780mm)<br>0.050" (1.2700mm)                      | Standard                 | \$          |
| 0.030" (0.7620mm)   | 0.085" (2.1590mm)<br>0.070" (1.7780mm)<br>0.050" (1.2700mm)                      | Guided Probe             | \$\$        |
| 0.025" (0.6350mm)   | 0.085" (2.1590mm)<br>0.070" (1.7780mm)<br>0.050" (1.2700mm)<br>0.039" (0.9906mm) | Guided X-Probe           | \$\$\$      |

**Note:** Dollar signs indicate cost and variable cost increase, not a multiplier.

CID: 25 Content Owner: Jabil Content Type: Requirement

Ensure [soldermask](#) is not present on test point pads.

- Soldermask on a test point pad could prevent good electrical contact.

CID: 37 Content Owner: Jabil Content Type: Requirement

If the PCB surface finish is [OSP](#) or immersion tin, ensure [solderpaste](#) is printed on the pads of test points.

- The test probes will have better electrical contact if solderpaste is applied to these surface finishes. Other surface finishes do not require solderpaste on the test points.

CID: 30 Content Owner: Jabil Content Type: Requirement

Minimum clearance from edge of test point to conveyed PCB edge on [primary](#) and [secondary](#) sides = 5.0000mm

- This can cause issues with printing solderpaste on the test points.

**Note:** Use of automated PCB handlers in test may require more clearance depending on the equipment used.

CID: 31 Content Owner: Jabil Content Type: Requirement

Minimum clearance from edge of test point to [non-conveyed PCB edge](#) on primary and secondary sides = 1.2500mm

- This can cause interference with the test equipment preventing test point access.

**Note:** Use of automated PCB handlers in test may require more clearance depending on the equipment used.

CID: 32

Content Owner: Jabil

Content Type: Requirement

Minimum edge of test point to edge of [NPTH](#) spacing on primary and secondary sides = 1.2500mm

- This can cause interference with the test equipment preventing test point access.

## Related Entries

---

DFA Guideline [1410 Flex / ACF Bonding > Flex / ACF Bonding Requirements > FPC Testability](#)

DFM Rule [1136 PCB Design > Test Points > Test Point to Component Spacing](#)

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DFM > PCB Design > Test Points

Entry ID: 1136

## Test Point to Component Spacing

### Rule

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 5 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Spacing requirements ensure [test points](#) are accessible and are not interfered with by component placement variation. If the spacing is less than specified, test contact issues, damaged components or damage to the test fixture could result.

| Component Height                     | Test Point Center to Edge of Component Body |
|--------------------------------------|---|
| Less than 1.5250mm                   | 0.4750mm                                    |
| 1.5250mm up to 2.5400mm              | 0.4750mm                                    |
| Greater than 2.5400mm up to 7.6200mm | 0.8500mm                                    |
| Greater than 7.6200mm                | 2.4500mm                                    |

In [wave solder](#) areas, minimum spacing from test point edge to edge of component pad = 1.1500mm

- If test points are too close to component pads, solder bridging may occur.

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 6 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Ensure test points are not obstructed by components.

- Test points obstructed by components would prevent testing.

### Related Entries

[DFM Rule 1034](#) PCB Design > Test Points > Test Points

[DFM Rule 1075](#) PCB Design > General > Tooling Holes

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## Test Points Under Large SMT Components

### Guideline

CID: 3

Content Owner: Jabil

Content Type: Requirement

Test points placed on the opposite side from large **SMT** components should be kept to a minimum.

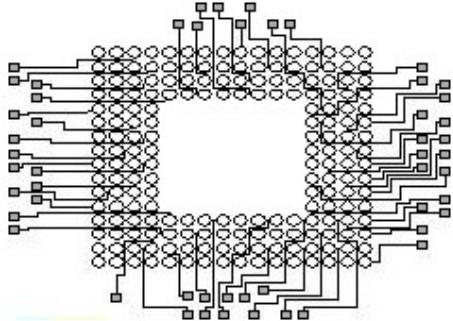
The definition of a large SMT devices is any device that is 729 square millimeters or larger.

For PCBs less than 1.9000mm thick: maximum 100 test points per 645 square millimeters on the opposite side from SMT components 729 square millimeters or larger.

For PCBs between 1.9000mm and 5.0000mm thick: maximum 150 test points per 645 square millimeters on the opposite side from SMT components 729 square millimeters or larger.

- Exceeding the probe density guideline can result in physical damage to the product due to stress.
- Test points can be moved outside the component perimeter, routed outside the component perimeter or placed on both sides of the PCB to mitigate the strain on these components.

**Note:** These limitations do not apply to PCBs thicker than 5.0000mm.



### Related Entries

DFM Rule [1034](#) PCB Design > Test Points > Test Points

DFM Rule [1136](#) PCB Design > Test Points > Test Point to Component Spacing

## Solid Tab Depaneling

### Rule

CID: 3

Content Owner: Jabil

Content Type: Requirement

For solid tab depaneling:

Minimum solid tab width for routing = 1.2000mm

- A narrower tab may break and cause issues during manufacturing.

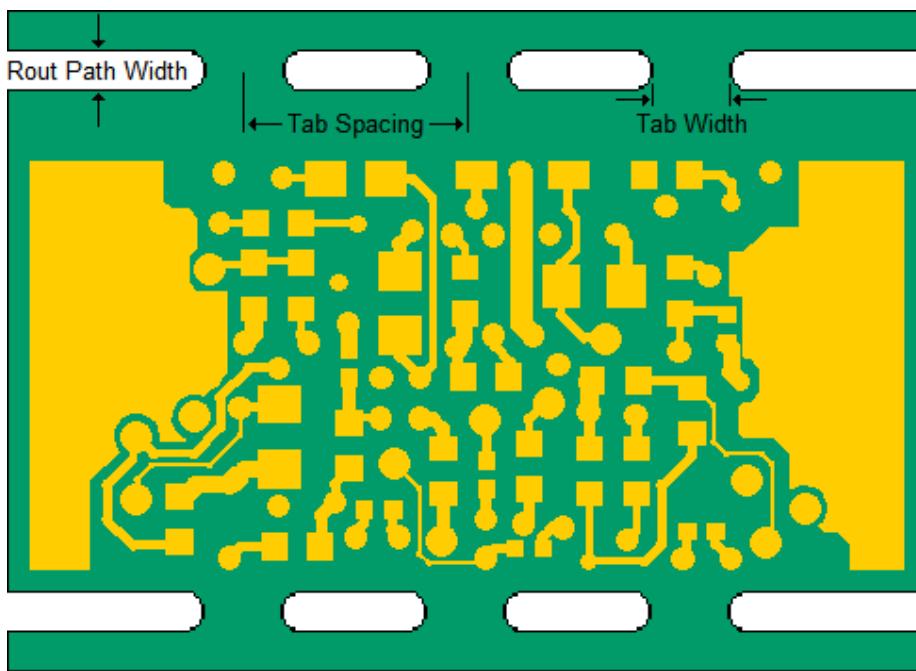
Solid tab rout path width = 1.2000mm to 2.4000mm

- Too narrow may not provide enough space for the router bit to travel between the PCBs, too wide and the router may not be able to remove all of the tab material between the PCBs.

Maximum center to center tab spacing = 60.0000mm

There must be a tab within 20.0000mm of all corners.

- Greater spacing may allow the joints to flex too much or prematurely break during manufacturing.



For dust sensitive components, do not select the solid tab depaneling process.

- Components like switches, connectors, microphones etc. can be damaged by the dust created during the routing process.

**Note:** Key Points to consider in choosing solid tab routing panelization:

- Joint strength using solid tab routing is stronger than V-score and drilled breakaway (mouse bite) depaneling.

- Solid tab routing causes significantly less strain on nearby components than other depaneling methods.
- Depanelization may only be performed with a machine, either a high speed automated router or shearing machine.
- Routed areas are smooth, leaving 0.1250mm of material residue.

## Related Entries

---

DFM Rule [1038](#) PCB Design > Depanel > Drilled Breakaway (Mouse Bite) Depaneling

DFM Rule [1043](#) PCB Design > Depanel > Scored Breakaway (V-Score) Depaneling

DFM Rule [1156](#) PCB Design > Keep-out > Copper to PCB Edge and NPTH Keep-Outs

DFM Rule [1321](#) Component Placement > Location > Component to Solid Tab PCB Edge Clearance

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DFM > PCB Design > Depanel

Entry ID: 1038

## Drilled Breakaway (Mouse Bite) Depaneling

### Rule

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 3 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Avoid using [drilled breakaway \(mousebite\) depaneling](#).

- This can be the weakest, and is the least preferred depaneling option. [Solid tab depaneling \(routing\)](#) causes significantly less strain on nearby components and is the recommended depaneling option.

Drilled breakaway (mousebite) tab width = 5.0000mm

- Narrower tabs may prematurely break during manufacturing.

Drilled breakaway (mousebite) tab rout path width = 1.6000mm (preferred) or up to 3.2000mm

- Non-standard widths may cause poor joint strength or issues during PCB fabrication.

Maximum center to center drilled breakaway (mousebite) tab spacing = 50.0000mm

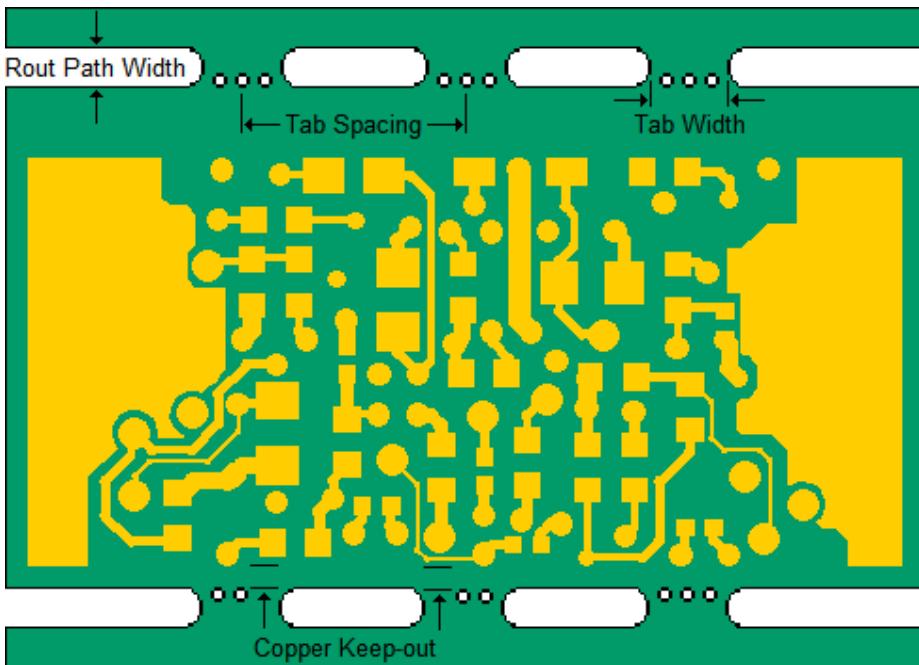
- This may allow the joints to flex too much or prematurely break during manufacturing.

Ensure a drilled breakaway (mousebite) tab is within 12.5000mm of all corners.

- This may allow the joints to flex too much or prematurely break during manufacturing.

For each drilled breakaway (mousebite) tab: minimum clearance from recessed NPTH drill holes to inner and outer layer PCB copper features = 1.2500mm

- A minimum clearance is necessary to avoid damaging copper features on the PCB.



#### **Drilled breakaway tab layout requirements:**

If [tooling holes](#) are located in the drilled breakaway (mousebite) rail, minimum rail width = 7.0000mm

- Enough material needs to be provided on both sides of the tooling hole to adequately support the PCB during manufacturing. If a narrower rail width is necessary to reduce PCB cost, an agreement with the customer to ensure there won't be a negative impact to manufacturability / yield is recommended.

If tooling holes are located in the drilled breakaway (mousebite) rail, minimum distance from center of tooling hole to rail outer edge = 5.0000mm

- This spacing is based on legacy equipment and conveyor tooling pin specifications, and may prevent issues during PCB fabrication and manufacturing.

If tooling holes are located in the drilled breakaway (mousebite) rail, minimum distance from inner edge of tooling hole to rail inner edge = 1.5000mm

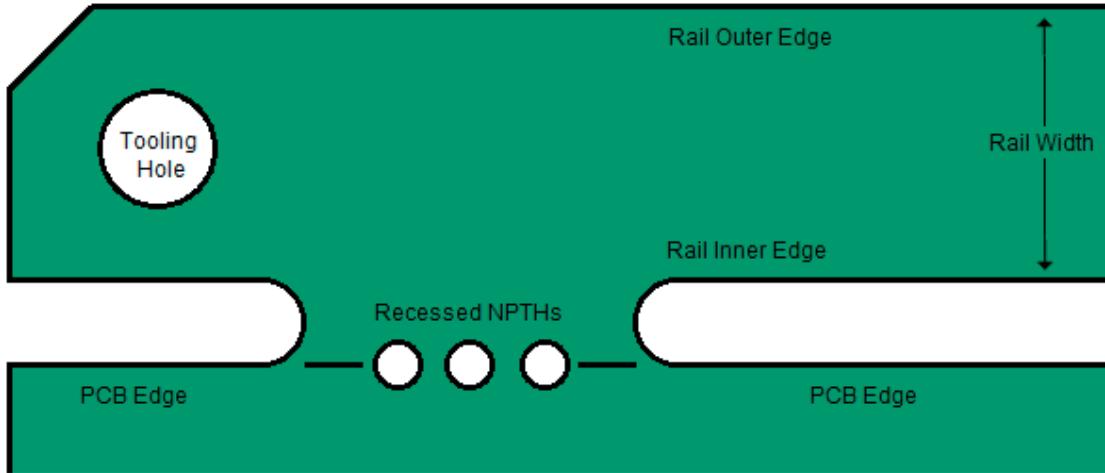
- Enough material is needed to prevent breakout of the tooling hole during PCB fabrication.

If the drilled breakaway (mousebite) rail does not contain tooling holes, minimum rail width = 5.0000mm

- Enough material needs to be provided to adequately support the PCB during manufacturing.

For each drilled breakaway (mousebite) tab: provide three 0.8000mm diameter recessed [NPTH](#) drill holes, center of holes in line with the PCB edge, spaced 1.2500mm center to center.

- This provides the most reliable separation during the depopulation process, and the least stress on the PCB and adjoining components.



#### Key points to consider in choosing drilled breakaway depanelization:

- Should not be used on PCBs thicker than 2.3000mm.
- Joint strength using drilled breakaway is weaker than [V-Score](#) and solid tabs.
- Depanelization can be manual (hand break, nibblers) or done with a router (preferred).
- Routing causes significantly less strain on nearby components than a manual depanelization method.
- Routed areas are smooth with some exposed fiber at tabs, leaving ~ +/-0.1250mm of material residue.

#### Related Entries

---

[DFM Rule 1035](#) PCB Design > Depanel > Solid Tab Depaneling

[DFM Rule 1043](#) PCB Design > Depanel > Scored Breakaway (V-Score) Depaneling

[DFM Rule 1156](#) PCB Design > Keep-out > Copper to PCB Edge and NPTH Keep-Outs

[DFM Rule 1320](#) Component Placement > Location > Component to Drilled Breakaway (Mouse Bite) PCB Edge Clearance

[DFM Rule 1075](#) PCB Design > General > Tooling Holes

DFM > PCB Design > Depanel

Entry ID: 1043

## Scored Breakaway (V-Score) Depaneling

### Rule

CID: 3

Content Owner: Jabil

Content Type: Requirement

#### Observe requirements when using the V-score depaneling method:

V-score technology is limited to PCBs between 0.8000mm and 2.4000mm thick.

- If the PCB is too thin, it may sag causing issues in manufacturing or if it is too thick it may be hard to separate and / or experience excessive stress.

Specify in the fab drawing that V-score angle = less than 60 degrees

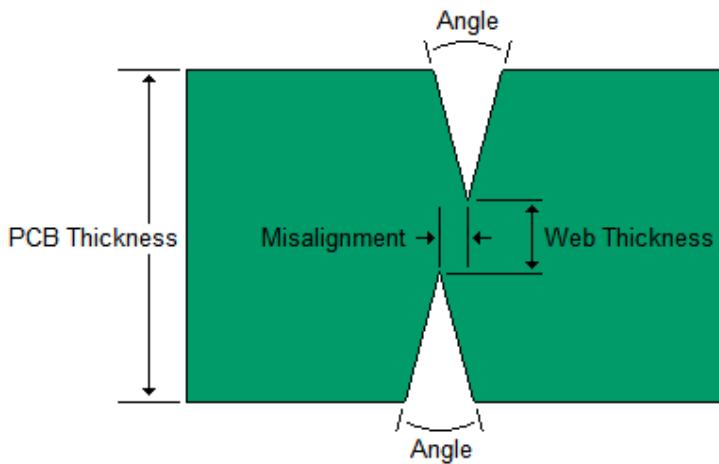
- A poor V-score angle may cause additional stress on the PCB during depaneling and should be validated on the actual design.

Specify in the fab drawing that the maximum V-score top to bottom misalignment = 0.1500mm

- Poor alignment may cause issues during the separation process.

Specify in the fab drawing that V-score web thickness = 0.6000mm with a tolerance of plus or minus 0.1000mm

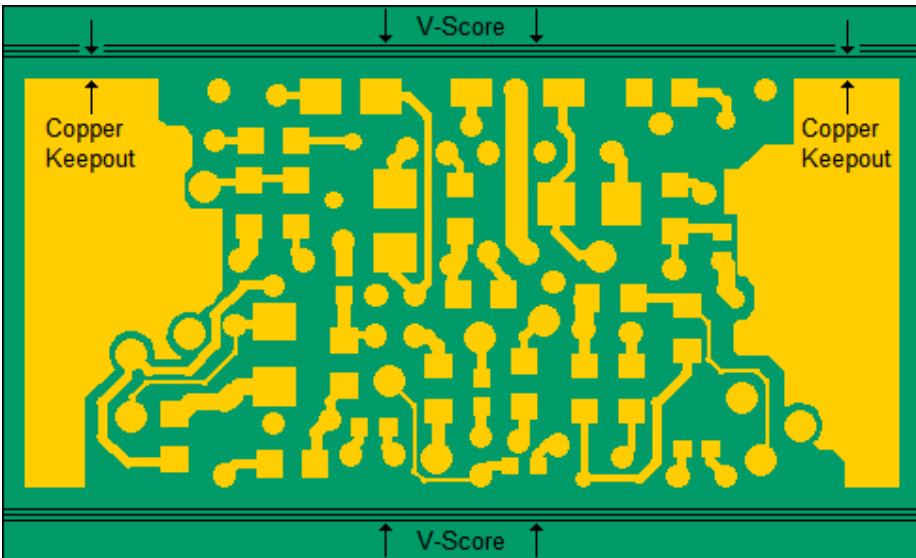
- A web that is too thick may make the PCB difficult to separate and if too thin it may prematurely break.



Specify in the fab drawing that minimum copper to V-score edge keep-out, excluding component pads = 0.6350mm

- This may expose or damage copper during the separation process.

See [Entry 1319](#) for component pad spacing.



#### Key points to consider in choosing V-score panelization:

- Joint strength using V-score is weaker than solid tab routing and may be more susceptible to handling issues.
- Depanelization may be performed manually or with a machine.
- Scoring provides a uniform but slightly rough edge, leaving ~ 0.1250mm to 0.2500mm of residual material.
- PCBs may be placed adjacent to each other in the panel.
- Solid tab routing causes significantly less strain on nearby components than V-score depaneling.

#### Related Entries

---

DFM Rule [1035](#) PCB Design > Depanel > Solid Tab Depaneling

DFM Rule [1038](#) PCB Design > Depanel > Drilled Breakaway (Mouse Bite) Depaneling

DFM Rule [1156](#) PCB Design > Keep-out > Copper to PCB Edge and NPTH Keep-Outs

DFM Rule [1319](#) Component Placement > Location > Component to Scored Breakaway (V-Score) PCB Edge Clearance

DFM > PCB Design > Depanel

Entry ID: 1736

## Punching Depanel

### Guideline

CID: 2

Content Owner: Jabil

Content Type: Requirement

For punching **depanel**: minimum clearance from center of punching pins to adjacent exposed metal surfaces on both sides of the **PCB** = 7.0000mm

- The pin support tooling may scratch the PCB surface.

For punching depanel: minimum clearance from center of punching pins to adjacent component bodies or pads on both sides of the **PCB** = 7.0000mm

- The component could be damaged and / or the punching process may not be possible.

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DFM > PCB Design > Keep-out

Entry ID: 1156

## Copper to PCB Edge and NPTH Keep-Outs

### Rule

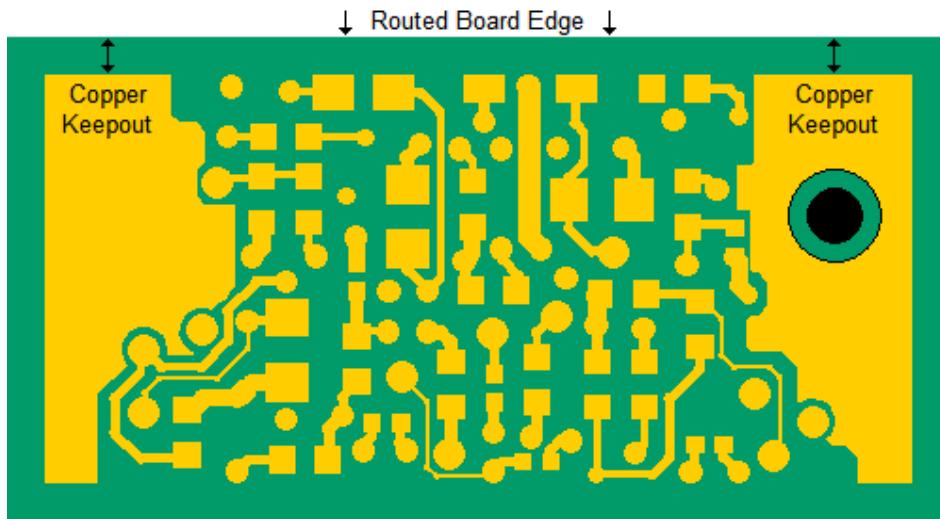
CID: 6

Content Owner: Jabil

Content Type: Requirement

Minimum distance from copper features to the routed PCB edge = 0.5000mm

- This may damage or expose copper features during the routing process.



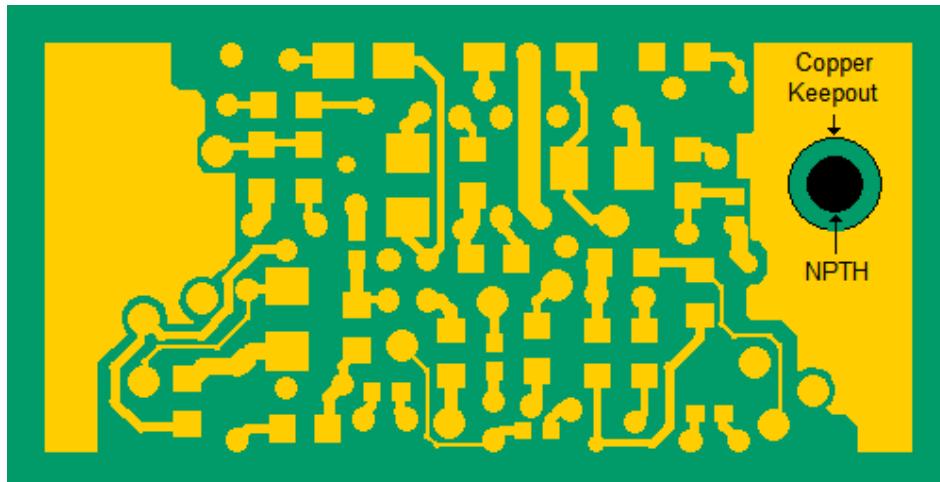
CID: 7

Content Owner: Jabil

Content Type: Requirement

Minimum distance from copper features to NPTH edge = 0.2500mm

- This may damage or expose copper features during the drill process.



### Related Entries

DFM Rule [1035](#) PCB Design > Depanel > Solid Tab Depaneling

DFM Rule [1038](#) PCB Design > Depanel > Drilled Breakaway (Mouse Bite) Depaneling



DFM > PCB Design > Keep-out

Entry ID: 1742

## Scannable Label Location

### Guideline

CID: 2

Content Owner: Jabil

Content Type: Requirement

Observe location and [keep-outs](#) for scannable labels / markings.

- Labels / markings that are obscured can't be automatically scanned and will slow down manufacturing.
- Labels / markings on the bottom of the [PCB](#) can't be automatically scanned at [ICT](#).
- A solid surrounding copper keep-out area for laser engraved markings is necessary for scanning.

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DFM > PCB Design > Keep-out

Entry ID: 1744

## Gold Finger Clearance

### Guideline

CID: 2

Content Owner: Jabil

Content Type: Requirement

Minimum clearance from edge of gold finger to edge of solderable surface = 2.0000mm

- Minimum clearance is necessary to avoid getting solder on the gold fingers.

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DFM > PCB Design > Keep-out

Entry ID: 1747

## Connector Ejector Tab Clearance

### Guideline

CID: 2

Content Owner: Jabil

Content Type: Requirement

Provide adequate clearance for connector ejector tabs.

- It may be difficult or impossible to remove connectors if adequate clearance is not available.

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DFM > PCB Design > Keep-out

Entry ID: 1748

## Heat Sink Clearance

### Guideline

CID: 2

Content Owner: Jabil

Content Type: Requirement

Provide adequate clearance for [heat sinks](#).

- Heat sinks have a variety of clearance issues that could make assembly difficult or impossible.

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DFM > PCB Design > Padstacks

Entry ID: 1040

## Fiducials

### Rule

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 4 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Ensure **fiducials** are solid copper filled and circular.

- Non-circular or partially filled fiducials can cause reflections that distort the outline preventing proper optical alignment of the PCB in the assembly equipment.

|         |                      |                           |
|---------|----------------------|---------------------------|
| CID: 26 | Content Owner: Jabil | Content Type: Requirement |
|---------|----------------------|---------------------------|

Ensure fiducial diameter = 1.0000mm

- Non-standard fiducials may require additional setup / programming time. Fiducials between 0.8000mm and 2.0000mm in diameter are acceptable but less preferred.

|         |                      |                           |
|---------|----------------------|---------------------------|
| CID: 17 | Content Owner: Jabil | Content Type: Requirement |
|---------|----------------------|---------------------------|

Ensure component bodies do not partially or fully cover fiducials.

- An obscured fiducial could prevent downstream processes from utilizing it.

|         |                      |                           |
|---------|----------------------|---------------------------|
| CID: 27 | Content Owner: Jabil | Content Type: Requirement |
|---------|----------------------|---------------------------|

Minimum clearance from edge of fiducial to edge of component bodies = 0.6500mm

- Insufficient component body clearance can distort recognition of the fiducial.

|         |                      |                           |
|---------|----------------------|---------------------------|
| CID: 28 | Content Owner: Jabil | Content Type: Requirement |
|---------|----------------------|---------------------------|

Minimum clearance from edge of fiducial to edge of **soldermask** and **silkscreen** = 0.5000mm

Minimum clearance from edge of fiducial to edge of **copper** on the same layer = 0.6250mm

- Insufficient clearance can distort recognition of the fiducial.

Minimum clearance from edge of fiducial to edge of copper on the layer below the fiducial = 0.50000mm

- Insufficient copper clearance on the layer below the fiducial can distort recognition of the fiducial.

|         |                      |                           |
|---------|----------------------|---------------------------|
| CID: 18 | Content Owner: Jabil | Content Type: Requirement |
|---------|----------------------|---------------------------|

For single PCBs: on each **SMT** side, the minimum number of fiducials = 3

- This could cause inaccurate placement, 2 fiducials are acceptable as a bare minimum but not preferred.

CID: 6

Content Owner: Jabil

Content Type: Requirement

For single PCBs: fiducials must be located in diagonally opposed corners and the third fiducial must be located perpendicular to the other two.

- This could cause inaccurate placement.

For single PCBs: locate fiducials at different distances from their respective corners.

- This could allow the PCB to be placed in the equipment backwards.

CID: 33

Content Owner: Jabil

Content Type: Requirement

For panels: on each [SMT](#) side, the minimum number of fiducials = 3

- This could cause inaccurate placement, 2 fiducials are acceptable as a bare minimum but not preferred.

For panels: fiducials must be located in diagonally opposed corners and the third fiducial must be located perpendicular to the other two.

- This could cause inaccurate placement.

For panels: locate fiducials at different distances from their respective corners.

- This could allow the panel to be placed in the equipment backwards.

CID: 31

Content Owner: Jabil

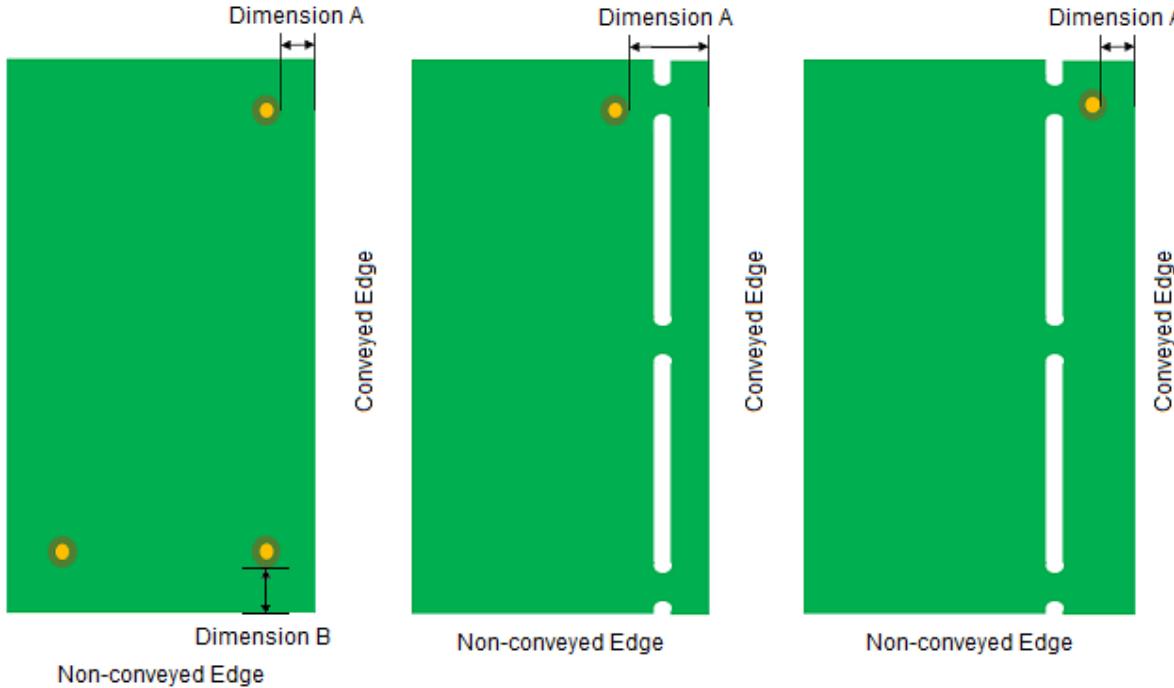
Content Type: Requirement

Minimum clearance from edge of fiducial to conveyed edge of PCB (Dimension A) = 5.0000mm

- This could distort recognition of the fiducial.
- If the PCB has rails on the conveyed edge, 5.0000mm from edge of fiducial to outer edge of rail (Dimension A) is required. When the fiducials are on the rail, the conveyed edge spacing of 5.0000mm (Dimension A) applies.

Minimum clearance from edge of fiducial to non-conveyed edge of PCB (Dimension B) = 1.5000mm

- This could distort recognition of the fiducial.
- Fiducials 1.5000mm (Dimension B) from non-conveyed edge may limit the option to rotate the PCB during the assembly process.



CID: 29

Content Owner: Jabil

Content Type: Requirement

All components with a pitch greater than 0.5000mm must be within 125.0000mm of the nearest fiducial.

- This could cause inaccurate placement.

All components with a pitch less than or equal to 0.5000mm must be within 50.0000mm of the nearest fiducial.

- Fine pitch components require fiducials close by or it could cause inaccurate placement.

CID: 30

Content Owner: Jabil

Content Type: Requirement

Minimum [keep-out](#) from edge of soldermask defined area of fiducials to edge of [NPTH](#) or [PTH](#) pad edge = 3.5000mm

- Features inside the keep-out area can distort recognition of the fiducial.

CID: 32

Content Owner: Jabil

Content Type: Requirement

Minimum clearance between edge of fiducials and edge of like pads = 3.5000mm

- This could cause the vision system to incorrectly register the feature as a fiducial causing misalignment.
- Like pads are defined as any feature of the same shape within +/-10% of the fiducial size.

DFM > PCB Design > Silkscreen

Entry ID: 1044

## Silkscreen

### Rule

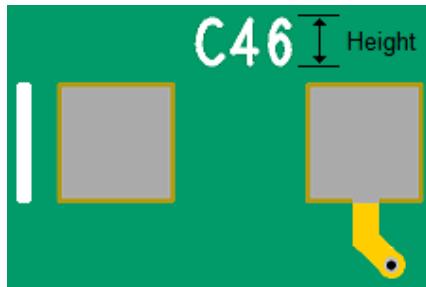
CID: 26

Content Owner: Jabil

Content Type: Requirement

Minimum silkscreen text height = 1.0000mm

- This is considered to be the smallest human readable text size.



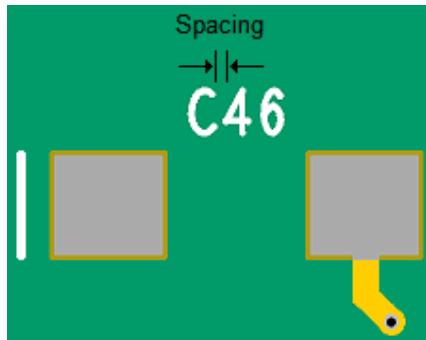
CID: 27

Content Owner: Jabil

Content Type: Requirement

Minimum silkscreen text spacing = 0.1500mm

- This is considered necessary for it to be human readable text.



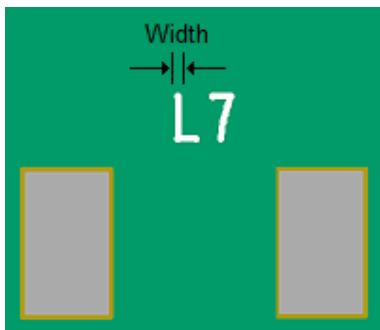
CID: 28

Content Owner: Jabil

Content Type: Requirement

Minimum silkscreen line width = 0.1500mm

- This can cause gaps or issues with visibility on the manufacturing floor.



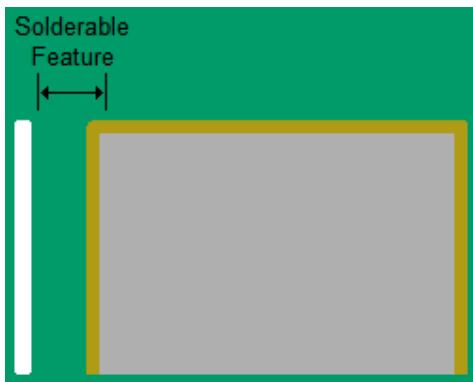
CID: 30

Content Owner: Jabil

Content Type: Requirement

Minimum clearance from silkscreen to solderable features = 0.2250mm

- Inadequate clearance may cause disturbed solder joints if the silkscreen is touching the solderable feature. Inadequate clearance to SMT component pads may cause a [solderpaste](#) stencil standoff issue, resulting in poor solderpaste print definition.



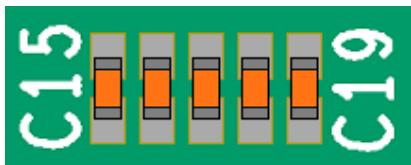
CID: 18

Content Owner: Jabil

Content Type: Requirement

Silkscreen reference designators must be near their components.

- This can cause issues with test debug, repair, and inspection.
- If components are in a row and in sequence, it is acceptable to label the first and last only.



CID: 16

Content Owner: Jabil

Content Type: Requirement

All silkscreen reference designators must be visible after assembly.

- This can cause issues with test debug, repair and inspection.

CID: 7

Content Owner: Jabil

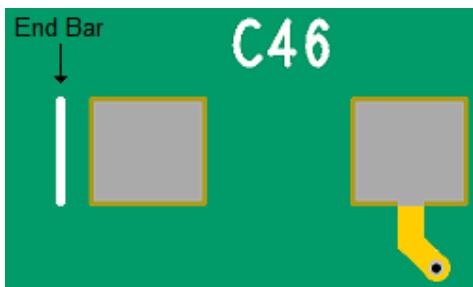
Content Type: Requirement

All silkscreen polarity and orientation markings must be visible after assembly.

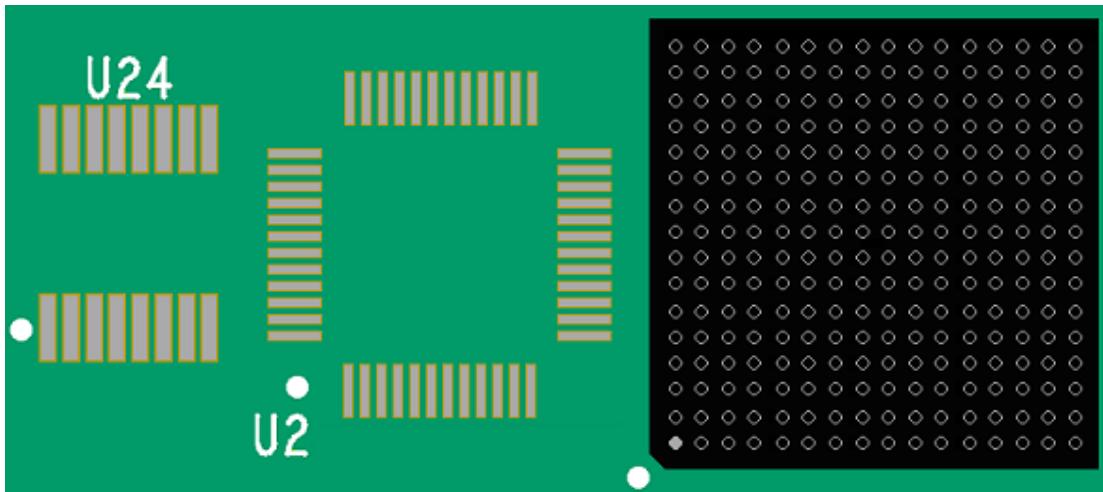
- This can cause issues with test debug, repair, inspection and solderpaste printing.

Diodes - silkscreen an "A" at the anode and a "C" at the cathode.

Other discretes - use an end bar to match the component marking.



Leaded on 2 sides, 4 sides, ICs, QFNs, BGAs, etc. - use a dot.



CID: 34

Content Owner: Jabil

Content Type: Requirement

Indicate component orientation in silkscreen for all polarity and orientation sensitive devices with minimally sized polarity markings:

- This can cause issues with test debug, repair, inspection and solderpaste printing.
- If silkscreen is not possible, indicating polarity with copper features is acceptable.

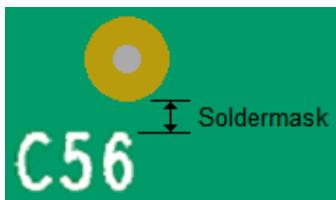
CID: 33

Content Owner: Jabil

Content Type: Requirement

Minimum clearance from silkscreen to the edge of soldermask openings = 0.1500mm

- This could cause the silkscreen to get cut off, making it unreadable.



CID: 10

Content Owner: Jabil

Content Type: Requirement

Do not place silkscreen over covered or plugged vias that are underneath components.

- This can affect the component coplanarity.

CID: 11

Content Owner: Jabil

Content Type: Requirement

Do not place silkscreen under the bodies of SMT components.

- This can cause solderpaste stencil standoff issues resulting in solder opens and bridging.

CID: 35

Content Owner: Jabil

Content Type: Requirement

Indicate label size and placement in silkscreen.

- Not having a clear location can lead to inconsistent placement.

## Related Entries

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DFM Information [1423 PCB Design > General > FAB Notes](#)

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DFM > PCB Design > Soldermask

Entry ID: 1032

## Soldermask

### Rule

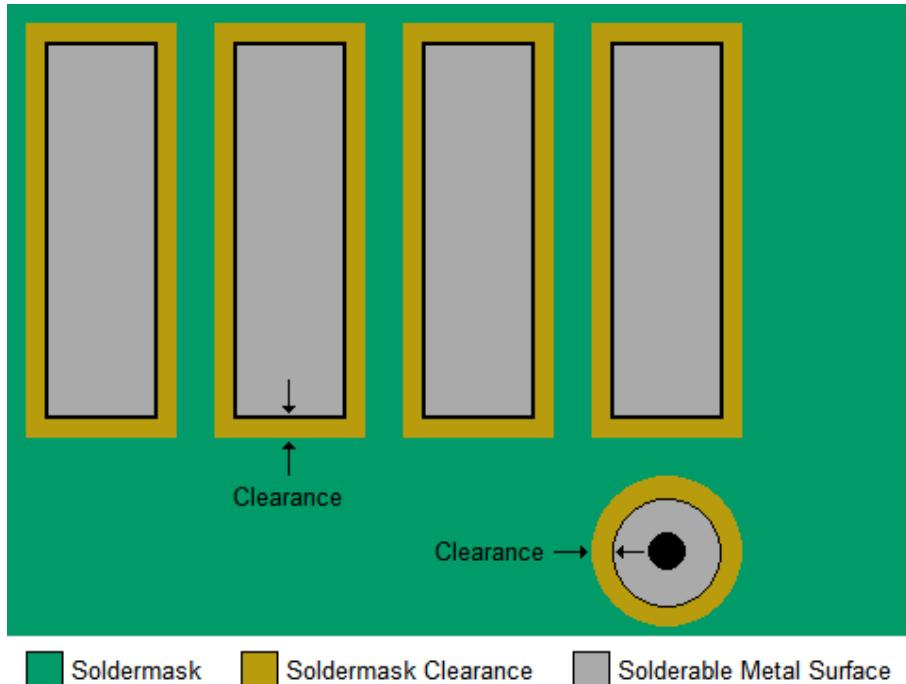
CID: 6

Content Owner: Jabil

Content Type: Requirement

Minimum soldermask clearance to solderable metal surfaces = 0.0750mm

- Soldermask registration requirements from the vendors are typically +/- 0.0750mm and would interfere with solder joint formation if mask is present on the pads.



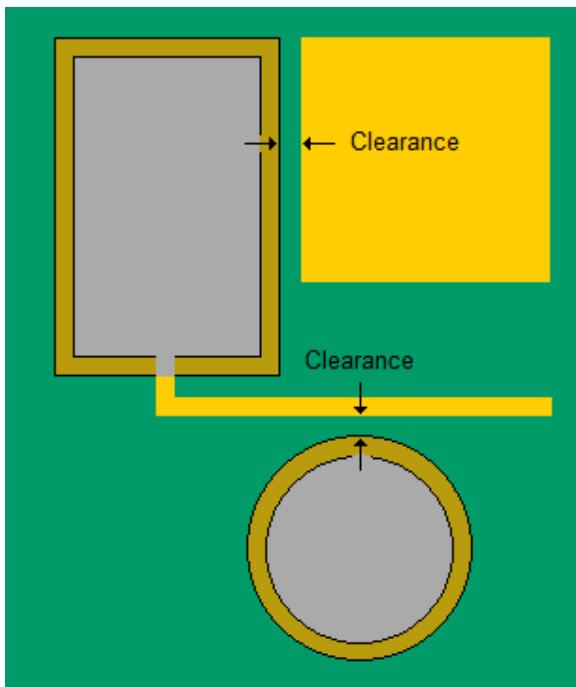
CID: 8

Content Owner: Jabil

Content Type: Requirement

Maintain a minimum clearance of 0.0750mm from covered copper features to soldermask openings.

- Soldermask registration requirements from the vendors are typically +/- 0.0750mm and could expose the adjacent covered copper.



Soldermask  
Soldermask Opening  
Exposed Copper  
Covered Copper

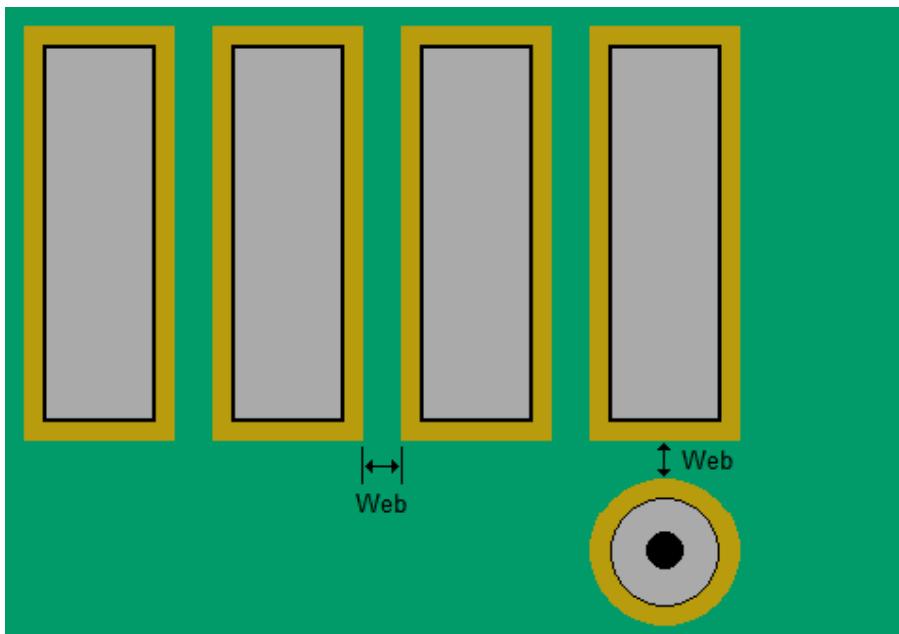
CID: 10

Content Owner: Jabil

Content Type: Requirement

Minimum [soldermask web](#) width = 0.1000mm. Requirement applies to all soldermask features.

- The soldermask must be thick enough to prevent bridging between solderable features.



Soldermask  
Soldermask Clearance  
Solderable Metal Surface

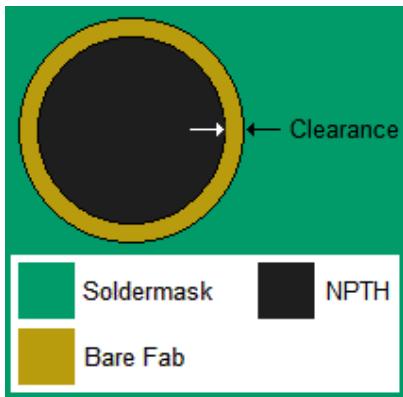
CID: 12

Content Owner: Jabil

Content Type: Requirement

Minimum [NPTH soldermask](#) clearance = 0.0750mm

- Clearance is needed to avoid soldermask encroaching on the hole.



CID: 14

Content Owner: Jabil

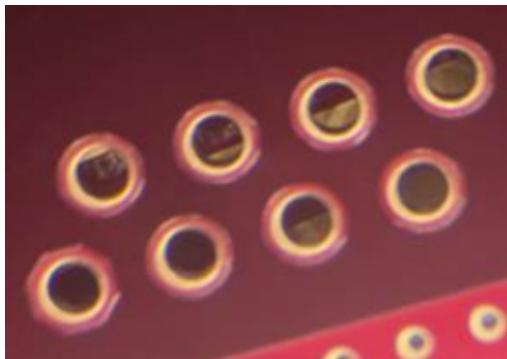
Content Type: Requirement

**PSM** is the intentional reduction in the solder-side, **soldermask** opening on a **PTH** annular ring to help reduce and / or eliminate solder bridging in the **wave** and **selective** soldering processes. Whereas the soldermask opening is typically larger than the annular ring (resulting in a copper defined **fillet**), it now covers up most of the PTH annular ring resulting in a soldermask defined solderable area / fillet.

All **PCB** vendors that Jabil uses should be able to meet a +/- 0.0750mm soldermask to drill registration specification. It should be noted that the copper design of the board is not changed in any way causing minimal work for the designer to make the change, therefore the change can easily be implemented on an assembly already in production.

If PSM is utilized: the recommended soldermask opening centered around the PTH holes is the **FHS + 0.2000mm**

- A soldermask opening that is too small may allow the soldermask to encroach into the hole preventing a good solder joint. An opening that is too large both increases the solder volume and reduces the copper to copper spacing, increasing the chances of bridging.



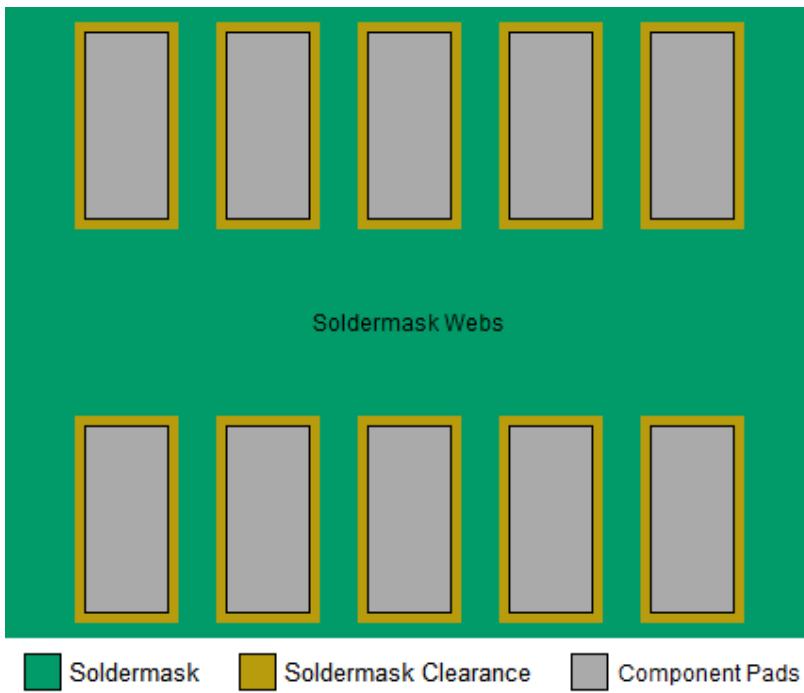
CID: 16

Content Owner: Jabil

Content Type: Requirement

**SMT** components with a **pitch** of 0.5000mm or greater should have a soldermask web between adjacent component pads.

- A soldermask web between the pads can be reliably produced by PCB suppliers and can benefit manufacturing by making solder bridging less likely.



Soldermask      Soldermask Clearance      Component Pads

## Related Entries

---

DFM Guideline 1039 Component Land Pattern > General > Selective and Wave Soldered THMT Component Pads

DFM Rule 1314 Component Land Pattern > General > Selective and Wave Soldered THMT Component Hole Size

DFM Rule 1076 PCB Design > General > Thermal Reliefs

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DFM > PCB Design > Soldermask

Entry ID: 1395

## Soldermask Alignment for Fine Pitch Components

### Information

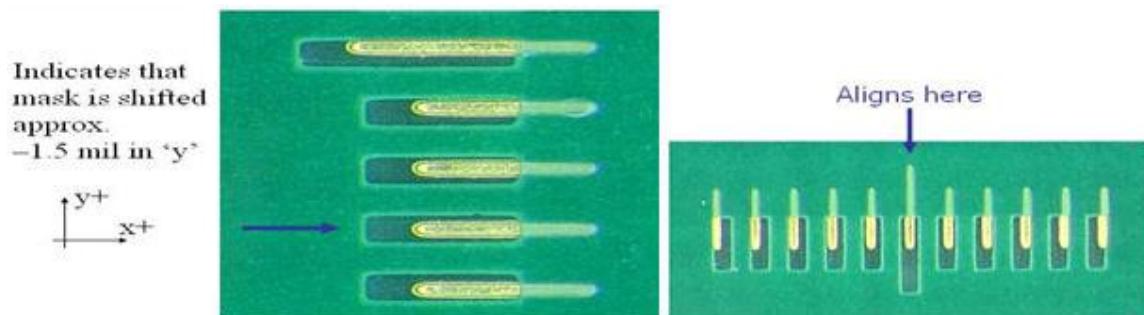
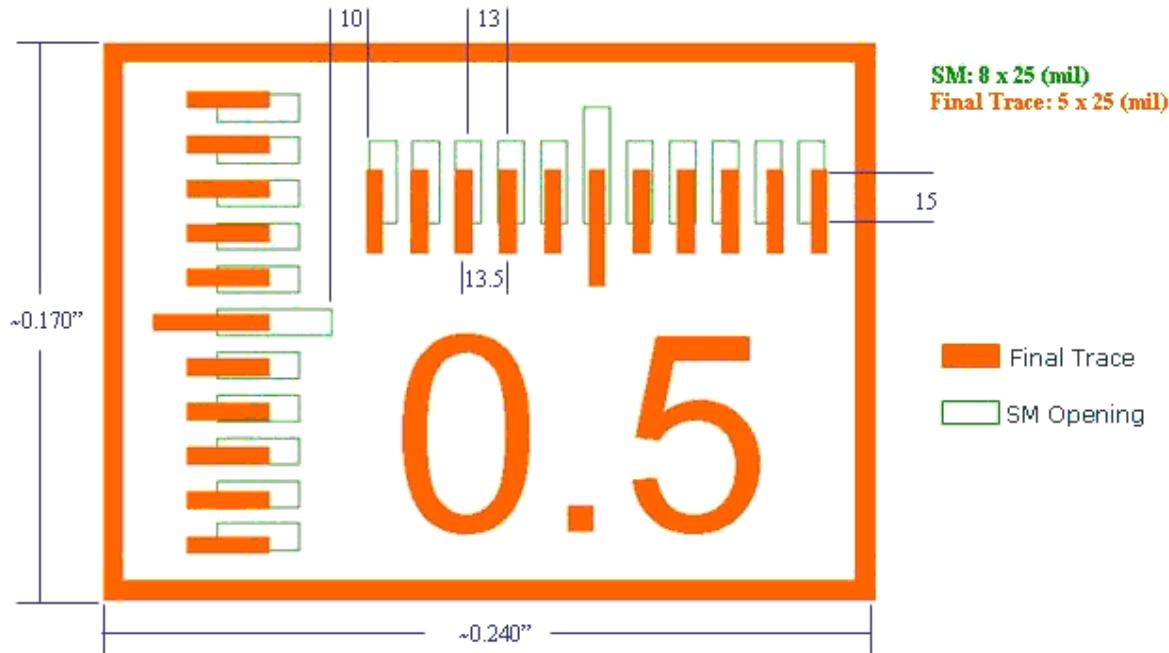
CID: 1

Content Owner: Jabil

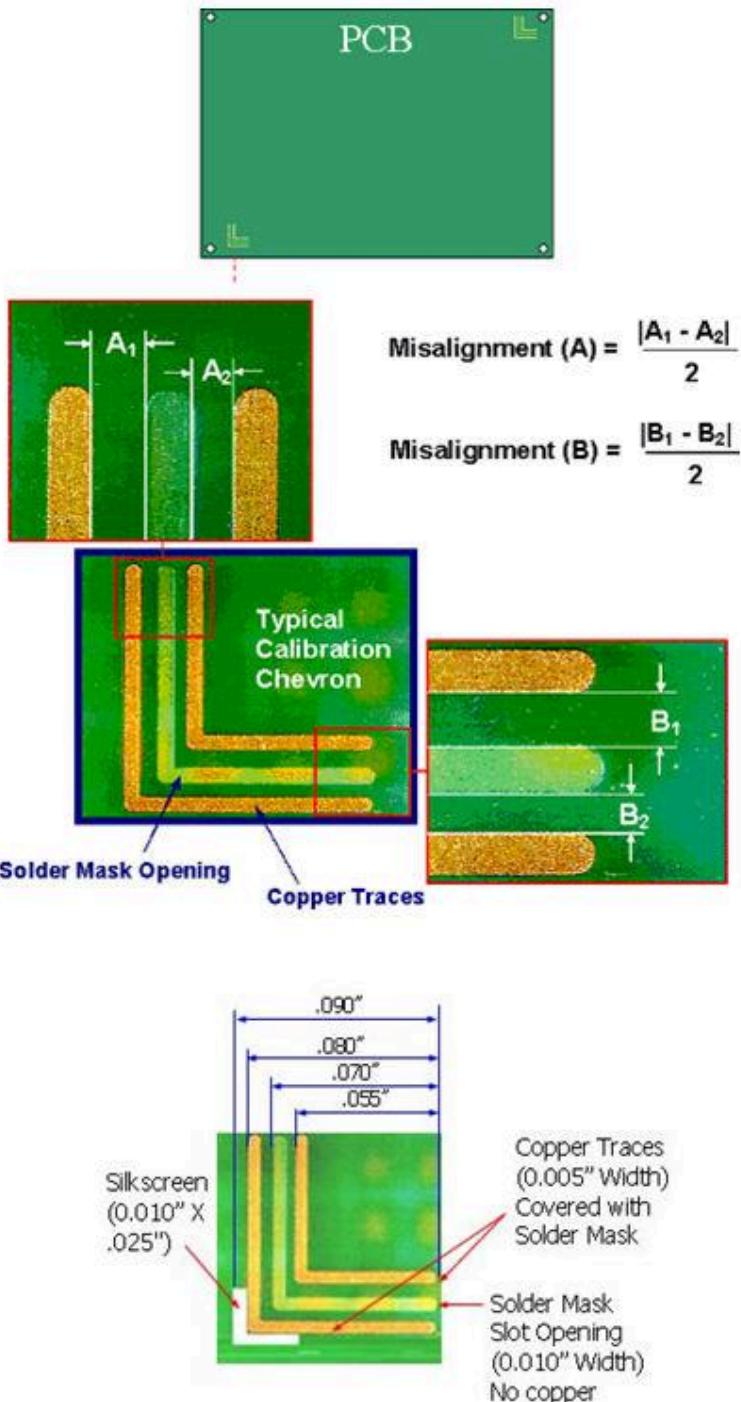
Content Type: Information

Preferred method: Apply a "Vernier" registration pattern to any PCB with <0.8mm pitch BGA, CSP, and flip chip components and / or 0201 or smaller discrete chips so manufacturing can verify the soldermask registration is accurate.

Preferred design for 0.0005" resolution



Alternate Method: Apply a "Chevron" registration pattern to any PCB with <0.8mm pitch BGA, CSP, and flip chip components and / or 0201 or smaller discrete chips so manufacturing can verify the soldermask registration is accurate.



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DFM > PCB Design > Solderpaste

Entry ID: 1306

## Solderpaste

### Rule

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 2 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Do not put solderpaste on non-SMT component pads.

- This can cause solder bridges or solder migration.

Ensure solderpaste is present on all SMT component pads.

- This can cause solder opens.

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 9 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Minimum distance from solderpaste to solderpaste = 0.2100mm

- This can cause solder bridges and decreased stencil life.

|         |                      |                           |
|---------|----------------------|---------------------------|
| CID: 11 | Content Owner: Jabil | Content Type: Requirement |
|---------|----------------------|---------------------------|

Minimum label clearance to solderpaste = 3.7500mm

- Labels too close to solderpaste openings in the stencil can lift the stencil and create printing issues.

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DFM &gt; PCB Design &gt; Solderpaste

Entry ID: 1780

## Solderpaste Stencil Considerations

### Guideline

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 2 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Minimum solderpaste area ratio for individual apertures = 0.66

- A minimum area ratio results in consistent solderpaste release during the printing process.

### Calculations:

Area ratio for square and rectangular apertures is defined as aperture area divided by stencil wall area.

Calculation requires known values for stencil thickness and measured aperture size. (L=Aperture Length, W=Aperture Width, T=Stencil Thickness).

$$\text{Area Ratio} = \frac{\text{Area of Pad}}{\text{Area of Aperture Walls}} = \frac{L \times W}{2 \times (L + W) \times T}$$

Area ratio for circular apertures is defined as diameter divided by 4 times stencil thickness.

Calculation requires known values for stencil thickness and measured aperture size. (D = Aperture Diameter, T = Stencil Thickness).

$$\text{Area Ratio (Diameter)} = \frac{D}{(4 \times T)}$$

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 3 | Content Owner: Jabil | Content Type: Information |
|--------|----------------------|---------------------------|

### Minimum Aspect Ratio (Square / Rectangular):

Aspect ratio is preferred to be greater than 1.5, defined as aperture width (W) divided by stencil thickness (T). A minimum aspect ratio results in consistent solderpaste release during the printing process.

Calculation requires known values for stencil thickness and measured aperture size.

$$\text{Aspect Ratio} = \frac{\text{Width of Aperture}}{\text{Thickness of Stencil Foil}} = \frac{W}{T}$$

### Minimum Aspect Ratio (Circular Aperture):

Aspect ratio is preferred to be greater than 1.5, defined as circumference divided by stencil thickness. A minimum aspect ratio results in consistent solderpaste release during the printing process.

Calculation requires known values for stencil thickness and circumference. (C = Circumference, T = Stencil Thickness).

$$\text{Aspect Ratio} = \frac{C}{T}$$

DFM > PCB Design > Traces

Entry ID: 1031

## Trace Width and Copper to Copper Spacing

### Guideline

|         |                      |                           |
|---------|----------------------|---------------------------|
| CID: 19 | Content Owner: Jabil | Content Type: Requirement |
|---------|----------------------|---------------------------|

For 0.33 oz base copper inner layers: Minimum [trace width](#) = 0.0750mm

For 0.33 oz base copper inner layers: Minimum [copper feature](#) to copper feature spacing = 0.0750mm

For 0.33 oz base copper outer layers: Minimum trace width = 0.0750mm

For 0.33 oz base copper outer layers: Minimum copper feature to copper feature spacing = 0.0750mm

- Failure to do so may cause issues during [PCB fabrication](#) and exceed the PCB vendor's capability.

|         |                      |                           |
|---------|----------------------|---------------------------|
| CID: 10 | Content Owner: Jabil | Content Type: Requirement |
|---------|----------------------|---------------------------|

For 0.5 oz base copper inner layers: Minimum [trace width](#) = 0.1000mm

For 0.5 oz base copper inner layers: Minimum [copper feature](#) to copper feature spacing = 0.1000mm

For 0.5 oz base copper outer layers: Minimum trace width = 0.1000mm

For 0.5 oz base copper outer layers: Minimum copper feature to copper feature spacing = 0.1000mm

- Failure to do so may cause issues during [PCB fabrication](#) and exceed the PCB vendor's capability.

|         |                      |                           |
|---------|----------------------|---------------------------|
| CID: 13 | Content Owner: Jabil | Content Type: Requirement |
|---------|----------------------|---------------------------|

For 1 oz base copper inner layers: Minimum trace width = 0.1000mm

For 1 oz base copper inner layers: Minimum copper feature to copper feature spacing = 0.1000mm

For 1 oz base copper outer layers: Minimum trace width = 0.125mm

For 1 oz base copper outer layers: Minimum copper feature to copper feature spacing = 0.125mm

- Failure to do so may cause issues during [PCB fabrication](#) and exceed the PCB vendor's capability.

|         |                      |                           |
|---------|----------------------|---------------------------|
| CID: 14 | Content Owner: Jabil | Content Type: Requirement |
|---------|----------------------|---------------------------|

For 2 oz base copper inner layers: Minimum trace width = 0.1500mm

For 2 oz base copper inner layers: Minimum copper feature to copper feature spacing = 0.1500mm

For 2 oz base copper outer layers: Minimum trace width = 0.2000mm

For 2 oz base copper outer layers: Minimum copper feature to copper feature spacing = 0.2000mm

- Failure to do so may cause issues during [PCB fabrication](#) and exceed the PCB vendor's capability.

|         |                      |                           |
|---------|----------------------|---------------------------|
| CID: 15 | Content Owner: Jabil | Content Type: Requirement |
|---------|----------------------|---------------------------|

For 3 oz base copper inner layers: Minimum trace width = 0.2000mm

For 3 oz base copper inner layers: Minimum copper feature to copper feature spacing = 0.2000mm

For 3 oz base copper outer layers: Minimum trace width = 0.2250mm

For 3 oz base copper outer layers: Minimum copper feature to copper feature spacing = 0.2250mm

- Failure to do so may cause issues during PCB fabrication and exceed the PCB vendor's capability.

CID: 16

Content Owner: Jabil

Content Type: Requirement

For 4 oz base copper inner layers: Minimum trace width = 0.2500mm

For 4 oz base copper inner layers: Minimum copper feature to copper feature spacing = 0.3000mm

For 4 oz base copper outer layers: Minimum trace width = 0.2750mm

For 4 oz base copper outer layers: Minimum copper feature to copper feature spacing = 0.3000mm

- Failure to do so may cause issues during PCB fabrication and exceed the PCB vendor's capability.

CID: 18

Content Owner: Jabil

Content Type: Requirement

Minimum plane to plane spacing = 0.3000mm

- Failure to do so may cause issues during PCB fabrication and exceed the PCB vendor's capability.

CID: 17

Content Owner: Jabil

Content Type: Requirement

Minimum inner layer copper feature to edge of **PTH** drill spacing = 0.2250mm

- Accuracy tolerance may allow the drill to cut into the copper feature.

CID: 20

Content Owner: Jabil

Content Type: Requirement

Avoid photoresist and copper **slivers**.

- A photoresist or copper sliver might cause material to detach during the photo-imaging and etching processes in PCB fabrication. The floating piece can cause solder defects and / or shorts.

CID: 21

Content Owner: Jabil

Content Type: Requirement

Avoid nets making unintentional contact with other nets or copper features. **\*\*coverage cad\_short, \*:no\_net\_name\_short\*\***

- Two separate nets or a net and another copper feature touching each other could represent a design issue. If it is an issue, this may cause a delay at the PCB manufacturer.

Avoid loops in a signal net. **\*\*coverage net\_loop\*\***

- If a single net is touching a copper feature in two different locations, this could create a closed loop and may represent a design issue. If it is an issue, this may cause a delay at the PCB manufacturer.

## Related Entries



## Copper Between Component Pads

### Guideline

CID: 2

Content Owner: Jabil

Content Type: Requirement

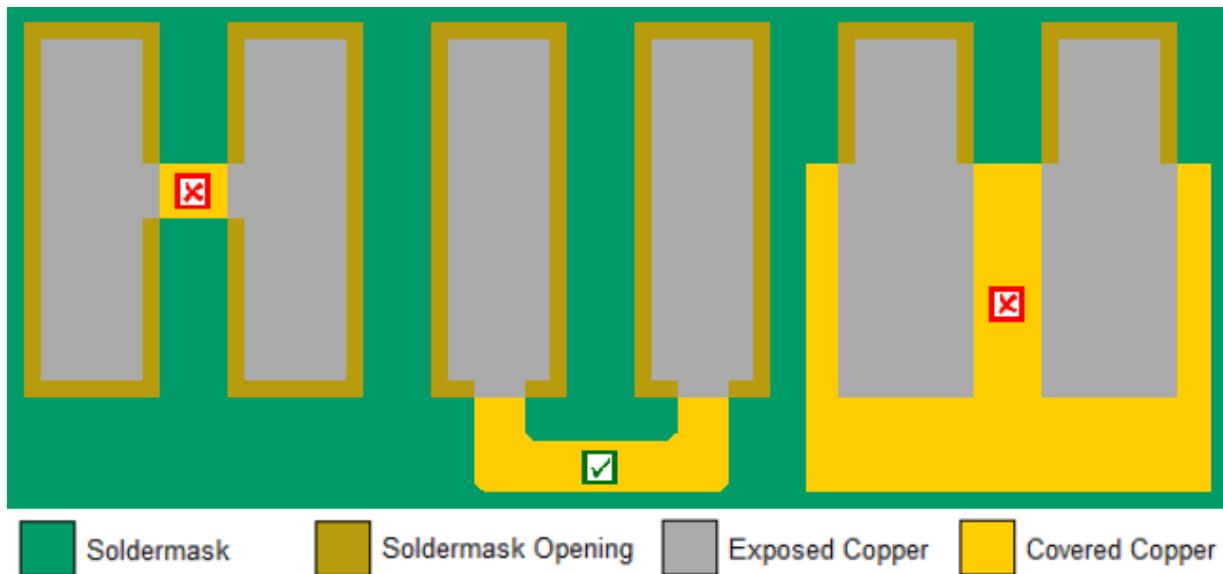
#### For SMT connectors, networks, PLCCs, QFNs, QFPs, SOICs, and SOTs:

Do not route traces directly between adjacent component pads on outer PCB layers.

Do not place copper pours / planes between adjacent component pads on outer PCB layers.

- This can look like a solder bridge at inspection and they may try to repair it, potentially damaging the PCB.

**Note:** electrical current capacity, thermal dissipative, and / or RF requirements may override the need for compliance.



## Narrow Trace Connections to Pads

### Guideline

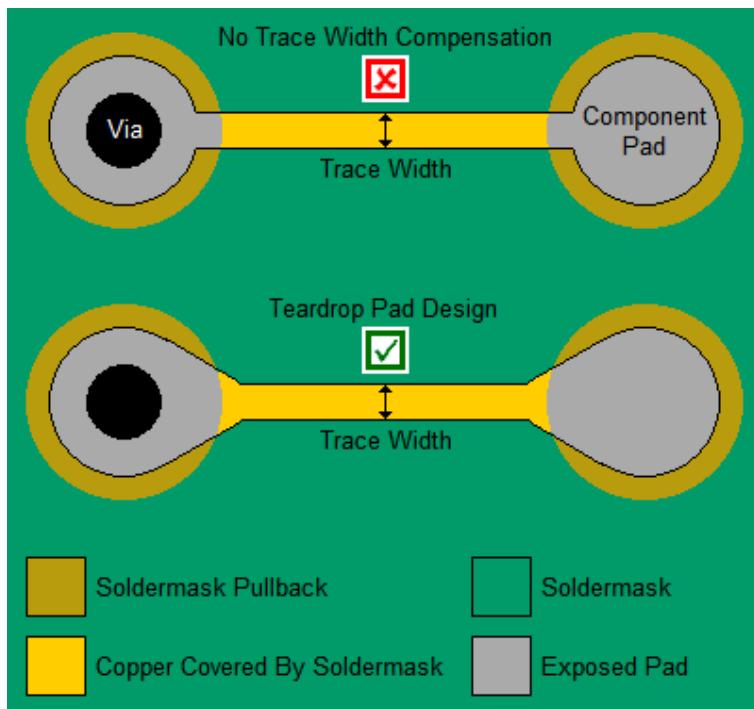
CID: 5

Content Owner: Jabil

Content Type: Requirement

For **via** and **THMT** component pads, utilize a teardrop pad design for connecting **trace** widths less than or equal to 0.1500mm

- This can allow the drill to break the pad to trace connection if drilled off center or may result in trace cracking at the pad to trace junction due to thermal cycling.



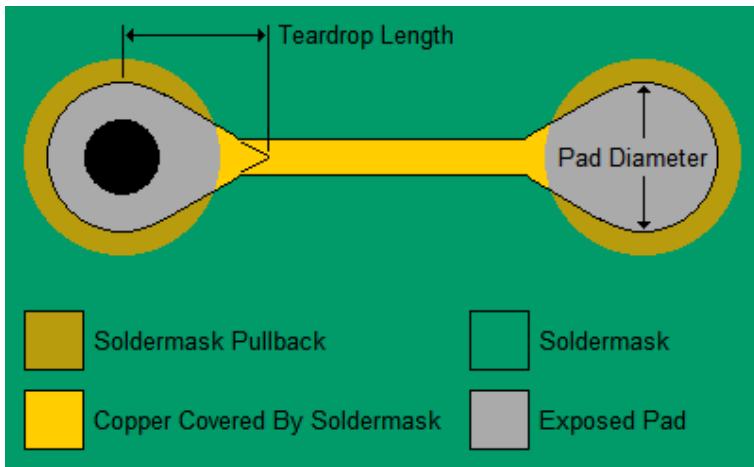
CID: 4

Content Owner: Jabil

Content Type: Requirement

For teardrop pad designs, teardrop length = pad diameter

- This may result in the pad not providing adequate mitigation for the narrow trace.



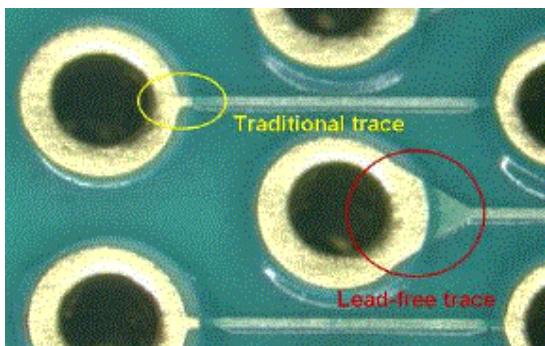
CID: 6

Content Owner: Jabil

Content Type: Requirement

For lead-free wave soldered THMT components and vias, route traces internally or utilize a teardrop pad design.

- When exposed to lead-free wave solder, the trace can be dissolved.
- Additionally, an ENIG PCB finish may be used to further reduce potential copper dissolution due to the nickel layer under the gold.



## Related Entries

[DFM Guideline 1031 PCB Design > Traces > Trace Width and Copper to Copper Spacing](#)

[DFM Guideline 1054 PCB Design > Vias > Vias and Micro-Vias](#)

[DFM Rule 1074 PCB Design > General > BGA Pads and Trace Connections](#)

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## Vias Under a BGA Exposed to the Wave Solder

### Rule

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 2 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Vias under a BGA that are exposed to the [wave solder](#) must be protected. Lack of protection can lead to solder wicking up the vias and shorting the BGA as well as the BGA joint being exposed to an additional thermal cycle. Protect the exposed vias opposite the BGA, use of a selective [masked pallet](#) (preferred) or [plugging](#) from the topside (more expensive).

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## Through Hole Via-in-Pad for Surface Mount Components

### Rule

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 2 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Do not use through hole **via-in-pad** for surface mount components.

- This can cause voids or solder wicking during the **reflow process** which weakens the solder joint.
- **Solderpaste** covering the through-hole via will liquefy during the reflow process and "wick" into the hole if it is not **plugged** causing insufficient solder in the joint.
- **BGAs, CSPs, and Flip Chip** devices are especially susceptible to this problem and via-in-pad should be avoided if at all possible.
- Potential mitigation options include routing the via away from the component pad, utilizing **blind vias**, **filled / planarized vias** or **plated over filled vias**. The use of blind vias, plated over filled vias etc. may increase the cost of the assembly.

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 5 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

In thermal pads, utilize the minimum via hole size possible while still maintaining the via aspect ratio (see [Entry 1054](#)).

- For example, a PCB thickness of 1.5700mm would be a via hole size of 0.200mm and a PCB thickness of 2.3600mm would be a hole size of 0.2950mm.
- Solder may wick down the large via holes and result in solder voids, insufficient solder, and solder balls on the opposite side of the PCB.
- Soldermask via plugging, **VIPPO** (see [Entry 1054](#)) or having copper pads attached on all layers may be effective mitigation techniques.
- **Note:** when using a vacuum reflow oven, it may be required to use VIPPO as a mitigation technique to prevent solder wicking.

### Related Entries

DFM Information [1385](#) Component Land Pattern > SMT > Land Patterns for BGA Components

DFM Information [1326](#) PCB Design > Vias > Via Treatments

DFM > PCB Design > Vias

Entry ID: 1054

## Vias and Micro-Vias

### Guideline

CID: 19

Content Owner: Jabil

Content Type: Requirement

Minimum [via](#) hole diameter = 0.2000mm

Via pad size = via hole diameter + 0.2500mm

- This may cause [PCB](#) manufacturability issues.

CID: 34

Content Owner: Jabil

Content Type: Requirement

For mechanically drilled vias: maintain a maximum aspect ratio of 8 (drilled layer thickness / via hole diameter).

For laser drilled vias: maintain a maximum aspect ratio of 0.8 (drilled layer thickness / via hole diameter).

- This may exceed PCB manufacturing physical limitations.

Do not cover vias on both sides of the PCB.

- Vias cannot be [tented](#) on both sides of the PCB in the [reflow oven](#) or [wave soldering](#), the entrapped air can blow out the tenting material.
- Chemicals can be trapped inside the barrel of the via and may result in latent failures.

For [OSP](#) and [ENIG](#) PCB surface finishes: do not cover vias with [soldermask](#).

- If vias are covered or filled with soldermask, chemicals related to OSP and ENIG can get trapped inside the via and cause latent field failures.

Ensure vias are not located under components with metal surfaces.

- Metal component surfaces may make contact with vias and create electrical shorts.

Avoid selecting [tent](#)ed vias.

- Soldermask coverage for tented vias can be inconsistent, sometimes covering the hole and sometimes not. Tented vias can also create uneven PCB surface profiles and result in [solderpaste](#) printing issues and / or solder draining into the via holes instead of staying on the surface of the PCB.

Minimum soldermask opening for [encroached vias](#) = via hole size + 50% of the via [annular ring](#).

- If the soldermask opening is too small, the soldermask could get in the hole, blocking it.

CID: 22

Content Owner: Jabil

Content Type: Requirement

**Observe via spacing requirements on [signal \(positive\) layers](#):**

Minimum via pad edge to via pad edge = 0.1000mm

Minimum via pad edge to all other [copper features](#) = 0.1000mm

- This may cause PCB manufacturability issues.

Minimum exposed via pad edge to exposed via pad edge on [reflow soldered](#) side of PCBs = 0.1000mm

Minimum exposed via pad edge to exposed copper features on reflow soldered side of PCBs = 0.2500mm

Minimum exposed via pad edge to exposed component pad edge on reflow soldered side of PCBs = 0.1500mm

Minimum exposed via pad edge to exposed component pad edge on [wave soldered](#) side of PCBs = 0.7500mm

- This may cause solder bridging issues.

CID: 24

Content Owner: Jabil

Content Type: Requirement

#### **Observe via spacing requirements on signal (positive) layers:**

Minimum exposed via pad edge to exposed via pad edge on wave soldered side of PCBs = 0.7500mm

Minimum exposed via pad edge to exposed copper on wave soldered side of PCBs = 0.7500mm

- This may cause solder bridging issues.

Minimum gap between the top of plated exposed vias to the underside of the body of leadless or chip components = 0.1250mm

- This may cause manufacturability or shorting issues.

CID: 29

Content Owner: Jabil

Content Type: Requirement

Minimum edge of via drill to edge of copper features = 0.2250mm

- This may cause PCB manufacturability issues.

CID: 26

Content Owner: Jabil

Content Type: Requirement

Avoid using laser drilled [micro-vias](#).

- Micro-via layers are very thin and bottom side layers exposed to wave soldering can result in delamination.

CID: 37

Content Owner: Jabil

Content Type: Requirement

Ensure through hole vias are connected to an outer layer, and at least one additional layer.

- This could indicate a design problem, sometimes referred to as an antenna stub, because there is no electrical connection.

CID: 38

Content Owner: Jabil

Content Type: Requirement

#### **VIPPO specific requirements:**

For [VIPPO](#): minimum FHS = 0.2000mm and maximum FHS = 0.5000mm

- Other sizes outside this range may have issues consistently filling.

For VIPPO: utilize a maximum of three different sizes for FHS in the same PCB.

- More than three sizes could exceed the PCB supplier capabilities.

For VIPPO: the maximum difference between the smallest and largest FHS in the same PCB is <=0.1500mm

- Too large of a difference in FHS sizes could exceed the PCB supplier capabilities.

For VIPPO: minimum PCB thickness = 0.6000mm

- PCBs that are too thin could exceed the PCB supplier capabilities.

For VIPPO: specify a maximum bump of 0.0025mm and a maximum dimple of 0.0025mm

- Controlling the flatness of the component pad is necessary to prevent solder voiding. BGA components may be more susceptible to this issue.
- IPC-6012 specifies a maximum bump of 0.0050mm and a maximum dimple of 0.0076mm. This total range of allowable variation is too large to consistently control voiding and should not be applied.

**Note:** if the design requires violating any of these VIPPO specific requirements, contact the PCB supplier to ensure capability.

## Related Entries

---

DFM Guideline [1031](#) PCB Design > Traces > Trace Width and Copper to Copper Spacing

DFM Rule [1295](#) PCB Design > General > NPTH Clearance

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## Surface Mounted Shields and RF Circuits

### Guideline

CID: 2

Content Owner: Jabil

Content Type: Requirement

Ensure grounding [vias](#) at the shield / [PCB](#) interface of surface mounted shields in an [RF](#) circuit have a spacing of  $1/10^{\text{th}}$  the wavelength at the highest frequency of operation.

- The absence of grounding vias can result in poor performance of the RF circuit by allowing interference.

Grounding vias need to be placed around the perimeter of the shield. The calculation of wavelength is to be performed in the respective medium such as in the PCB material as opposed to the wavelength in air. The placement and quantity of grounding vias can influence the electrical characteristics and lead to poor performance of the RF circuit.

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DFM > Component Land Pattern > General

Entry ID: 1039

## Selective and Wave Soldered THMT Component Pads

### Guideline

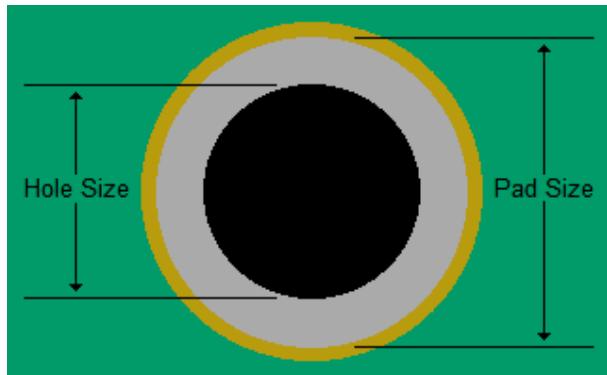
CID: 4

Content Owner: Jabil

Content Type: Requirement

Minimum **selective** and **wave soldered THMT** component pad size on both sides of the **PCB** = finished hole size + 0.4000mm

- This could cause soldering issues or pad lifting.



CID: 5

Content Owner: Jabil

Content Type: Requirement

For selective and wave soldered THMT components: minimum exposed pad to exposed pad spacing within a single THMT component = 0.7500mm

- Pads that are too close together have a higher likelihood of solder bridging.

For selective and wave soldered THMT components: round pads are recommended.

- Square pads tend to retain more solder and can result in more frequent solder bridging.
- Square pads can be soldermask defined to emulate the round shape.

### Related Entries

[DFM Rule 1032](#) PCB Design > Soldermask > Personalized Soldermask Requirements

[DFM Rule 1314](#) Component Land Pattern > General > Selective and Wave Soldered THMT Component Hole Size

[DFM Rule 1077](#) PCB Design > General > Auto-Insertion

[DFM Rule 1076](#) PCB Design > General > Thermal Reliefs

DFM > Component Land Pattern > General

Entry ID: 1314

## Selective and Wave Soldered THMT Component Hole Size

### Rule

CID: 4

Content Owner: Jabil

Content Type: Requirement

#### For tin-lead selective and wave soldered THMT component pins with a pitch of 2.5000mm or greater:

Finished hole size = maximum lead diameter (Dimension A) + minimum of 0.3000mm and maximum of 0.7000mm

Recommended finished hole size = maximum lead diameter (Dimension A) + 0.5000mm

- Smaller sizes may not fill completely and larger holes may allow the solder to drain (also referred to as "drool") out of the hole before the solder joint solidifies. If holes are overly large, the component may not maintain the intended position.

#### For tin-lead selective and wave soldered THMT component pins with a pitch less than 2.5000mm, maximum copper weight of 2oz, and PCB thickness less than 2.5000mm:

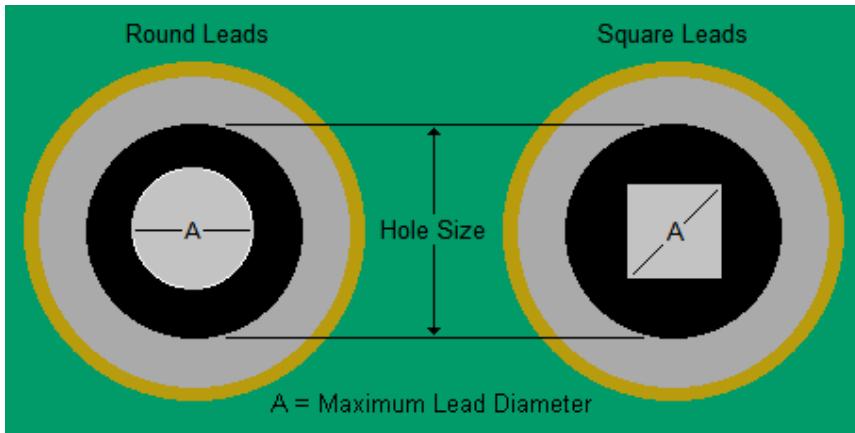
Round pins: finished hole size = maximum lead diameter (Dimension A) + minimum of 0.3000mm and maximum of 0.7000mm

Recommended finished hole size = maximum lead diameter (Dimension A) + 0.5000mm

Square pins: finished hole size = maximum lead diameter (Dimension A) + minimum of 0.2000mm and maximum of 0.6000mm

Recommended finished hole size = maximum lead diameter (Dimension A) + 0.4000mm

- Smaller sizes may not fill completely and larger holes may allow the solder to drain (also referred to as "drool") out of the hole before the solder joint solidifies. If holes are overly large, the component may not maintain the intended position.



**Note:** For components with a pitch less than 2.5000mm, hole diameter may have to be smaller than specified to avoid violating other design relationships. The hole should be made as large as practically possible and / or [Personalized Solder Mask \(PSM\)](#) should be utilized. See [Entry 1032](#) for details. Contact the [DFx team](#) for additional assistance.

CID: 6

Content Owner: Jabil

Content Type: Requirement

#### For lead-free selective and wave soldered THMT component pins:

##### Low thermal mass pins:

Finished hole size = maximum lead diameter (Dimension A) + minimum of 0.5500mm and maximum of 0.6500mm

Recommended finished hole size = maximum lead diameter (Dimension A) + 0.6000mm

- Smaller sizes may not fill completely and larger holes may allow the solder to drain (also referred to as "drool") out of the hole before the solder joint solidifies. If holes are overly large, the component may not maintain the intended position.

#### **High thermal mass - adjacent pins:**

Finished hole size = maximum lead diameter (Dimension A) + minimum of 0.7000mm and maximum of 0.8000mm

Recommended finished hole size = maximum lead diameter (Dimension A) + 0.7500mm

- Smaller sizes may not fill completely and larger holes may allow the solder to drain (also referred to as "drool") out of the hole before the solder joint solidifies. If holes are overly large, the component may not maintain the intended position.

#### **High thermal mass - isolated pins:**

Finished hole size = maximum lead diameter (Dimension A) + minimum of 0.9500mm and maximum of 1.0500mm

Recommended finished hole size = maximum lead diameter (Dimension A) + 1.0000mm

- Smaller sizes may not fill completely and larger holes may allow the solder to drain (also referred to as "drool") out of the hole before the solder joint solidifies. If holes are overly large, the component may not maintain the intended position.

#### **For lead-free selective and wave soldered THMT component pins with a pitch less than 2.5000mm, maximum copper weight of 2oz, and PCB thickness less than 2.5000mm:**

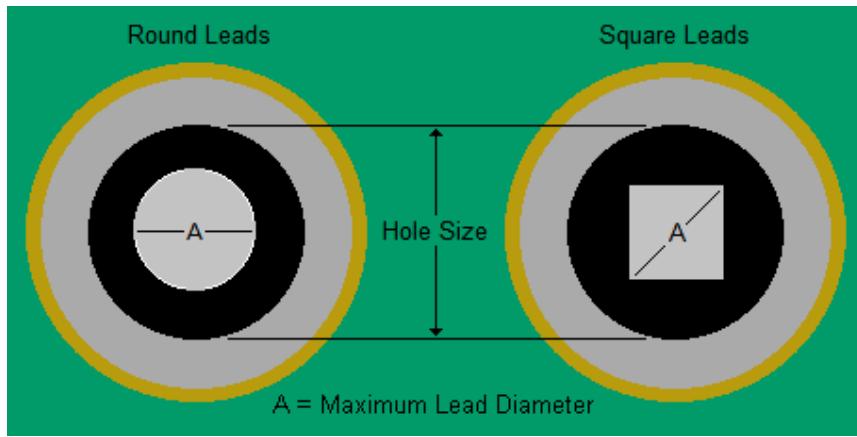
Round pins: finished hole size = maximum lead diameter (Dimension A) + minimum of 0.3000mm and maximum of 0.7000mm

Recommended finished hole size = maximum lead diameter (Dimension A) + 0.5000mm

Square pins: finished hole size = maximum lead diameter (Dimension A) + minimum of 0.2000mm and maximum of 0.6000mm

Recommended finished hole size = maximum lead diameter (Dimension A) + 0.4000mm

- Smaller sizes may not fill completely and larger holes may allow the solder to drain (also referred to as "drool") out of the hole before the solder joint solidifies. If holes are overly large, the component may not maintain the intended position.



**Note:** For components with a pitch less than 2.5000mm, hole diameter may have to be smaller than specified to avoid violating other design relationships. The hole should be made as large as practically possible and / or [Personalized Solder Mask \(PSM\)](#) should be utilized. See [Entry 1032](#) for details. Contact the [DFx team](#) for additional assistance.

**Note:** For PCB thicknesses less than 1.5000mm or more than 3.0000mm contact the [DFx team](#) for assistance.

#### Related Entries

DFM Rule [1032](#) PCB Design > Soldermask > Personalized Soldermask

DFM Guideline [1039](#) Component Land Pattern > General > Selective and Wave Soldered THMT Component Pads

DFM Rule 1077 PCB Design > General > Auto-Insertion

DFM Rule 1076 PCB Design > General > Thermal Reliefs

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DFM > Component Land Pattern > General

Entry ID: 1701

## Component Pin to PCB Pad

### Guideline

CID: 3

Content Owner: Jabil

Content Type: Information

#### Introduction:

The placement of each component in regard to component pin and PCB pad location, size and orientation is a major factor in product quality.

The following guidelines specify acceptable ranges for the relationships between component pins and their associated PCB pads.

CID: 2

Content Owner: Jabil

Content Type: Requirement

#### Component Pin to PCB Pad Distances:

Observe minimum **heel** distance.

Observe minimum **toe** distance.

Observe minimum **left and right** distance.

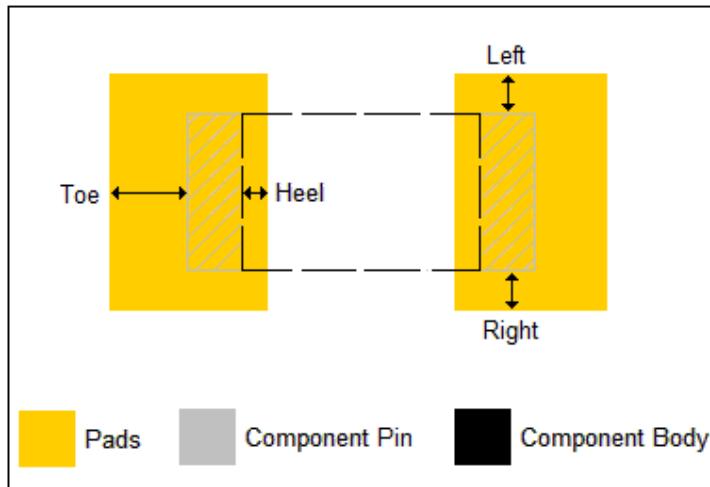
- Failure to observe the specified values could result in poor or incomplete solder joints making it difficult to achieve **IPC** requirements due to a lack of solderable surface area.

Observe maximum heel distance.

Observe maximum toe distance.

Observe maximum left and right distance.

- Failure to observe the specified values could result in available PCB area being unavailable for other design features. Components may move during **reflow soldering**, **solder balls** are more likely and **solder joints** may be insufficient due to excess solderable surface area dispersing the solder volume.



| Component Type | Min Heel | Max Heel | Min Toe  | Max Toe  | Min Left & Right | Max Left & Right |
|----------------|----------|----------|----------|----------|------------------|------------------|
| SMT Connector  | 0.3000mm | 0.8000mm | 0.3000mm | 0.8000mm | 0.0300mm         | 0.0500mm         |
| Discrete 01005 | 0.0000mm | 0.0300mm | 0.0800mm | 0.1500mm | 0.0000mm         | 0.0250mm         |

| Component Type          | Min Heel | Max Heel | Min Toe  | Max Toe  | Min Left & Right | Max Left & Right |
|-------------------------|----------|----------|----------|----------|------------------|------------------|
| Discrete 0201           | 0.0000mm | 0.0400mm | 0.1000mm | 0.1800mm | 0.0000mm         | 0.0500mm         |
| Discrete 0402           | 0.0000mm | 0.0750mm | 0.1000mm | 0.2500mm | 0.0000mm         | 0.0500mm         |
| Discrete 0603           | 0.0000mm | 0.1000mm | 0.2000mm | 0.5000mm | 0.0000mm         | 0.1000mm         |
| Discrete 0805           | 0.0000mm | 0.1000mm | 0.3000mm | 0.6000mm | 0.0000mm         | 0.1250mm         |
| Discrete Other          | 0.0000mm | 0.1500mm | 0.4000mm | 0.9500mm | 0.0000mm         | 0.2000mm         |
| Discrete Tall           | 0.1000mm | 0.9500mm | 0.2500mm | 1.0000mm | 0.3500mm         | 0.6500mm         |
| MELF                    | 0.0000mm | 0.7000mm | 0.2250mm | 0.6000mm | 0.0000mm         | 0.2500mm         |
| Network                 | 0.0000mm | 0.1000mm | 0.2000mm | 0.6000mm | 0.0000mm         | 0.0500mm         |
| PLCC                    | 0.1500mm | 0.3000mm | 0.3000mm | 0.9500mm | 0.0500mm         | 0.2000mm         |
| QFN Cwrap               | 0.0000mm | 0.1000mm | 0.2000mm | 0.8000mm | 0.0000mm         | 0.0500mm         |
| QFN Leadless            | 0.0000mm | 0.2000mm | 0.0000mm | 0.2000mm | 0.0000mm         | 0.2000mm         |
| QFP Fine Pitch          | 0.3000mm | 0.8000mm | 0.2000mm | 0.8000mm | 0.0000mm         | 0.0500mm         |
| QFP Standard Pitch      | 0.3000mm | 0.8000mm | 0.2000mm | 0.8000mm | 0.0000mm         | 0.0750mm         |
| SMT Covering            | 0.2000mm | 0.4000mm | 0.2000mm | 0.6000mm | 0.0000mm         | 0.1000mm         |
| SMT Miscellaneous Short | 0.3000mm | 0.8000mm | 0.2000mm | 0.6000mm | 0.2500mm         | 1.0000mm         |
| SMT Miscellaneous Tall  | 0.3000mm | 0.8000mm | 0.2000mm | 0.6000mm | 0.2500mm         | 1.0000mm         |
| SOIC Fine Pitch         | 0.3000mm | 0.8000mm | 0.2000mm | 0.8000mm | 0.0250mm         | 0.0500mm         |
| SOIC Standard Pitch     | 0.3000mm | 0.8000mm | 0.2000mm | 0.9000mm | 0.0500mm         | 0.2000mm         |
| SOT                     | 0.1000mm | 0.3000mm | 0.2000mm | 0.6000mm | 0.1000mm         | 0.2000mm         |
| Tantalum                | 0.0000mm | 1.0000mm | 0.2750mm | 0.9000mm | 0.0000mm         | 0.7000mm         |

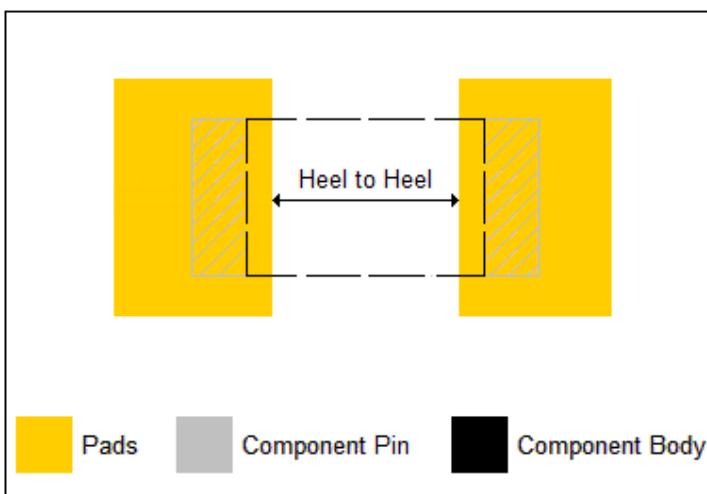
#### Heel to Heel Gap for Discrete Components:

Observe minimum heel to heel distance for discrete components.

- If the distance is too small, solder balls are more likely to form.

Observe maximum heel to heel distance for discrete components.

- If the distance is too large, the component may tombstone during reflow soldering.



| Component Type | Min Heel to Heel | Max Heel to Heel |
|----------------|------------------|------------------|
| Discrete 01005 | 0.1500mm         | 0.2000mm         |
| Discrete 0201  | 0.2000mm         | 0.3000mm         |
| Discrete 0402  | 0.3500mm         | 0.5000mm         |

| Component Type | Min Heel to Heel | Max Heel to Heel |
|----------------|------------------|------------------|
| Discrete 0603  | 0.6000mm         | 0.8000mm         |
| Discrete 0805  | 0.8000mm         | 1.0000mm         |

CID: 4

Content Owner: Jabil

Content Type: Requirement

**Automated Checks:**

The pin holes of [THMT auto-inserted](#), [press fit](#) and [PTH](#) components must be plated.

- The solder joint will not form properly and will not complete the circuit.

Ensure all [THMT](#) pins have corresponding holes in the PCB.

- A hole is necessary to insert the THMT component pins into the PCB.

Ensure [THMT](#) auto-inserted, press fit and PTH components only have one drill hole defined for each pin location.

- More than one drill defined for a pin hole complicates the PCB supplier's drilling process.

Ensure [QFN](#) component pins are not larger than the corresponding pad.

- The component may not solder properly.

Ensure mechanical pins for THMT auto-inserted, press fit and PTH components have copper clearances on all [plane](#) layers.

- An electrical connection is not necessary for mechanical pins and connecting them to planes will reduce the ability to form an adequate solder joint.

Ensure all [SMT](#) pins have corresponding pads on the PCB.

- A pad is necessary to solder the component pin to the PCB.

Ensure THMT auto-inserted and PTH component pins are not larger than their corresponding drilled hole.

- The component will not fit in the holes.

Ensure press fit pins are not smaller than their corresponding drilled holes.

- The component may not have a reliable electrical connection and may not stay connected to the PCB.

Ensure SMT component pins do not touch [soldermask](#).

- The component pins may not form adequate solder joints.

Ensure the component pin [pitch](#) matches the pad pitch.

- The component may not fit or solder properly.

CID: 5

Content Owner: Jabil

Content Type: Requirement

## Manual Checks:

Do not put soldermask between the pads of discrete 01005 and 0201 components.

- The soldermask can lift the [solderpaste stencil](#) causing the solderpaste to smear.

For [DFNs](#), [QFNs](#), [QFPs](#), SMT connectors and [SOICs](#): verify the pad width for the associated pitch.

| Pitch    | Recommended Pad Width |
|----------|-----------------------|
| 0.4000mm | 0.2400mm              |
| 0.5000mm | 0.2800mm              |
| 0.6500mm | 0.4000mm              |
| 0.8000mm | 0.5000mm              |
| 1.0000mm | 0.6000mm              |
| 1.2700mm | 0.7000mm              |

- Pin width for these component types can vary significantly so following the recommended pad width is necessary to ensure all component pins will fit on the pads.

For [gull wing](#) component bodies with a standoff less than or equal to 0.1000mm from the PCB surface: the pads should not extend underneath the component body.

- The solderpaste could touch the component body resulting in component drift and / or solder balls during reflow soldering.

For the [thermal PCB pad](#) underneath DFNs, QFNs and QFPs: the preferred PCB pad size is the nominal component thermal pin size.

- Matching the maximum component thermal pin size can result in decreased spacing between the PCB thermal pad and the other component pads causing shorts.

Ensure components with a positional tolerance of +/- 0.2000mm or less have appropriate land patterns.

- Components may shift more than allowed during reflow soldering with typical land patterns.

Ensure NPTH alignment pins meet the size tolerances necessary.

- If the NPTH size tolerance is too large, the component will not consistently meet the required positional tolerance.

Utilize soldermask defined pads for electrolytic caps and SMT connector [anchor pads](#).

- Electrolytic caps and SMT connectors are more likely to get ripped off the PCB.
- Utilizing a larger copper pad that is soldermask defined increases the peel strength.

Ensure thermal pads are not covered by soldermask and / or missing completely.

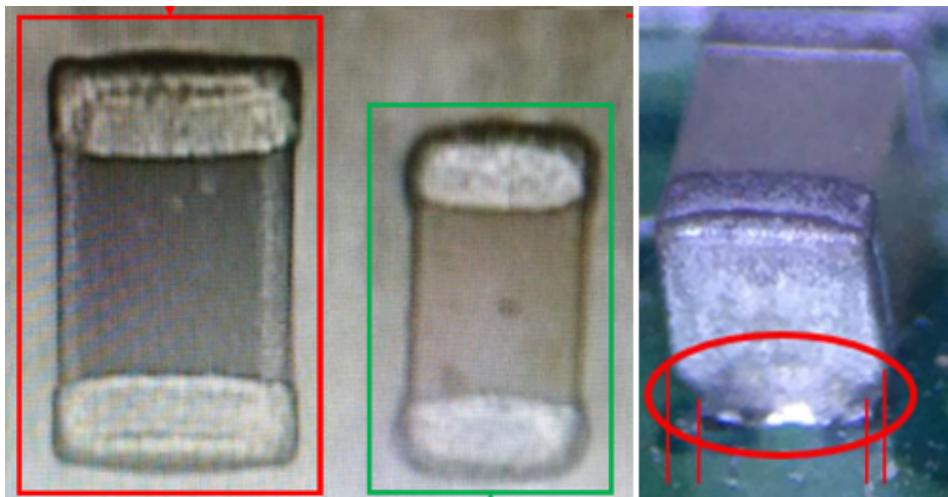
- If the thermal pad is not present or the heat is not able to transfer to the PCB, the component may fail.

Ensure the soldermask opening for battery holders allows good electrical contact.

- If the soldermask opening is too small, it could prevent the battery from making good electrical contact with the pad on the PCB.

For all discrete-0402 MLCC capacitors: if the length or width of the body +/- tolerance is 0.1500mm or larger, verify the land pattern size will accommodate the larger than normal 0402 body.

- All affected MPNs per customer part numbers in the BOM for the 0402 MLCC capacitors must have their datasheets checked to verify the maximum body tolerance.
- These 0402 capacitors tend to be at the high end of the tolerance range and will not fit on most typical 0402 land patterns, so there will not be adequate solder fillets.
- In order to avoid the parts not fitting on the pad, the recommended land pattern is: width 0.6000mm X length 0.5250mm X 0.4000mm heel to heel.
- **Note:** the body height is not a factor in selecting the land pattern.



Ensure press fit component hole sizes are within the recommended hole size range and the PCB surface finish is compatible per the component vendor datasheet.

- Holes that are too small may cause issues during insertion and holes that are too large may not provide adequate mechanical or electrical contact. An incompatible PCB surface finish could cause additional friction on the pins, making it difficult or impossible to consistently insert the pins.

DFM > Component Land Pattern > SMT

Entry ID: 1047

## Soldermask for SMT Discrete Components

### Rule

CID: 2

Content Owner: Jabil

Content Type: Requirement

**SMT discrete components** of size 0402 (1005 metric) or larger should have a [soldermask web](#) between the pads within the padstack. This provides better isolation to reduce the risk of solder shorts in case of solder smearing.

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DFM > Component Land Pattern > SMT

Entry ID: 1349

## Pad Shapes for Automated X-ray

### Information

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 1 | Content Owner: Jabil | Content Type: Information |
|--------|----------------------|---------------------------|

For enhanced defect detection at x-ray use alternative pad shapes for [BGA](#), [CBGA](#), [flip chip](#) and [CSP](#). Diamond shaped pads produce the clearest contrast between a good and bad solder joint.

There is an unknown reliability impact when using alternate pad shapes, see [Entry 1074](#) for circular pad requirements.

Alternative pad shapes:

- Preferred choice – diamond pads
- Second choice – octagon pads
- Third choice – oval pads

### Related Entries

DFM Rule [1074](#) PCB Design > General > BGA Pads and Trace Connections

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DFM &gt; Component Land Pattern &gt; SMT

Entry ID: 1380

## Land Pattern for C / L Shaped Leads

### Information

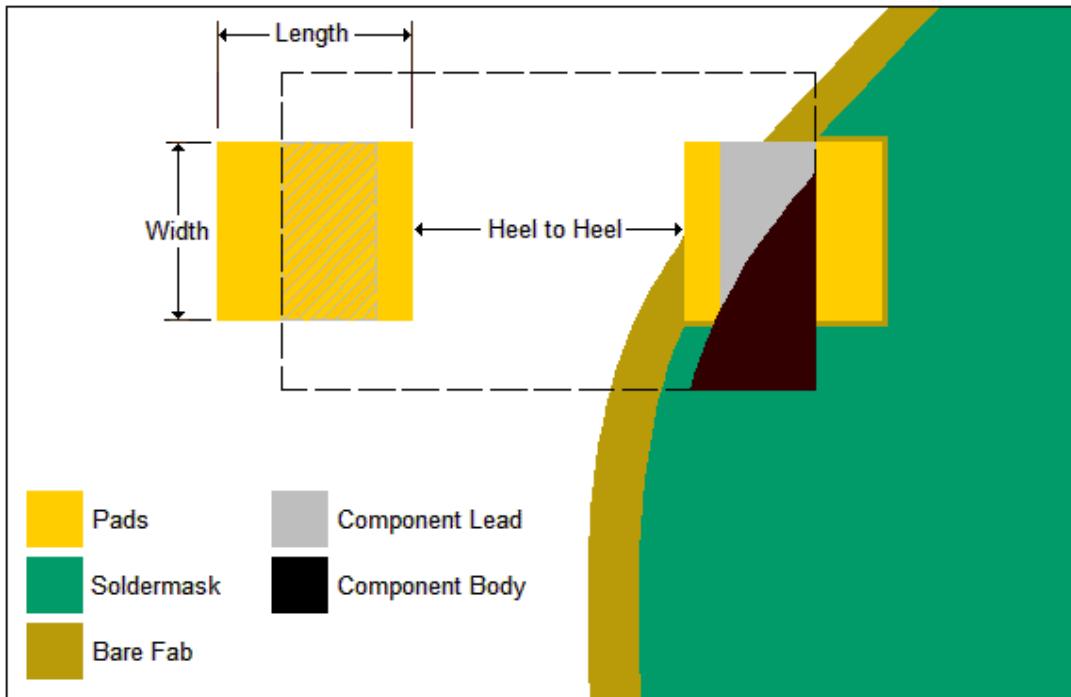
CID: 2

Content Owner: Jabil

Content Type: Information

Land pattern dimensions for rectangular components with C / L shaped leads.

| Package Style<br>English (Metric) | Land Pattern Dimensions |          |              |
|-----------------------------------|-------------------------|----------|--------------|
|                                   | Width                   | Length   | Heel to Heel |
| 0805 (2012)                       | 1.4000mm                | 0.9000mm | 1.0000mm     |
| (2520)                            | 1.6000mm                | 1.0500mm | 1.3000mm     |
| 1206 (3216)                       | 1.4000mm                | 1.1000mm | 1.9000mm     |
| 1210 (3225)                       | 1.4000mm                | 1.1000mm | 1.9000mm     |
| 1210 (3225)                       | 2.3000mm                | 1.1000mm | 1.9000mm     |
| (3528)                            | 2.5000mm                | 1.1000mm | 2.2000mm     |
| 1812 (4532)                       | 3.2000mm                | 1.4000mm | 2.8000mm     |
| (4726)                            | 2.0000mm                | 1.4500mm | 2.9000mm     |
| (5225)                            | 1.7000mm                | 1.9500mm | 2.5000mm     |
| (5535)                            | 2.6000mm                | 1.9000mm | 2.8000mm     |
| (5650)                            | 4.4000mm                | 1.6000mm | 3.5000mm     |
| (5846)                            | 3.3000mm                | 1.6500mm | 3.6000mm     |
| (6032)                            | 2.5000mm                | 1.7000mm | 3.7000mm     |
| (7343)                            | 3.0000mm                | 1.9500mm | 4.5000mm     |
| (7358)                            | 4.1000mm                | 1.9500mm | 4.5000mm     |
| (7640)                            | 2.7000mm                | 2.0000mm | 4.7000mm     |
| (8040)                            | 3.7000mm                | 2.0500mm | 5.0000mm     |
| (8059)                            | 3.7000mm                | 2.0500mm | 5.0000mm     |



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## Land Pattern for SOJ Components

### Information

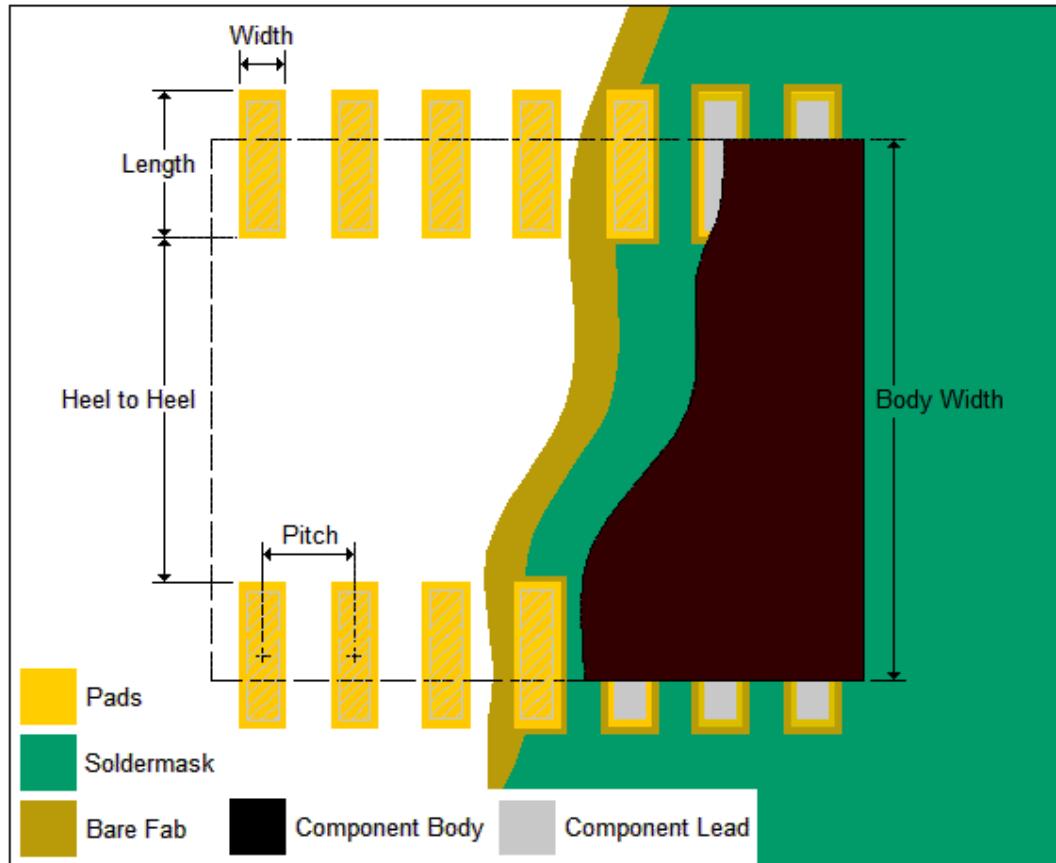
CID: 2

Content Owner: Jabil

Content Type: Information

Land pattern dimensions for [SOJ](#) components.

| Component Body Width English (Metric) | Pitch    | Heel to Heel | Width    | Length   |
|---------------------------------------|----------|--------------|----------|----------|
| 7.6200mm                              | 1.2700mm | 5.1000mm     | 0.7000mm | 3.2000mm |
| 8.8900mm                              | 1.2700mm | 6.4000mm     | 0.7000mm | 3.1000mm |
| 10.1600mm                             | 1.2700mm | 7.6000mm     | 0.7000mm | 3.3000mm |
| 12.7000mm                             | 1.2700mm | 10.2000mm    | 0.7000mm | 3.2000mm |
| 15.2400mm                             | 1.2700mm | 12.7000mm    | 0.7000mm | 3.2000mm |



## Land Pattern for Chip Components

### Information

CID: 3

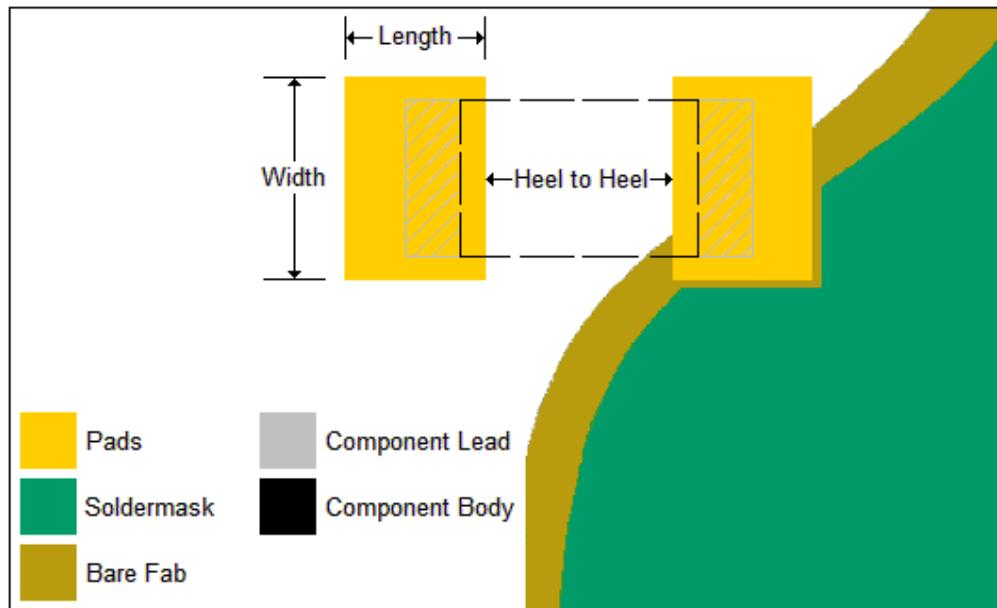
Content Owner: Jabil

Content Type: Information

Land pattern dimensions for chip components.

| Standard Package Style English (Metric)         | Width    | Length   | Heel to Heel |
|---|----------|----------|--------------|
| 0402 (1005)                                     | 0.5000mm | 0.4250mm | 0.4000mm     |
| <b>MLCC 0402 (1005) capacitors (see Note 1)</b> | 0.6000mm | 0.5250mm | 0.4000mm     |
| 0603 (1608)                                     | 0.8000mm | 0.7000mm | 0.8000mm     |
| 0805 (2012)                                     | 1.2500mm | 0.9000mm | 1.0000mm     |
| 1206 (3216)                                     | 1.6000mm | 1.0500mm | 2.0000mm     |
| 1210 (3225)                                     | 2.5000mm | 1.1500mm | 1.9000mm     |
| 1806 (4516)                                     | 1.9000mm | 1.3000mm | 2.8000mm     |
| 1812 (4532)                                     | 3.5000mm | 1.3500mm | 2.8000mm     |
| 2220 (5650)                                     | 5.3000mm | 1.6000mm | 3.5000mm     |

**Note 1:** for 0402 MLCC capacitors - if the length or width of the body +/- tolerance is 0.1500mm or larger, a larger land pattern is necessary or the capacitor may not fit on the pad.



## Land Pattern for SOD Components

### Information

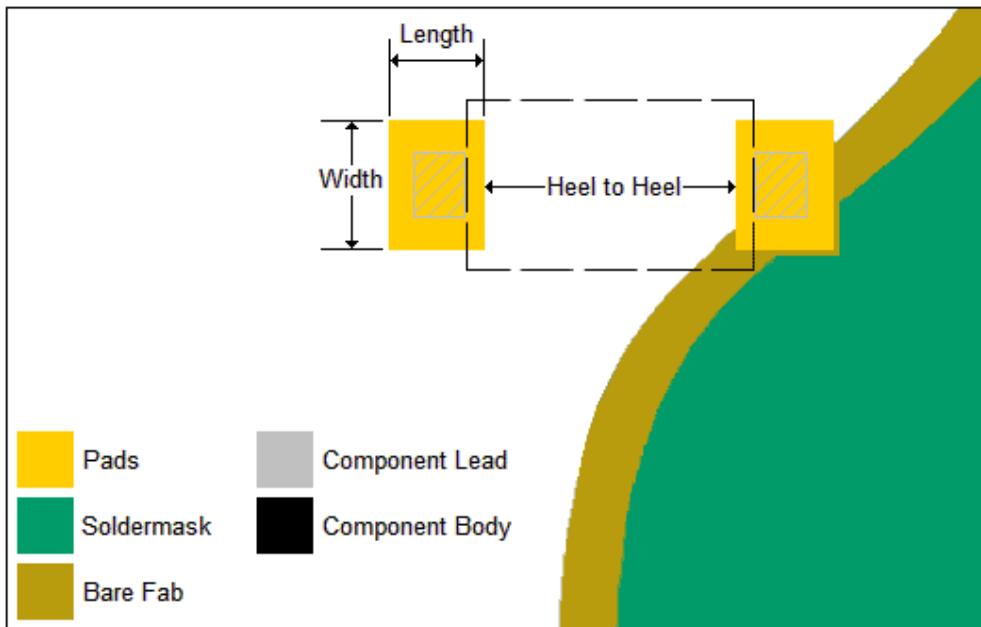
CID: 2

Content Owner: Jabil

Content Type: Information

Land pattern dimensions for [SOD](#) components.

| Package | Width    | Length   | Heel to Heel |
|---------|----------|----------|--------------|
| SOD123  | 1.1000mm | 0.8000mm | 2.7000mm     |
| SOD323  | 0.8000mm | 0.7000mm | 1.6000mm     |
| SOD523  | 0.7000mm | 0.5000mm | 1.0000mm     |



DFM &gt; Component Land Pattern &gt; SMT

Entry ID: 1384

## Land Pattern for QFP Components

### Information

CID: 2

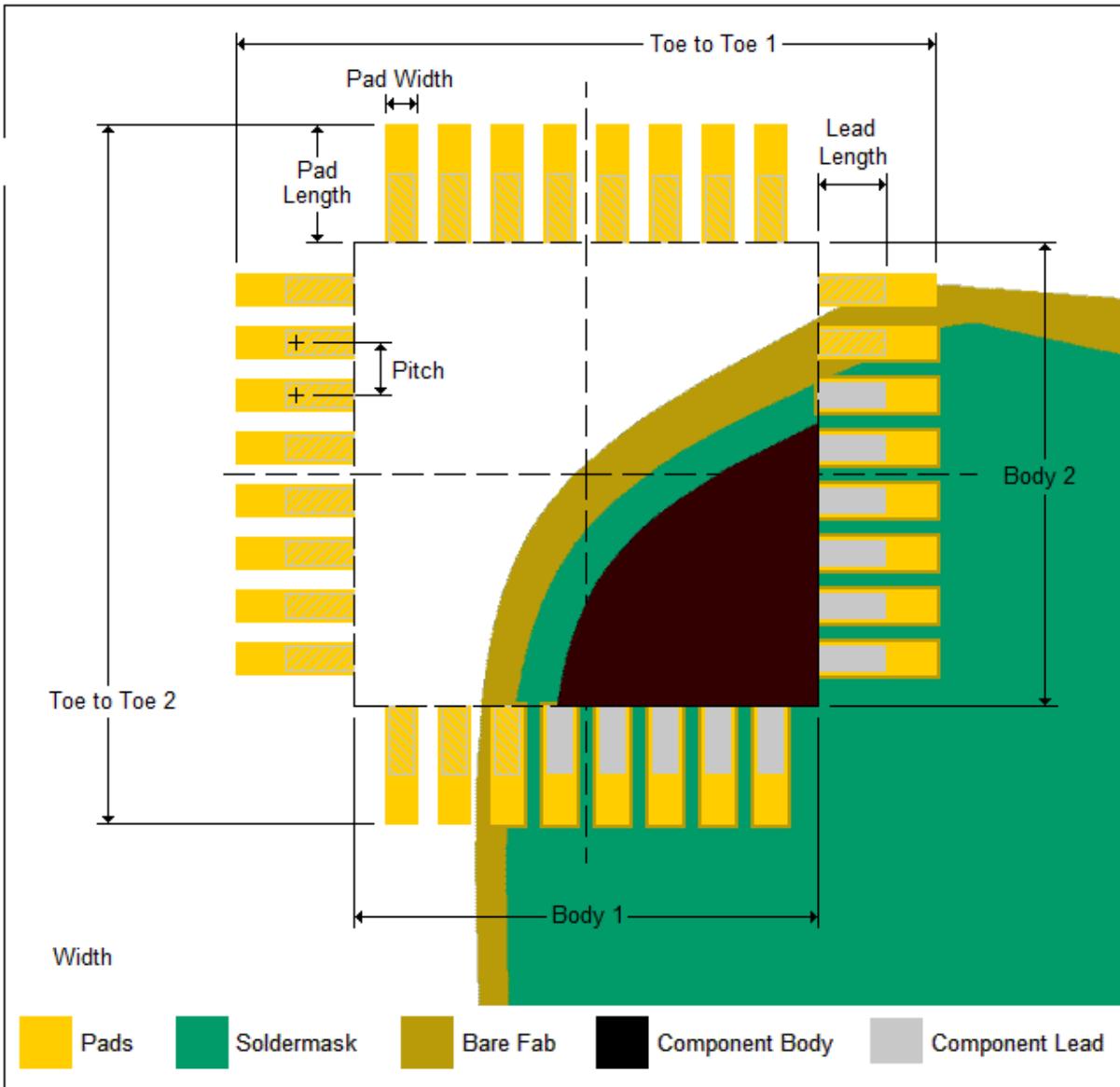
Content Owner: Jabil

Content Type: Information

Land pattern dimensions for [QFP](#) components.

| Component Lead Pitch | Pad Width |
|----------------------|-----------|
| 1.0000mm             | 0.6000mm  |
| 0.8000mm             | 0.5000mm  |
| 0.6500mm             | 0.4000mm  |
| 0.5000mm             | 0.2800mm  |
| 0.4000mm             | 0.2400mm  |

| Component |           | Pad         |              |              |            |
|-----------|-----------|-------------|--------------|--------------|------------|
| Body 1    | Body 2    | Lead Length | Toe to Toe 1 | Toe to Toe 2 | Pad Length |
| 5.5000mm  | 5.5000mm  | 1.0000mm    | 7.7000mm     | 7.7000mm     | 1.2000mm   |
| 7.5000mm  | 7.5000mm  | 1.0000mm    | 9.7000mm     | 9.7000mm     | 1.200mm    |
| 10.5000mm | 10.5000mm | 1.0000mm    | 12.7000mm    | 12.7000mm    | 1.200mm    |
|           |           | 1.6000mm    | 13.9000mm    | 13.9000mm    | 1.500mm    |
| 12.5000mm | 12.5000mm | 1.0000mm    | 14.7000mm    | 14.7000mm    | 1.200mm    |
|           |           | 1.6000mm    | 15.9000mm    | 15.9000mm    | 1.500mm    |
| 14.0000mm | 14.0000mm | 1.0000mm    | 16.7000mm    | 16.7000mm    | 1.200mm    |
|           |           | 1.6000mm    | 17.9000mm    | 17.9000mm    | 1.500mm    |
|           |           | 2.3000mm    | 19.3000mm    | 19.3000mm    | 2.200mm    |
|           |           | 3.1000mm    | 20.9000mm    | 20.9000mm    | 2.700mm    |
| 20.5000mm | 14.5000mm | 1.6000mm    | 23.9000mm    | 17.9000mm    | 1.500mm    |
|           |           | 2.3000mm    | 25.3000mm    | 19.3000mm    | 2.200mm    |
|           |           | 3.1000mm    | 26.9000mm    | 20.9000mm    | 2.700mm    |
| 20.5000mm | 20.5000mm | 1.0000mm    | 22.7000mm    | 22.7000mm    | 1.200mm    |
|           |           | 1.6000mm    | 23.9000mm    | 23.9000mm    | 1.500mm    |
| 24.5000mm | 24.5000mm | 1.0000mm    | 26.7000mm    | 26.7000mm    | 1.200mm    |
|           |           | 1.3000mm    | 27.3000mm    | 27.3000mm    | 1.200mm    |
| 28.5000mm | 28.5000mm | 1.0000mm    | 30.7000mm    | 30.7000mm    | 1.200mm    |
|           |           | 1.3000mm    | 31.3000mm    | 31.3000mm    | 1.200mm    |
|           |           | 1.6000mm    | 31.9000mm    | 31.9000mm    | 1.500mm    |
|           |           | 2.3000mm    | 33.3000mm    | 33.3000mm    | 2.200mm    |
| 28.5000mm | 40.0000mm | 1.3000mm    | 31.3000mm    | 43.3000mm    | 1.200mm    |
| 32.5000mm | 32.5000mm | 1.3000mm    | 35.3000mm    | 35.3000mm    | 1.200mm    |
|           |           | 1.6000mm    | 35.9000mm    | 35.9000mm    | 1.500mm    |
| 36.5000mm | 36.5000mm | 1.3000mm    | 39.3000mm    | 39.3000mm    | 1.200mm    |
| 40.0000mm | 40.0000mm | 1.3000mm    | 43.3000mm    | 43.3000mm    | 1.200mm    |
|           |           | 1.6000mm    | 43.9000mm    | 43.9000mm    | 1.500mm    |



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DFM > Component Land Pattern > SMT

Entry ID: 1385

## Land Patterns for BGA Components

### Information

CID: 1

Content Owner: Jabil

Content Type: Information

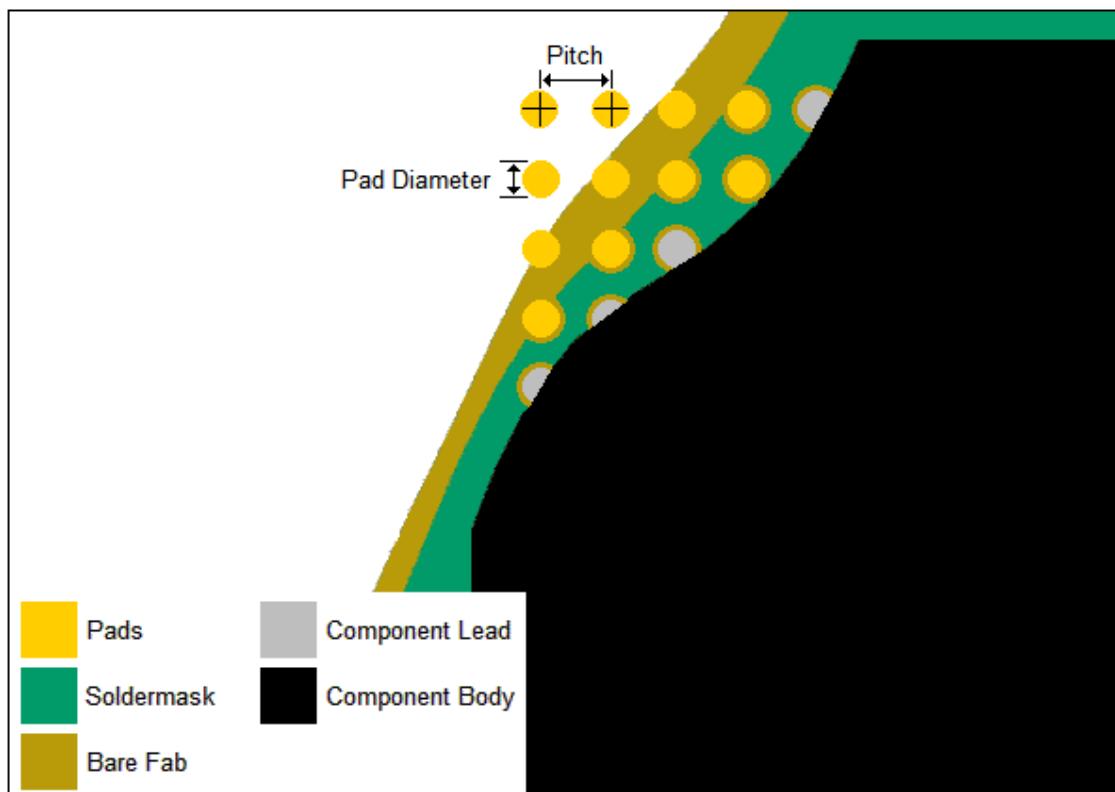
The **BGA** land pattern matrix includes **pad** and **stencil** recommendations by land pattern.

Metal defined pads are recommended for all land patterns.

**BGA Land Pattern Matrix** [File is located in the "File Attachments" folder.]

Refer to the following entries for additional related requirements:

- [Entry 1031](#) for copper to copper spacing
- [Entry 1032](#) for soldermask
- [Entry 1053](#) for via-in-pad
- [Entry 1054](#) for vias
- [Entry 1074](#) for BGA pads and **trace** connections



### Related Entries

DFM Guideline [1031](#) PCB Design > Traces > Trace Width and Copper to Copper Spacing

DFM Rule [1032](#) PCB Design > Soldermask > Soldermask

DFM Rule 1053 PCB Design > Vias > Through Hole Via-in-Pad for Surface Mount Components

DFM Guideline 1054 PCB Design > Vias > Vias and Micro-Vias

DFM Rule 1074 PCB Design > General > BGA Pads and Trace Connections

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## Land Pattern for Electrolytic Components

### Information

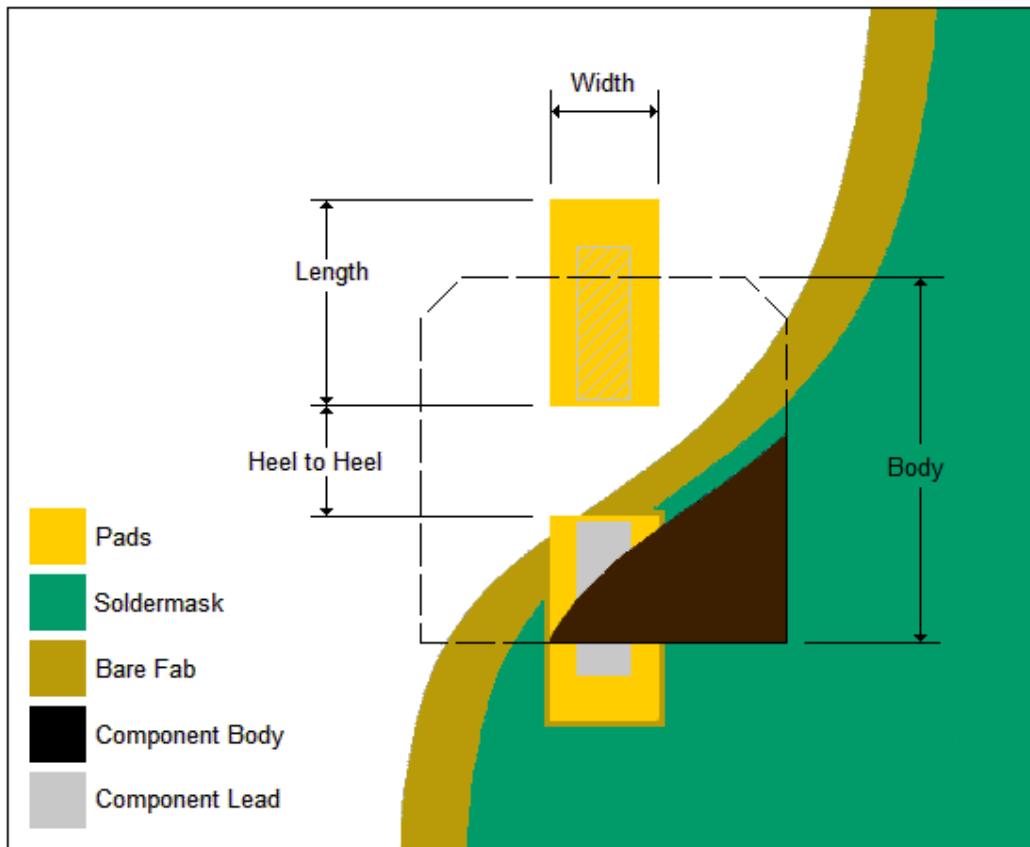
CID: 2

Content Owner: Jabil

Content Type: Information

Land pattern dimensions for electrolytic components.

| Component | Land Pattern Dimensions |          |              |
|-----------|-------------------------|----------|--------------|
| Body      | Width                   | Length   | Heel to Heel |
| 3.9000mm  | 1.5000mm                | 2.3000mm | 0.8000mm     |
| 4.9000mm  | 1.5000mm                | 2.8500mm | 0.8000mm     |
| 5.9000mm  | 1.5000mm                | 3.2500mm | 1.0000mm     |
| 7.5000mm  | 1.6000mm                | 3.6500mm | 1.5000mm     |
| 7.2000mm  | 1.4000mm                | 3.7000mm | 1.5000mm     |
| 9.3000mm  | 1.8000mm                | 4.5000mm | 1.5000mm     |
| 9.3000mm  | 1.9000mm                | 8.6000mm | 2.3000mm     |
| 11.4000mm | 1.9000mm                | 4.5500mm | 3.8000mm     |



## Land Pattern for PLCC Components

### Information

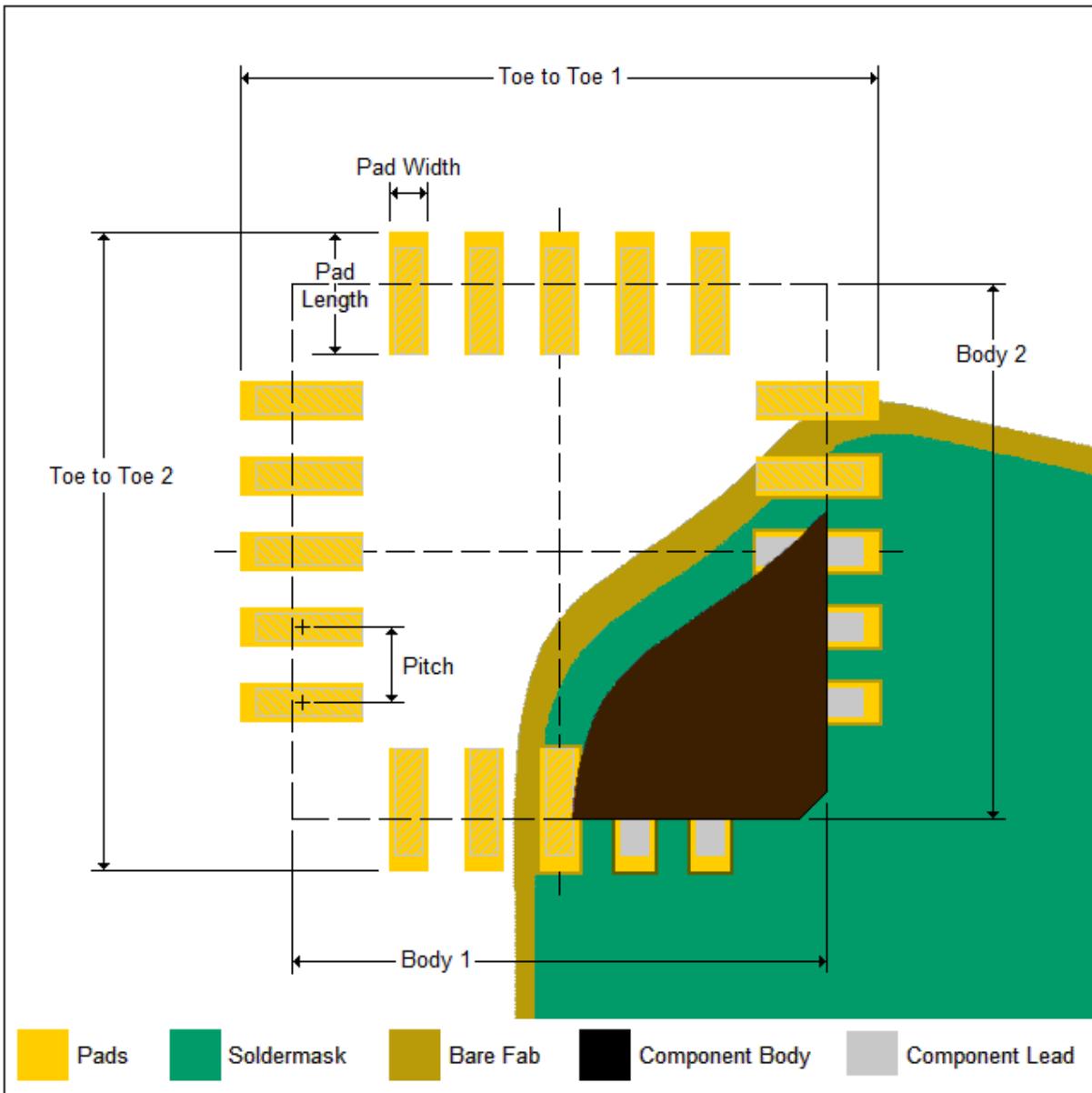
|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 2 | Content Owner: Jabil | Content Type: Information |
|--------|----------------------|---------------------------|

PLCC component land pattern dimensions for lead pitch of 1.2700mm.

Notes:

- Maximum component lead width = 0.5330mm
- Pad width for all defined patterns = 0.7000mm
- Lead count in the below table shows total number of leads on top with (side 1 – side 2) lead count below.

| Component    |              |                  | Pad          |              |            |
|--------------|--------------|------------------|--------------|--------------|------------|
| Body 1 (max) | Body 2 (max) | Lead Count       | Toe to Toe 1 | Toe to Toe 2 | Pad Length |
| 7.5700mm     | 11.1200mm    | 18<br>(4 - 5)    | 11.0000mm    | 14.5000mm    | 3.2500mm   |
| 7.7000mm     | 12.7800mm    | 18<br>(4 - 5)    | 11.2000mm    | 16.2000mm    | 3.3500mm   |
| 9.3000mm     | 9.3000mm     | 20<br>(5 - 5)    | 12.7000mm    | 12.7000mm    | 3.2500mm   |
| 7.7000mm     | 12.7800mm    | 22<br>(4 - 7)    | 11.2000mm    | 16.2000mm    | 3.3500mm   |
| 9.2200mm     | 14.300mm     | 28<br>(5 - 9)    | 12.7000mm    | 17.8000mm    | 3.3000mm   |
| 11.8400mm    | 11.8400mm    | 28<br>(7 - 7)    | 15.2000mm    | 15.2000mm    | 3.2500mm   |
| 11.7600mm    | 14.3000mm    | 32<br>(7 - 9)    | 15.2000mm    | 17.8000mm    | 3.3000mm   |
| 16.9200mm    | 16.9200mm    | 44<br>(11 - 11)  | 20.3000mm    | 20.3000mm    | 3.2500mm   |
| 19.4600mm    | 19.4600mm    | 52<br>(13 - 13)  | 22.8000mm    | 22.8000mm    | 3.2500mm   |
| 24.5900mm    | 24.5900mm    | 68<br>(17 - 17)  | 27.9000mm    | 27.9000mm    | 3.2500mm   |
| 29.6700mm    | 29.6700mm    | 84<br>(21 - 21)  | 33.0000mm    | 33.0000mm    | 3.2500mm   |
| 34.7500mm    | 34.7500mm    | 100<br>(25 - 25) | 38.1000mm    | 38.1000mm    | 3.2500mm   |
| 42.3700mm    | 42.3700mm    | 124<br>(31 - 31) | 45.7000mm    | 45.7000mm    | 3.2500mm   |



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## Land Pattern for Large SOIC Components

### Information

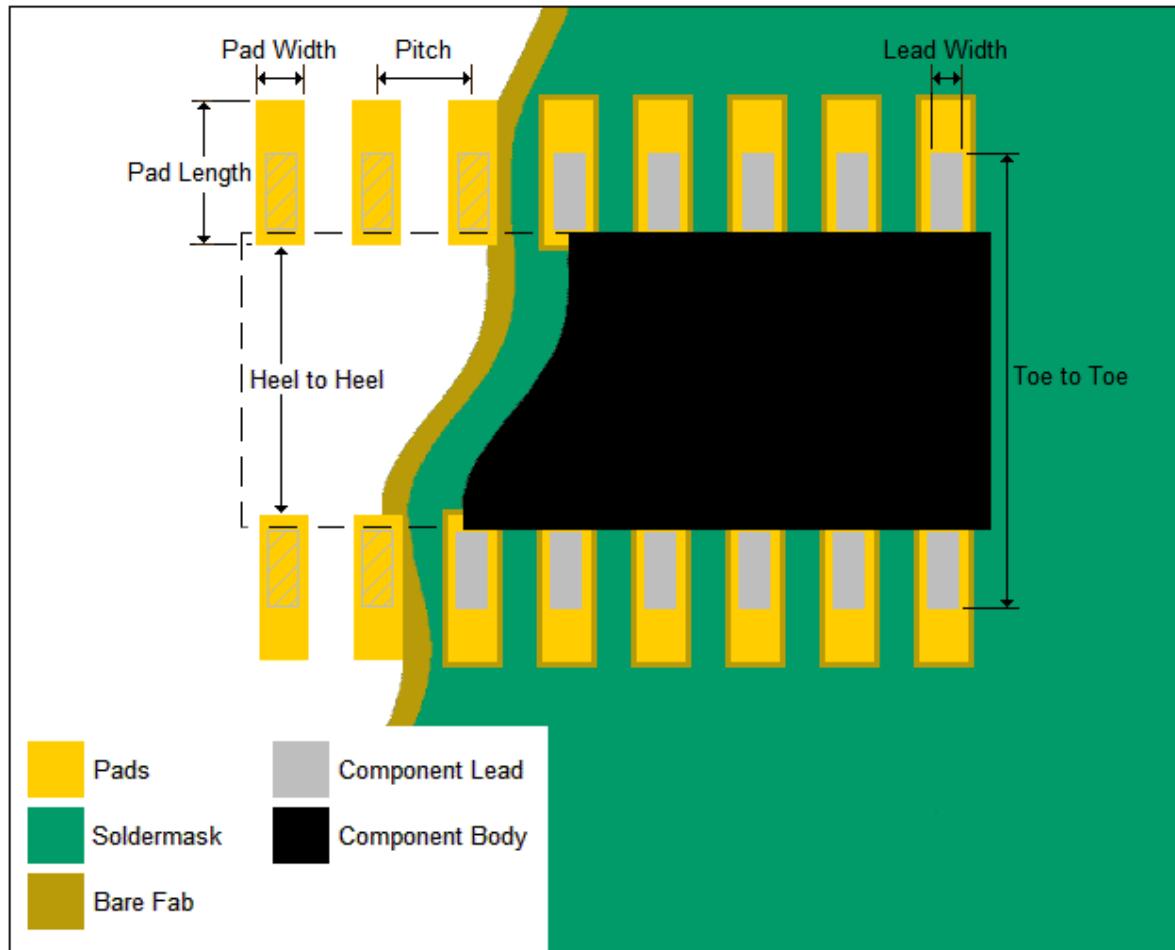
CID: 2

Content Owner: Jabil

Content Type: Information

Large SOIC component land pattern dimensions with lead pitch of 1.2700mm.

| Component      |                | Pad Definition |          |          |
|----------------|----------------|----------------|----------|----------|
| Toe to Toe Max | Lead Width Max | Heel to Heel   | Width    | Length   |
| 6.9900mm       | 0.5100mm       | 3.9000mm       | 0.7000mm | 1.7500mm |
| 8.8900mm       | 0.5100mm       | 5.1000mm       | 0.7000mm | 2.1000mm |
| 10.800mm       | 0.5100mm       | 6.4000mm       | 0.7000mm | 2.4000mm |
| 12.7000mm      | 0.5100mm       | 8.3000mm       | 0.7000mm | 2.4000mm |
| 14.6100mm      | 0.5100mm       | 10.3000mm      | 0.7000mm | 2.3500mm |
| 16.5100mm      | 0.5100mm       | 12.2000mm      | 0.7000mm | 2.3500mm |



### Related Entries

DFM Information [1389](#) Component Land Pattern > SMT > Land Pattern for Small SOIC Components

## Land Pattern for Small SOIC Components

### Information

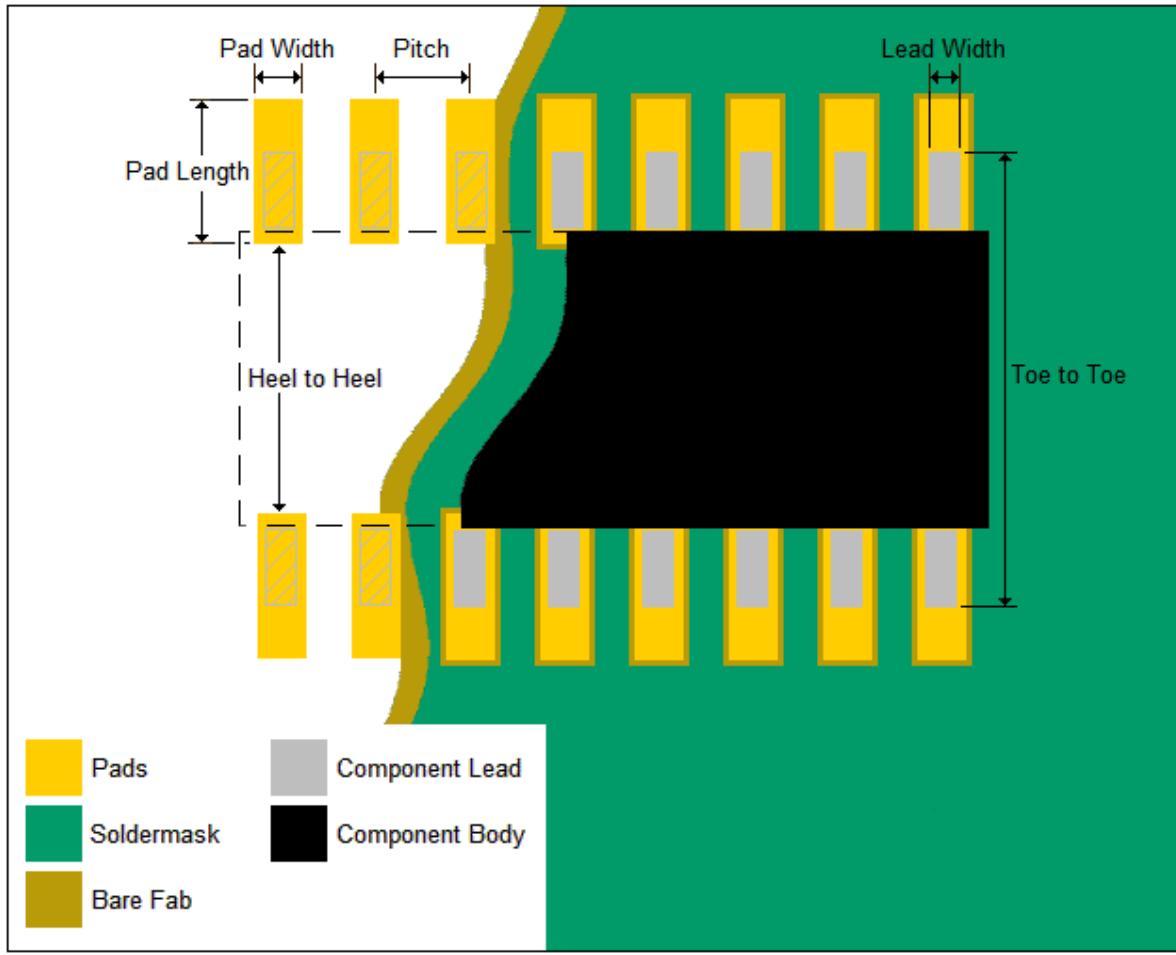
CID: 2

Content Owner: Jabil

Content Type: Information

Small SOIC component land pattern dimensions with lead pitch of 1.2700mm.

| Component      |                | Pad Definition |          |          |
|----------------|----------------|----------------|----------|----------|
| Toe to Toe Max | Lead Width Max | Heel to Heel   | Width    | Length   |
| 6.9900mm       | 0.5100mm       | 3.9000mm       | 0.7000mm | 1.7500mm |
| 8.8900mm       | 0.5100mm       | 5.1000mm       | 0.7000mm | 2.1000mm |
| 10.800mm       | 0.5100mm       | 6.4000mm       | 0.7000mm | 2.4000mm |



### Related Entries

[DFM Information 1388 Component Land Pattern > SMT > Land Pattern for Large SOIC Components](#)

## Land Pattern for SOT Components

### Information

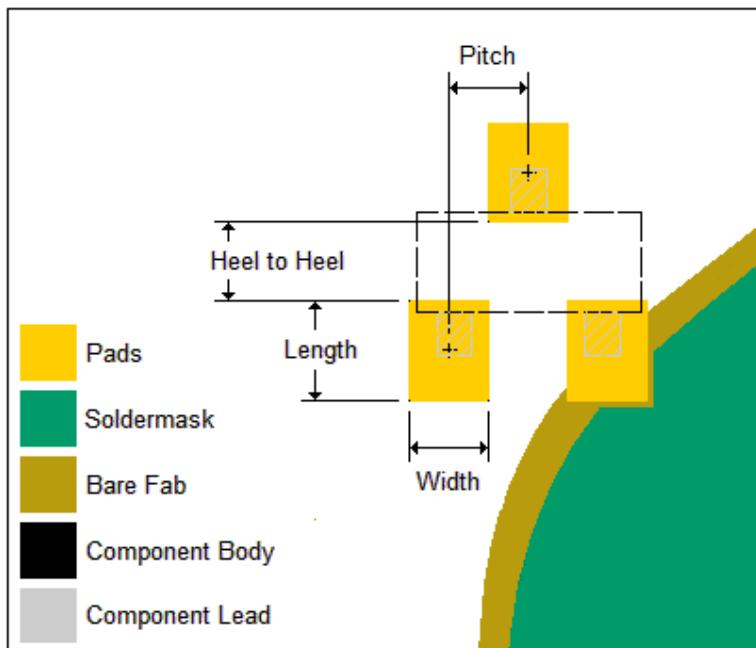
CID: 2

Content Owner: Jabil

Content Type: Information

Land pattern dimensions for [SOT](#) components.

| Component | Pitch    | Heel to Heel | Width    | Length   |
|-----------|----------|--------------|----------|----------|
| SOT23     | 0.9500mm | 1.3000mm     | 0.9000mm | 1.0000mm |
| SOT323    | 0.6500mm | 1.3000mm     | 0.8000mm | 0.6000mm |



DFM > Component Land Pattern > SMT

Entry ID: 1778

## Enlarged SMT Pads

### Guideline

CID: 2

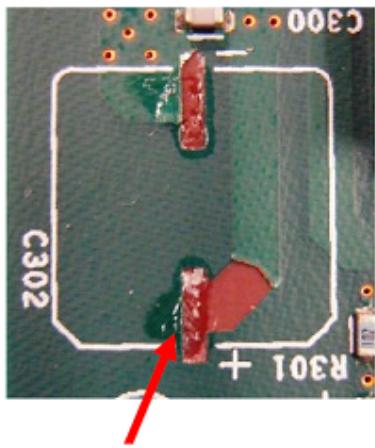
Content Owner: Jabil

Content Type: Requirement

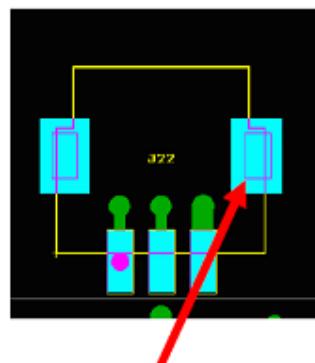
Copper peel strength varies from **PCB** material. Peel strength may be affected by dielectric thickness, copper thickness, number of **reflow** cycles, reflow temperatures, etc.

For large **SMT** components with small **pin** contact surfaces, enlarge copper **pads** and utilize **soldermask** defined pads.

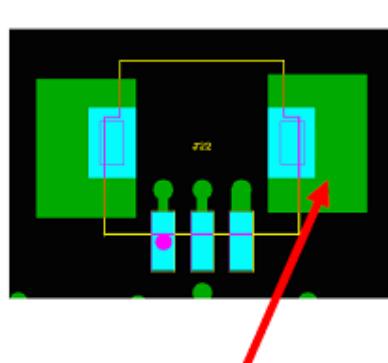
- Increasing the amount of copper attached to the PCB will improve the peel strength, resulting in a lower chance of the component being ripped off of the PCB.



Component Ripped off the PCB



Standard Pad  
Copper 1.7500mm x 2.8000mm



Enlarged Pad  
Copper 4.0500mm x 5.5750mm

Components to consider for enlarged pads include electrolytic capacitors, SMT headers, SMT connectors, and SMT test loops.



DFM > Component Land Pattern > SMT

Entry ID: 1838

## Wave Solder Land Patterns

### Information

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 1 | Content Owner: Jabil | Content Type: Information |
|--------|----------------------|---------------------------|

See [Entry 1000](#) for the list of [component types](#) that are allowed to be in exposed [wave solder areas](#) on the [secondary side](#).

When designing land patterns that will be located in exposed wave solder areas on the secondary side, follow this [ECAD Design \[File is located in the "File Attachments" folder.\]](#) document.

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DFM > Component Placement > Location

Entry ID: 1000

## Component to Component Spacing

### Rule

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 2 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Observe the minimum component to component spacing requirements that are shown in the Component Spacing table [Spacing table is in a separate extract file].

- Components too close to each other can cause issues with placement, soldering and repair.
- This can add cost, reduce throughput and negatively impact quality.

|         |                      |                           |
|---------|----------------------|---------------------------|
| CID: 10 | Content Owner: Jabil | Content Type: Requirement |
|---------|----------------------|---------------------------|

Do not place the following incompatible components in exposed wave solder areas on the secondary side:

axial, BGA fine pitch, BGA standard pitch, connector press fit, connector PTH, connector SMT, DIP, discrete 01005, discrete 0201, discrete 0402, discrete tall, flip chip, MELF, network, PLCC, printed, PTH covering, PTH miscellaneous short, PTH miscellaneous tall, QFN Cwrap, QFN leadless, QFP fine pitch, QFP standard pitch, radial, SMT covering, SMT miscellaneous tall, SOIC fine pitch.

- This can cause quality issues and / or special processing requirements that add cost.

The following components are allowed in exposed wave solder areas on the secondary side:

- discrete 0603, discrete 0805, discrete other, SMT miscellaneous short, SOIC standard pitch, SOT, tantalum.

|         |                      |                           |
|---------|----------------------|---------------------------|
| CID: 11 | Content Owner: Jabil | Content Type: Requirement |
|---------|----------------------|---------------------------|

Do not select fine pitch BGAs, flip chips, discrete 01005 or discrete 0201 components.

- These component types are not compatible with this product class.

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 4 | Content Owner: Jabil | Content Type: Information |
|--------|----------------------|---------------------------|

### Spacing Table Structure

In addition to component types: the spacing table structure is further defined by spacing type (body to body, body to pad, or pad to pad), [product classification](#) and process area ([reflow](#) or [wave](#)).

### Component Orientation

Each component pair has spacing values for four different component orientations.

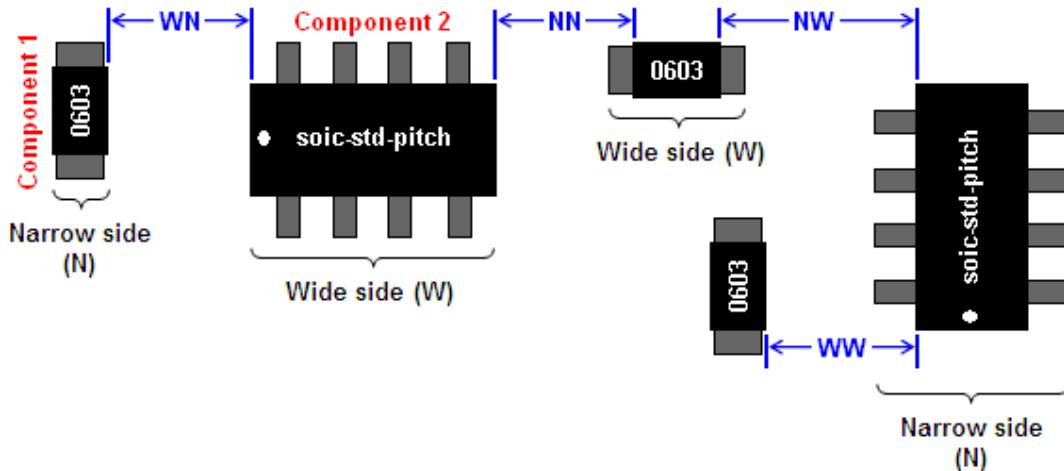
- NN** - Narrow side of component 1 to narrow side of component 2
- NW** - Narrow side of component 1 to wide side of component 2
- WN** - Wide side of component 1 to narrow side of component 2
- WW** - Wide side of component 1 to wide side of component 2

Component pairs are listed in alphabetic order. For example, the spacing table contains axial to sot, but it does not contain duplicate values for sot to axial.

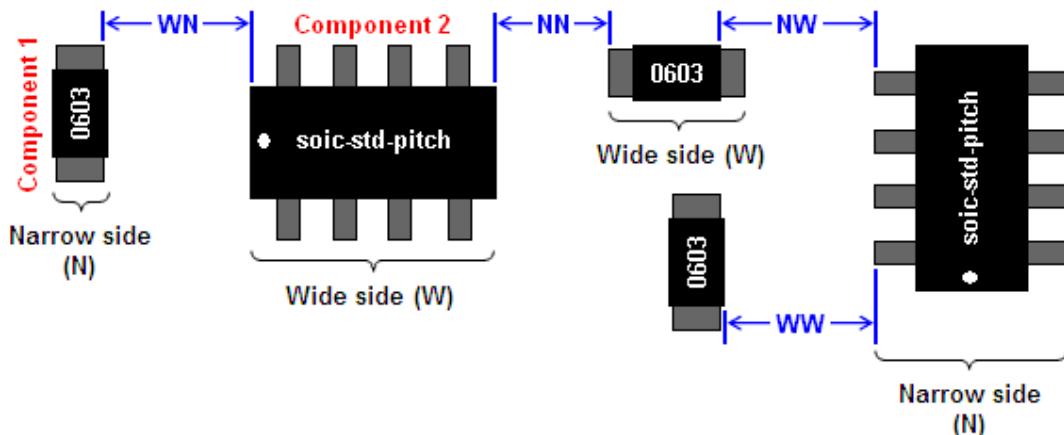
**Note:** All component graphics are a relative representation of a component shape and may not be representative of the actual component under review (ie. SMT Misc, Crystal, SMT Misc Tall). Utilize [CAD](#) and Part Manufacturer data sheets as necessary.

Narrow and wide are determined by the component body dimensions.

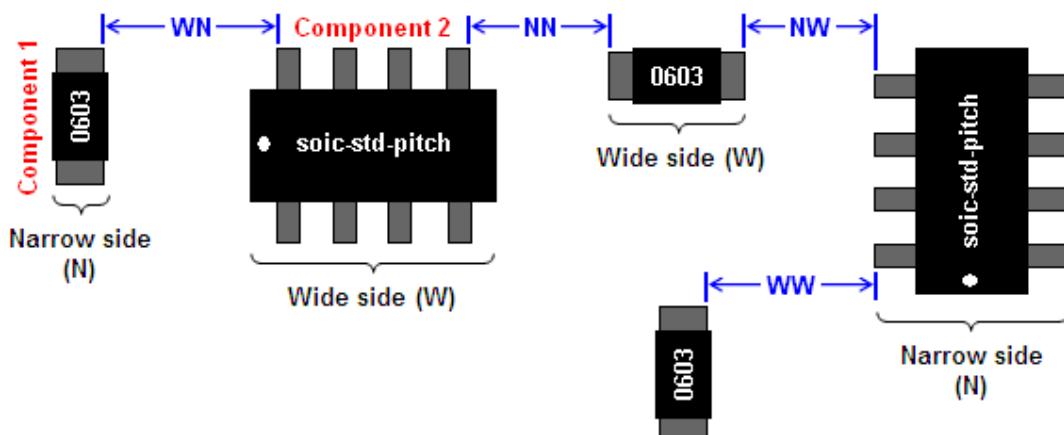
Body to Body Spacing Example:



Body to Pad Spacing Example:



Pad to Pad Spacing Example:



Related Entries

DFM Guideline [1117](#) Component Selection > Through Hole Mount > Lead Length Protrusion for THMT Soldering

DFM Guideline [1009](#) Component Placement > Location > THMT Components Requiring Wave Solder

DFM Guideline [1112](#) Component Selection > Surface Mount > Ceramic Capacitors in the Wave Solder

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DFM &gt; Component Placement &gt; Location

Entry ID: 1001

## Component to PCB Edge Clearance

### Rule

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 2 | Content Owner: Jabil | Content Type: Information |
|--------|----------------------|---------------------------|

These are minimum requirements for the automated assembly equipment ([SMT](#), [wave solder](#), etc).

|         |                      |                           |
|---------|----------------------|---------------------------|
| CID: 11 | Content Owner: Jabil | Content Type: Requirement |
|---------|----------------------|---------------------------|

Minimum distance to conveyed [PCB](#) edges.

| Minimum distance from                                 | Reference point  | Primary side & secondary side keep-out |
|---|------------------|--|
| SMT components  | Pad edge or body | 5.0000mm                               |
| <a href="#">BGA &amp; fine pitch components</a>       | Pad edge or body | 10.0000mm                              |
| <a href="#">THMT auto-inserted and PTH components</a> | Pad edge or body | 6.0000mm                               |
| <a href="#">Press fit components</a>                  | Pad edge         | 5.0000mm                               |
| Press fit components                                  | Body             | 0.0000mm (zero value)                  |
| PTH connectors  | Pad edge         | 5.0000mm                               |
| PTH connectors  | Body             | 0.0000mm (zero value)                  |

SMT component clearances are driven by the PCB resting on the rails as it travels down the conveyors in the automated assembly equipment. In addition, if SMT components are too close to the conveyed edge the solderpaste stencil may not make good contact with the PCB resulting in apertures too close to the edge having paste volumes up to 250% of normal resulting in solder shorts and potential opens with small apertures.

Additional clearance for BGA & fine pitch components is necessary to prevent [solderpaste](#) printing issues.

[THMT](#) auto-inserted component clearance is generally driven by the clinch mechanisms on the secondary side of the PCB.

Press fit component bodies can be even with or overhang the PCB edge but the pad edge must maintain spacing to allow the anvil to support the component during the press process.

Non-auto inserted PTH component clearance is driven by the pallet or conveyor fingers the PCB rests on as it travels through the wave solder.

PTH connector bodies can be even with the PCB edge but the pad edge clearance is driven by the pallet or conveyor fingers the PCB rests on as it travels through the wave solder.

|         |                      |                           |
|---------|----------------------|---------------------------|
| CID: 13 | Content Owner: Jabil | Content Type: Requirement |
|---------|----------------------|---------------------------|

Minimum distance to [non-conveyed PCB](#) edges.

| Minimum distance from            | Reference point  | Primary & secondary side keep-out |
|----------------------------------|------------------|-----------------------------------|
| SMT components                   | Pad edge         | 1.0000mm                          |
| SMT components                   | Body             | 0.3000mm                          |
| BGA & fine pitch components      | Pad edge or body | 5.0000mm                          |
| THMT auto-inserted components    | Pad edge         | 1.0000mm                          |
| THMT auto-inserted components    | Body             | 0.5000mm                          |
| Press fit components             | Pad edge         | 5.0000mm                          |
| Press fit components             | Body             | 0.0000mm (zero value)             |
| Non-auto inserted PTH components | Pad edge         | 1.0000mm                          |
| Non-auto inserted PTH components | Body             | 0.3000mm                          |

| Minimum distance from | Reference point | Primary & secondary side keep-out |
|-----------------------|-----------------|-----------------------------------|
| PTH connectors        | Pad edge        | 1.0000mm                          |
| PTH connectors        | Body            | 0.0000mm (zero value)             |

Additional clearance for BGA & fine pitch components is necessary to prevent solderpaste printing issues.

Press fit component bodies can be even with or overhang the PCB edge but the pad edge must maintain spacing to allow anvil to support component during the press process.

Non-auto inserted PTH component clearance is driven by the pallet as it travels through the wave solder.

PTH connector bodies can be even with the PCB edge but the pad edge clearance is driven by the pallet the PCB rests on as it travels through the wave solder.

PCBs that require stiffeners (solder dams) on the non-conveyed PCB edges as they pass through the wave solder machine may have larger clearance requirements.

## Related Entries

---

DFM Rule [1319](#) Component Placement > Location > Component to Scored Breakaway (V-Score) PCB Edge Clearance

DFM Rule [1320](#) Component Placement > Location > Component to Drilled Breakaway (Mouse Bite) PCB Edge Clearance

DFM Rule [1321](#) Component Placement > Location > Component to Solid Tab PCB Edge Clearance

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DFM > Component Placement > Location

Entry ID: 1007

## Heavy SMT Parts on One Side of the PCB

### Guideline

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 2 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

SMT parts placed on the bottom of a double-sided PCBA prior to second pass reflow are only held in place by surface tension of the solder joints. Heavy components may fall off the board during the second pass reflow and would require glue or manual processing. Heavy SMT parts should all be on one side of the PCBA.

The following formula may be used as a guide to determining if a component will fall off during a second pass reflow operation.

A ratio that evaluates the component's mass in relation to the lead contact surface area with the solderpaste is:

$$\text{(Weight of components (in grams)) / (Total lead contact surface area with the solderpaste (in square inches))}$$

Grams per square inch must be less than or equal to 30 for second-side mounting.

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DFM > Component Placement > Location

Entry ID: 1009

## THMT Components Requiring Wave Solder

### Guideline

CID: 2

Content Owner: Jabil

Content Type: Requirement

All THMT components requiring [wave solder](#) must be on the same side of the board to minimize assembly cost.

If needed, connectors placed on the opposite side should be [press fit](#) only as the area can be masked and the component manually inserted later.

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DFM > Component Placement > Location

Entry ID: 1080

## Tall Components and Test Access

### Guideline

CID: 3

Content Owner: Jabil

Content Type: Requirement

Components taller than 5.0000mm should not be placed on the test access side of the board where most or all of the test points typically reside.

- Components taller than 5.0000mm located on the test access side of the board may require additional fixture modifications and / or non-standard probes.

### Related Entries

DFM Rule [1099](#) Component Selection > General > Maximum Component Height

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DFM > Component Placement > Location

Entry ID: 1081

## PCB Support in a Test Fixture

### Guideline

CID: 3

Content Owner: Jabil

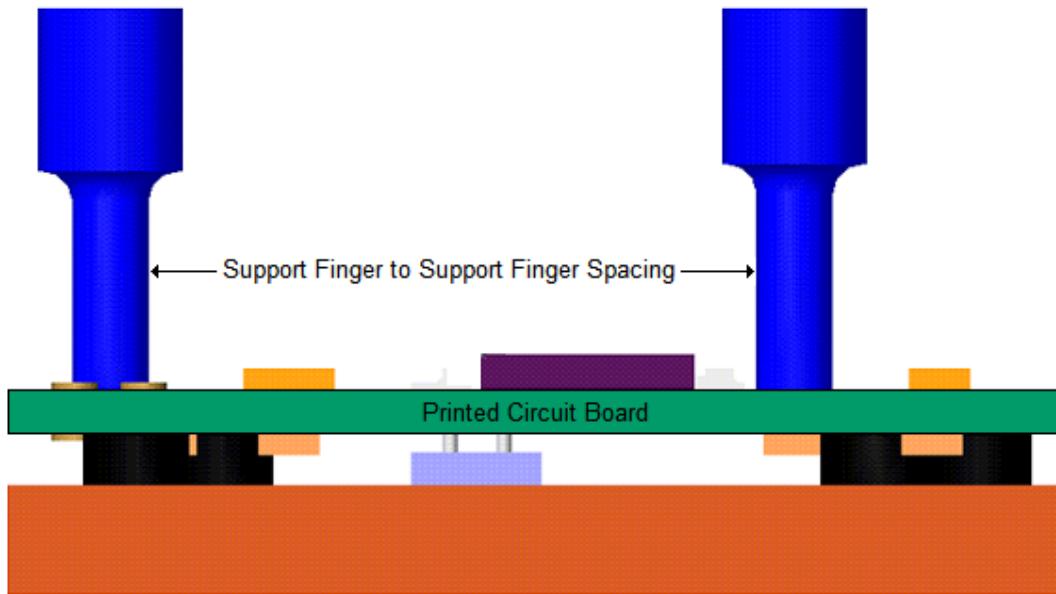
Content Type: Requirement

Minimum [test fixture support finger keep-out](#) area diameter = 6.3500mm

- Lack of a keep-out area could allow the fingers to make contact and damage components or solder joints.

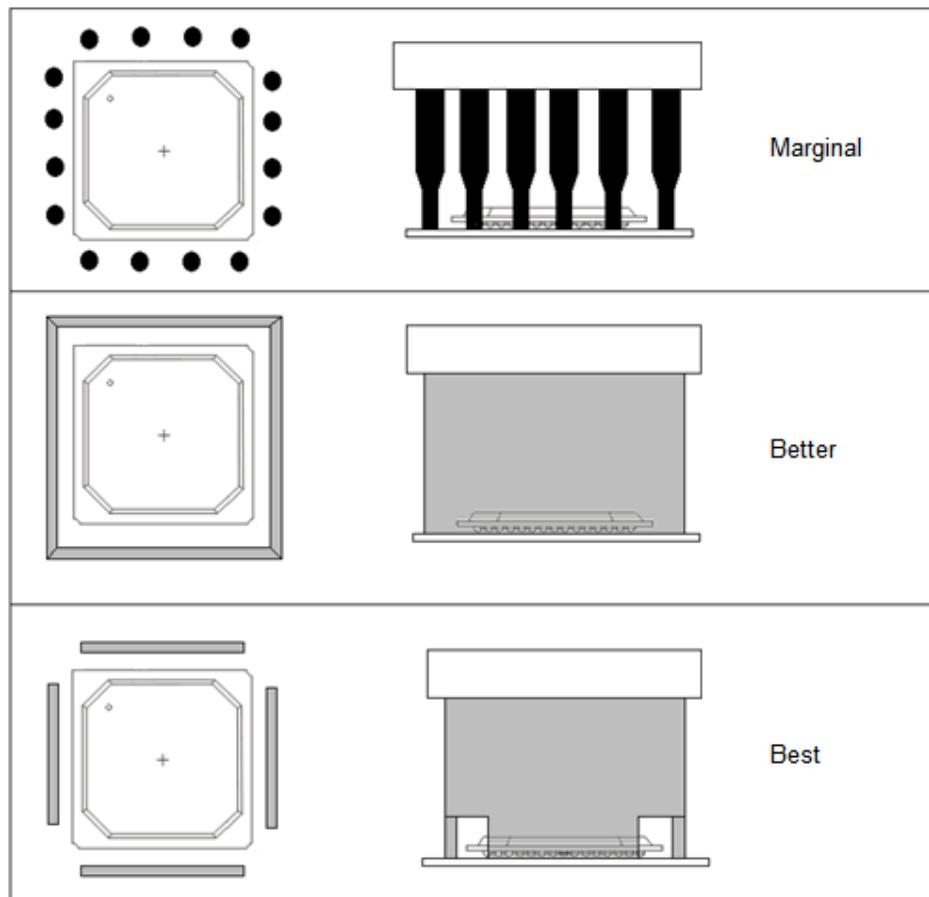
Provide test fixture support fingers every 50.8000mm or closer to maintain [PCB](#) coplanarity as dictated by probe density.

- Lack of support could cause strain on the PCB possibly damaging components or solder joints.



Provide perimeter support for [BGAs](#) opposite the test access side of an [ICT](#) fixture.

- BGAs need to be supported to counter the upward force of the test probes because it could cause strain on the solder joints and they are easily damaged.



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DFM > Component Placement > Location

Entry ID: 1319

## Component to Scored Breakaway (V-Score) PCB Edge Clearance

### Rule

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 2 | Content Owner: Jabil | Content Type: Information |
|--------|----------------------|---------------------------|

Scored breakaway (V-score) PCB edges may stress the [solder joints](#) or bodies of nearby components during the [depanel](#) process and require more clearance than typical component spacing. Tall components may interfere with the depanel process and require a greater [keep-out](#).

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 4 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Minimum scored breakaway (V-score) PCB edge to [MLCC](#) or [BGA](#) pad edge or body on primary & secondary side = 3.8000mm

- MLCC components that are too close may experience body cracking during the depanel process.
- The solder joints of nearby BGA components are especially susceptible to strain damage during the depanel process.

Minimum scored breakaway (V-score) PCB edge to fine pitch component pad edge or body on primary & secondary side = 2.0000mm

- The solder joints of nearby fine pitch components are especially susceptible to strain damage during the depanel process.

Minimum scored breakaway (V-score) PCB edge to press fit, PTH and SMT components 6.3500mm or taller pad edge or body on primary & secondary side = 1.5000mm

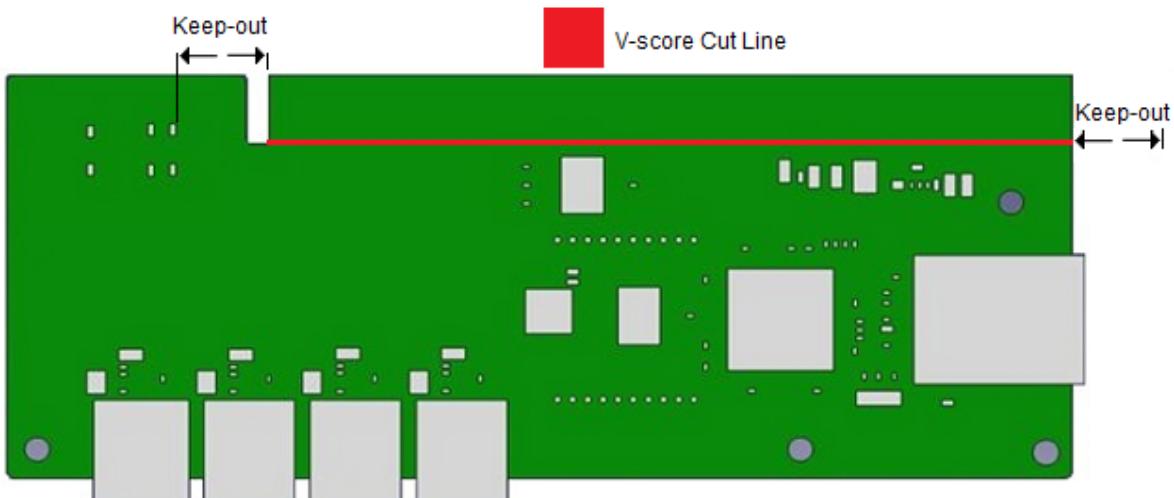
- The solder joints of nearby SMT and PTH components may experience strain damage during the depanel process.
- Tall components may interfere with the depanel process.

Minimum scored breakaway (V-score) PCB edge to SMT components shorter than 6.3500mm pad edge or body on primary & secondary side = 1.2500mm

- The solder joints of nearby SMT components may experience strain damage during the depanel process.

Minimum component keep-out area at the ends of V-score cut lines = 3.0000mm

- The cutting tool will continue beyond the end of the V-score cut line, so the component could be damaged and / or the V-score depanel process may not be possible.



Do not place overhanging components over V-score PCB edges.

- The component could be damaged and / or the V-score depanel process may not be possible.

Do not use a breakaway jig or hand breaking for the V-score depanel process.

- Studies have shown these processes can cause significant strain damage.
- If a breakaway jig or hand breaking process is necessary, a product specific validation study is highly recommended.

## Related Entries

---

[DFM Rule 1001 Component Placement > Location > Component to PCB Edge Clearance](#)

[DFM Rule 1320 Component Placement > Location > Component to Drilled Breakaway \(Mouse Bite\) PCB Edge Clearance](#)

[DFM Rule 1321 Component Placement > Location > Component to Solid Tab PCB Edge Clearance](#)

[DFM Rule 1043 PCB Design > Depanel > Scored Breakaway \(V-Score\) Depaneling](#)

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DFM > Component Placement > Location

Entry ID: 1320

## Component to Drilled Breakaway (Mouse Bite) PCB Edge Clearance

### Rule

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 3 | Content Owner: Jabil | Content Type: Information |
|--------|----------------------|---------------------------|

Drilled breakaway (mouse bite) PCB edges may stress the **solder joints** of nearby components during the **depanel** process and require more clearance than typical component spacing. Tall components may interfere with the depanel process and require a greater **keep-out**.

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 4 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Observe minimum component to drilled breakaway (mouse bite) PCB edge clearance requirements.

| Minimum distance from  | Reference point  | Primary Side & Secondary Side Keep-Out |
|--|------------------|--|
| SMT components   | Pad edge or body | 2.5000mm                               |
| BGA & Fine pitch components                                      | Pad edge or body | 8.0000mm                               |
| All (SMT, THMT Auto Insert, PTH) components $\geq$ 6.3500mm tall | Pad edge or body | 12.5000mm                              |
| THMT auto-inserted components                                    | Pad edge or body | 10.0000mm                              |
| Press fit components   | Pad edge or body | 2.0000mm                               |
| Non-auto inserted PTH components                                 | Pad edge         | 2.0000mm                               |

- The solder joints of nearby SMT components may experience strain damage during the depanel process.
- The solder joints of nearby BGA and fine pitch components are especially susceptible to strain damage during the depanel process.
- Tall components may interfere with the depanel process.
- Other components may experience strain during the depanel process.

### Related Entries

DFM Rule [1001](#) Component Placement > Location > Component to PCB Edge Clearance

DFM Rule [1319](#) Component Placement > Location > Component to Scored Breakaway (V-Score) PCB Edge Clearance

DFM Rule [1321](#) Component Placement > Location > Component to Solid Tab PCB Edge Clearance

DFM Rule [1038](#) PCB Design > Depanel > Drilled Breakaway (Mouse Bite) Depaneling

DFM > Component Placement > Location

Entry ID: 1321

## Component to Solid Tab PCB Edge Clearance

### Rule

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 3 | Content Owner: Jabil | Content Type: Information |
|--------|----------------------|---------------------------|

PCBs routed in-house can strain the **solder joints** of nearby **SMT** components, but it is the least damaging depanelization method and is preferred when placing components near the depanel edge. Tall components may interfere with the routing process and may require a greater **keep-out** based on the routing equipment.

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 5 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Minimum solid tab (in-house routed) PCB edge to component pad edge or body on primary & secondary side = 1.0000mm

- The solder joints of nearby components are susceptible to strain damage during the routing process.

Do not place overhanging components over solid tab (in-house routed) PCB edges.

- Overhanging components could make it difficult or impossible for the routing process.

### Related Entries

DFM Rule [1001](#) Component Placement > Location > Component to PCB Edge Clearance

DFM Rule [1319](#) Component Placement > Location > Component to Scored Breakaway (V-Score) PCB Edge Clearance

DFM Rule [1320](#) Component Placement > Location > Component to Drilled Breakaway (Mouse Bite) PCB Edge Clearance

DFM Rule [1035](#) PCB Design > Depanel > Solid Tab Depaneling

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DFM > Component Placement > Location

Entry ID: 1737

## Components Opposite X-ray Solder Joints

### Guideline

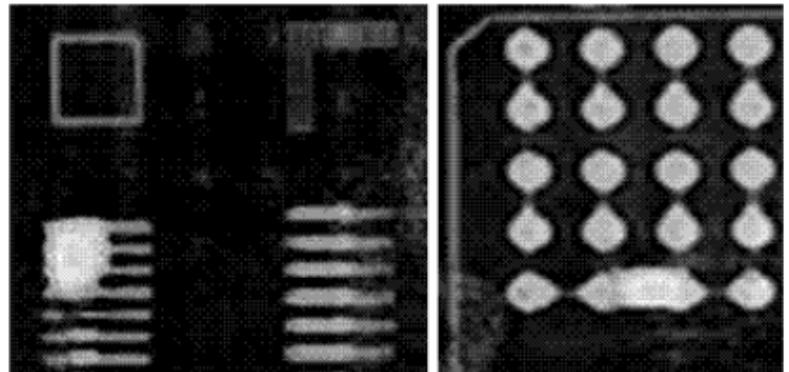
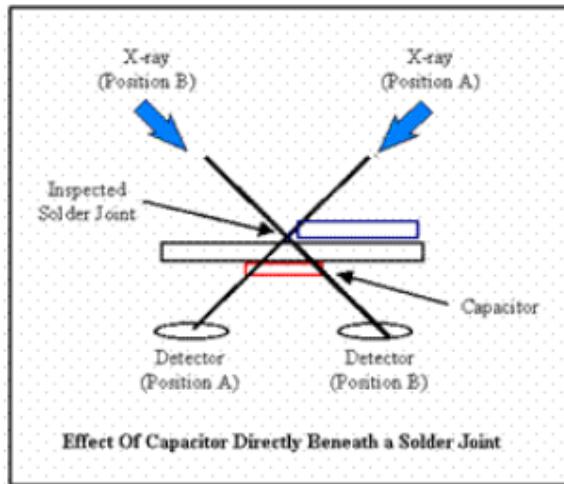
CID: 2

Content Owner: Jabil

Content Type: Requirement

Avoid placing capacitors, metal cased or other opaque (X-ray blocking) components directly opposite X-ray inspected solder joints.

- This will avoid attenuation or "shading" when viewing the solder joint, improving inspection coverage.



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DFM > Component Placement > Location

Entry ID: 1741

## Components in Flex Areas

### Guideline

CID: 2

Content Owner: Jabil

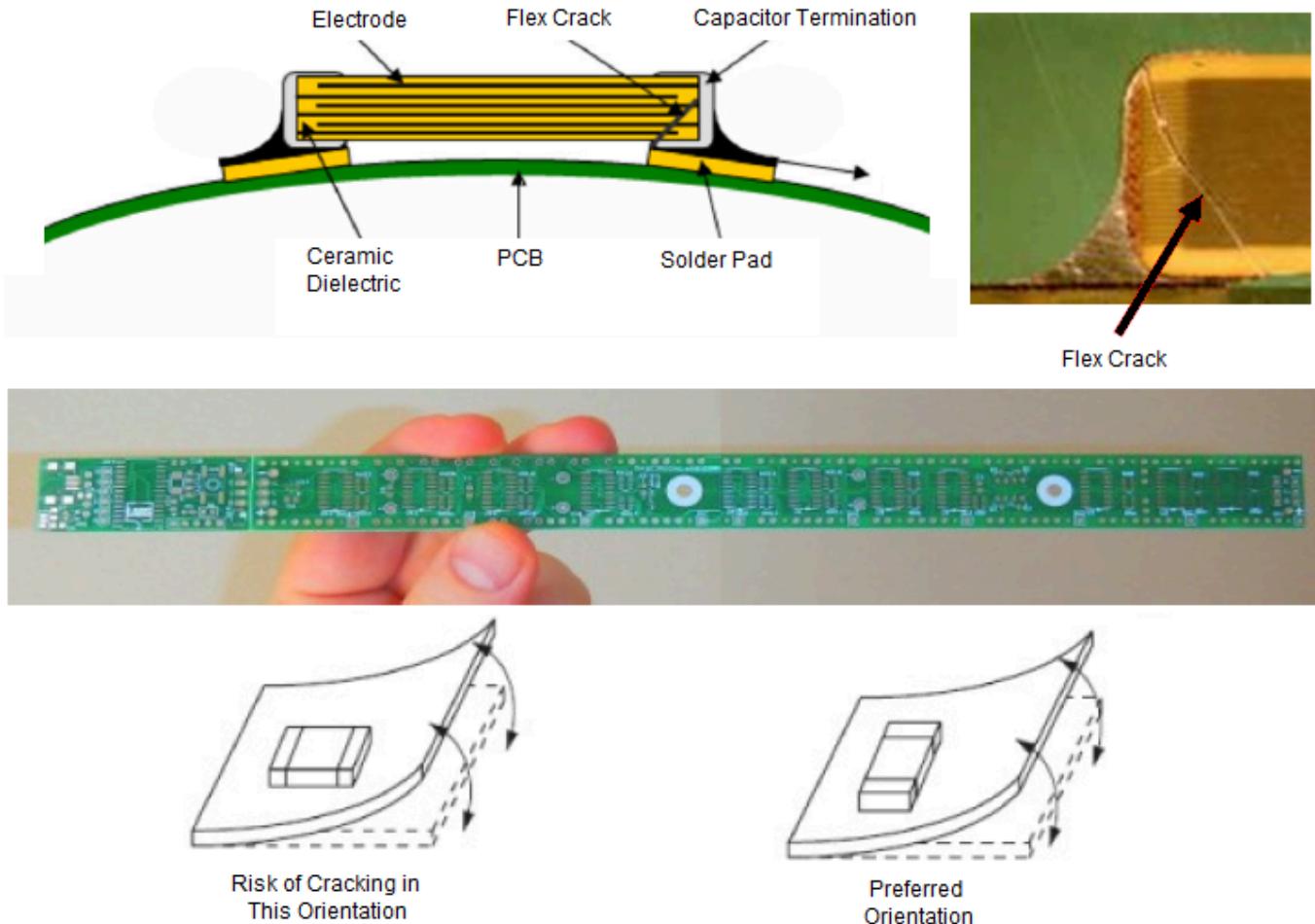
Content Type: Requirement

Avoid locating **BGAs** on bend lines / flex areas of the PCB.

- The solder joints of BGAs are susceptible to fracturing if they are located in areas such as between connectors and mounting holes that may flex during assembly.

Orient **discrete components** perpendicular to the long axis of long, thin PCBs.

- Long, thin PCBs tend to flex easily during handling and assembly processes.
- Discrete components are prone to cracking due to PCB flex and this orientation puts less stress on the component body.



DFM > Component Placement > Location

Entry ID: 1816

## Component Spacing Between Two Tall Components

### Guideline

CID: 2

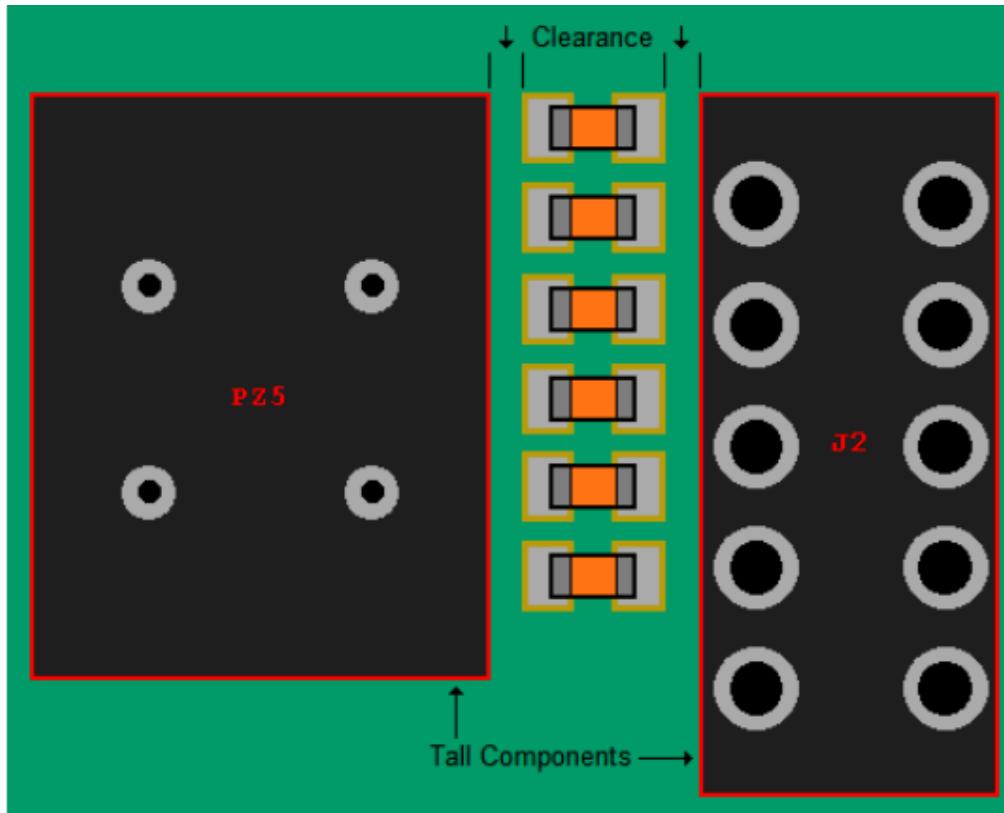
Content Owner: Jabil

Content Type: Requirement

SMT components located between two components 6.3500mm or taller (SMT or THMT), and whose pads are facing the tall components, require more clearance than typical component spacing.

Minimum distance from the pad of an SMT component between two adjacent components 6.3500mm or taller = height of the taller of the two components

- There may not be enough room for the soldering iron tip to access the SMT leads for repair / rework. The tall component will have to be removed before the middle component can be reworked.



### Related Entries

DFM Rule 1000 Component Placement > Location > Component to Component Spacing

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## Wave Solder Component Orientation

### Guideline

CID: 3

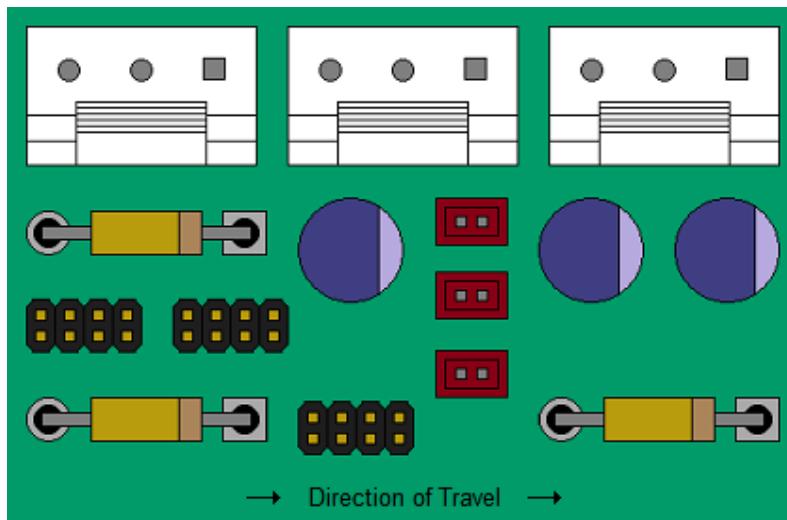
Content Owner: Jabil

Content Type: Requirement

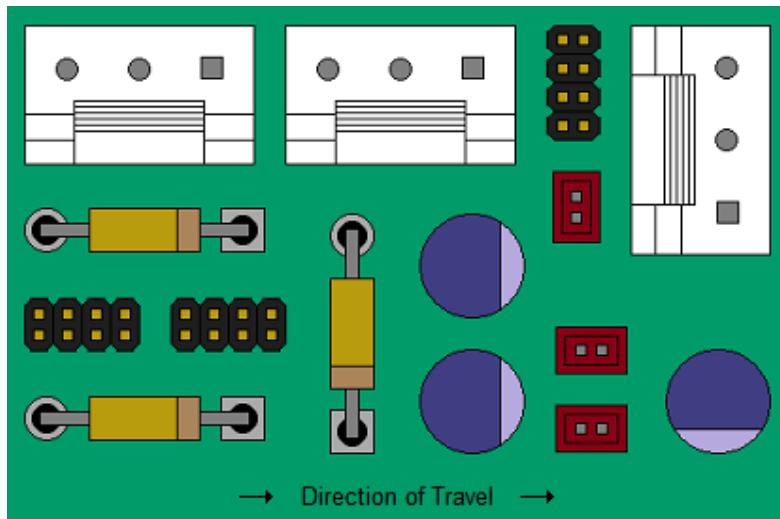
### For THMT components with round pads and a minimum pad to pad spacing of 0.7500mm or greater:

Ensure THMT components are all placed in a single orientation parallel to the [wave solder](#) process direction of travel.

- Inconsistent orientation will negatively affect assembly and inspection.



If necessary, a second orthogonal orientation perpendicular to the wave solder direction of travel is allowed.



CID: 2

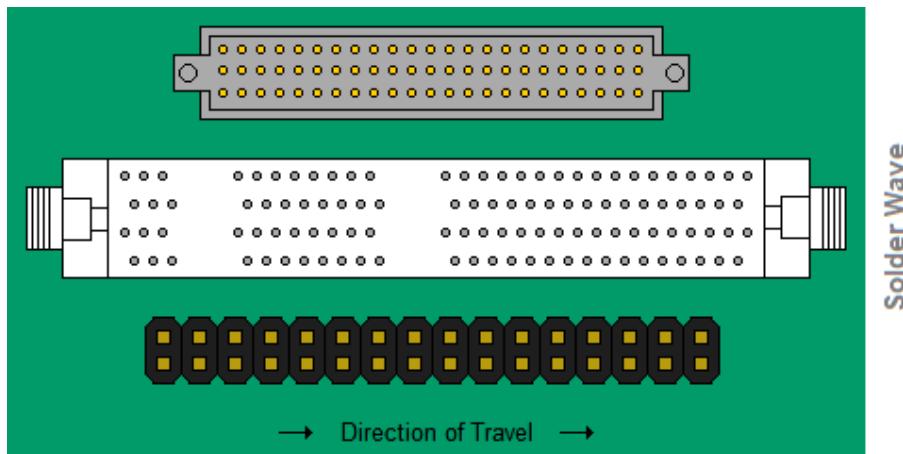
Content Owner: Jabil

Content Type: Requirement

### For THMT components with round pads and a minimum pad to pad spacing less than 0.7500mm:

Place THMT components in a single orientation parallel to the [wave solder](#) process direction of travel.

- Components with less than 0.7500mm pad to pad spacing oriented perpendicular to the direction of travel will pull a large solder meniscus as they exit the solder pot and have a higher risk of solder bridges. In addition, inconsistent orientation will negatively affect assembly and inspection.



CID: 6

Content Owner: Jabil

Content Type: Requirement

## For THMT components with round pads and a minimum pad to pad spacing less than 0.6000mm:

On the wave solder side, provide solder [thieving pads](#) at the trailing end of THMT component pad rows.

- Thieving pads can reduce bridging in the wave soldering process by pulling excess solder off the next to last pin and pad of the component.

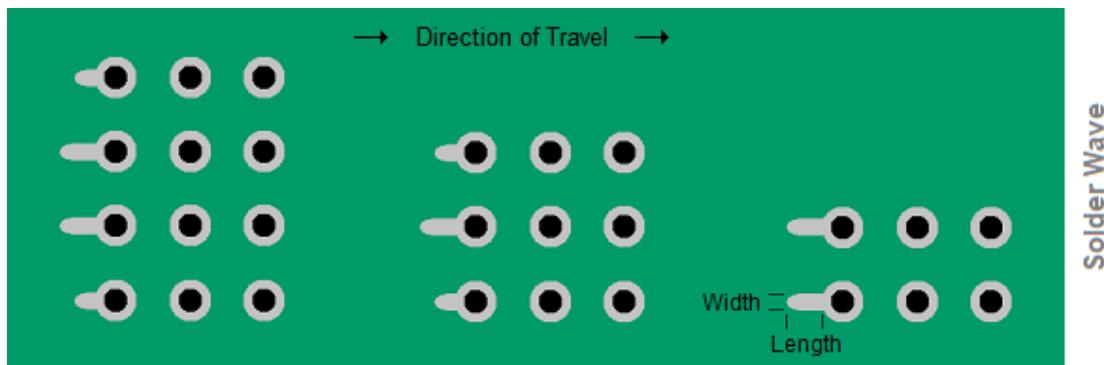
The width of solder thieving pads should be 1.0000mm

For single and double row components, the length of solder thieving pads should be 3.0000mm

For multi-row components, the length of solder thieving pads should be 1.5000mm for outer rows and 3.0000mm for middle rows.

- The solder thief must have adequate surface area to pull the solder off the next to last pin and pad of the component.

**Note:** solder thieves should be considered part of the pad and may affect spacing for [masked pallets](#), see [Entry 1297](#).



CID: 5

Content Owner: Jabil

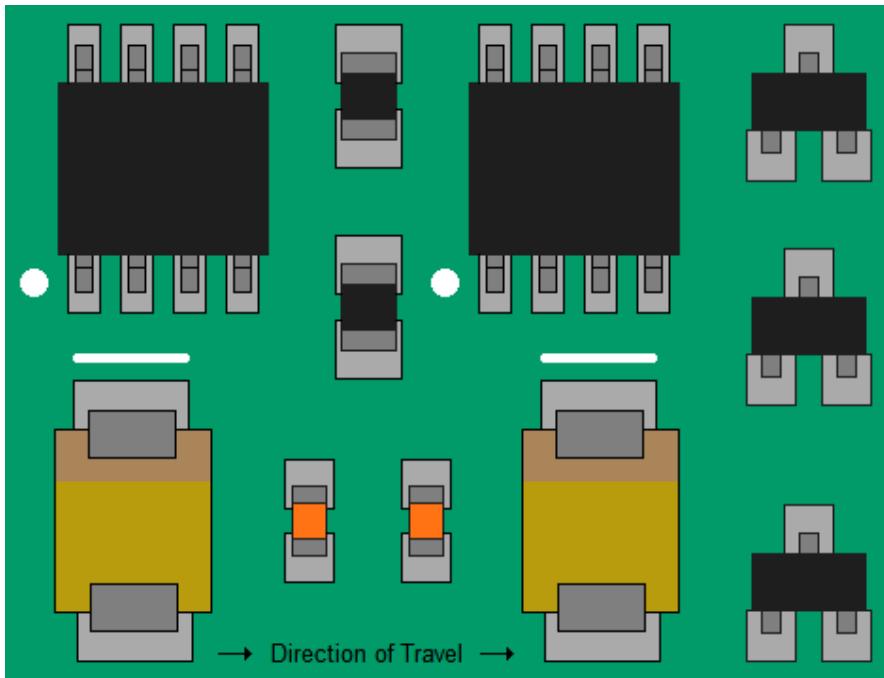
Content Type: Requirement

## SMT Components

See [Entry 1000](#) for a list of wave solder compatible SMT components.

Ensure wave solder compatible gull wing SMT components exposed to the wave are placed parallel to the direction of travel.

- Mis-oriented components have a higher risk of bridging.



## Related Entries

---

DFM Rule [1000 Component Placement > Location > Component to Component Spacing](#)

DFM Guideline [1039 Component Land Pattern > General > Selective and Wave Soldered THMT Component Pads](#)

DFM Rule [1077 PCB Design > General > Auto-Insertion](#)

DFM > Component Selection > General

Entry ID: 1095

## Board Wash Compatibility

### Rule

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 5 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Minimum built in or molded in standoffs for low profile **THMT** parts = 0.3750mm

- This can cause cleanliness issues under the components. If the component does not come with standoffs or shims, another method may be required.

Example: Power bricks, inductors, relays, DC-DC converters, etc.

Typical **SMT** components have a standoff less than 0.3750mm. Whenever possible, select SMT components with standoffs or shims.

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 3 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Whenever possible, components incompatible with aqueous board wash that are unsealed / unprotected such as batteries, switches, non-hermetically sealed DC-DC converters and delay lines should be avoided.

- Incompatible components may require hand soldering and incur extra cost.

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 4 | Content Owner: Jabil | Content Type: Information |
|--------|----------------------|---------------------------|

### Aqueous (Water) Wash:

Consider the increased cleanliness risks when cleaning low profile fine pitch SMT parts (i.e. QFPs, micro BGAs) processed with water soluble organically activated (OA) fluxes and removing the flux with a **deionized water** only (non-chemical) wash process. A DI only wash process has a high surface tension that may be unable to penetrate underneath low standoff parts in order to remove the flux residues.

### Aqueous (Water) Wash with a Defluxing agent:

Verify that the assembly components required to be washed in a cleaner using a defluxing agent are compatible with the process. Certain component sealants may be degraded when exposed to these chemical agents and therefore allow water and / or chemical intrusion that may degrade the component's functional performance.

BGAs with heat spreaders and vent holes also pose a process risk in that water from an inline / batch cleaning process could potentially enter and become difficult to remove without extended bakes.

### Related Entries

DFM Rule [1324](#) Component Selection > Surface Mount > Flux Cleanliness and QFN Components

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DFM > Component Selection > General

Entry ID: 1099

## Maximum Component Height

### Rule

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 5 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Maximum [SMT](#) component height on [primary side](#) = 12.7000mm

Maximum [wave soldered](#) component height on primary side = 100.0000mm

- Components that are too tall may cause issues in manufacturing and will likely incur additional cost.

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 6 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Maximum height for all components on the [secondary side](#) = 5.0000mm

- Components that are too tall may cause issues in manufacturing and will likely incur additional cost.

### Related Entries

DFM Guideline [1080](#) Component Placement > Location > Tall Components and Test Access

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DFM > Component Selection > General

Entry ID: 1107

## Optical Fiber Connectors

### Rule

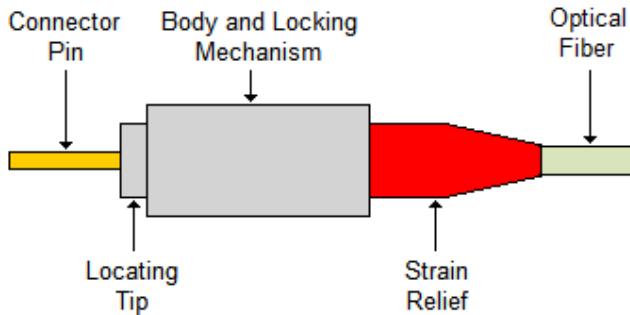
CID: 2

Content Owner: Jabil

Content Type: Requirement

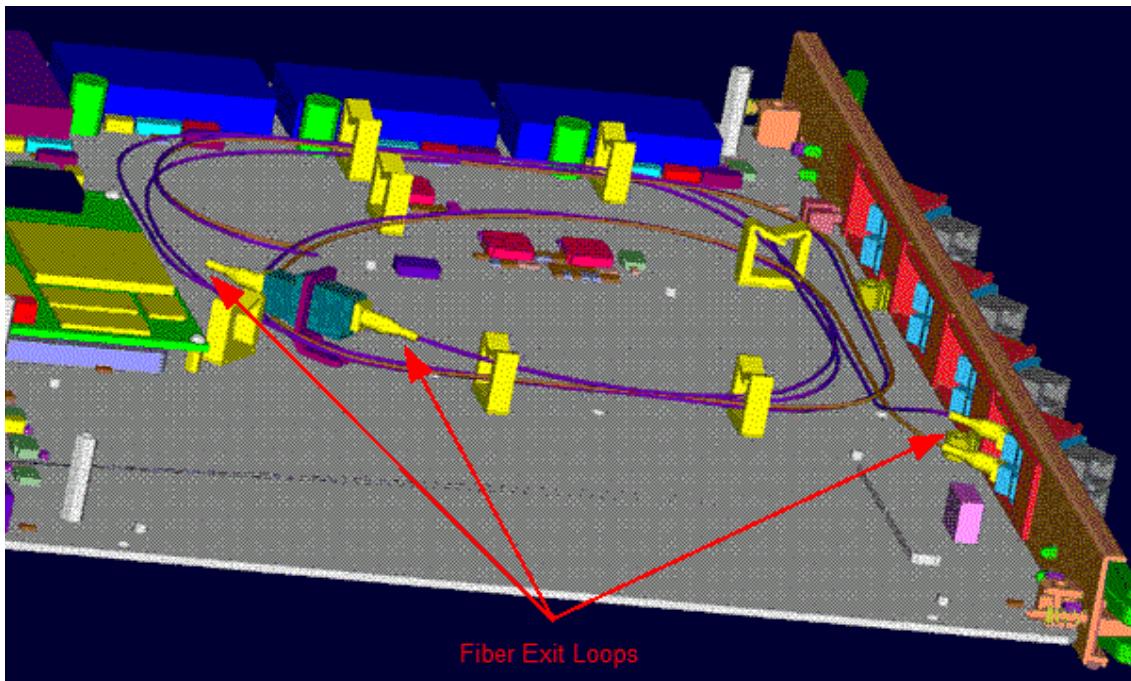
Select optical fiber connectors with strain reliefs.

- Stress or cracking may occur when the fiber entering or exiting a connector is bent at a severe angle which will lead to attenuation of the light intensity.



Position optical fiber connectors so that the exit locations minimize fiber bend.

- A properly positioned exit loop will come off the connector and directly into the hold down clip with little or no bend, avoiding any potential damage to the fiber.



### Related Entries

DFA Guideline 1726 Assembling > Assembling Requirements > Optical Fiber Routing

DFM Guideline 1108 Component Selection > General > Optical Fiber Pigtails

DFM Guideline [1124](#) Data and Deliverables > General > Optical Requirements in Design Drawings

DFA Rule [1728](#) Assembling > Assembling Requirements > Optical Fiber Bend Radius

DFA Guideline [1729](#) Assembling > Assembling Requirements > Optical Fiber Clips

DFM Guideline [1345](#) Component Selection > General > Self-Adhesive Pads and Optical Fibers

DFM Guideline [1636](#) PCB Design > General > Optical Design Considerations

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DFM > Component Selection > General

Entry ID: 1108

## Optical Fiber Pigtails

### Guideline

CID: 2

Content Owner: Jabil

Content Type: Requirement

Observe requirements for [optical fiber](#) pigtails:

Consider the maximum and minimum lengths of the pigtails so the fiber routing accounts for each extreme.

Make pigtails long enough to allow multiple rework operations.

Pigtails must be long enough to fit the [splicing](#) machines used in the manufacturing process.

When utilizing pigtails, avoid the use of dark buffers to enhance troubleshooting using a laser faultfinder.

- All of these requirements can impact the functionality of the product.

### Related Entries

DFA Guideline [1726](#) Assembling > Assembling Requirements > Optical Fiber Routing

DFM Rule [1107](#) Component Selection > General > Optical Fiber Connectors

DFM Guideline [1124](#) Data and Deliverables > General > Optical Requirements in Design Drawings

DFA Rule [1728](#) Assembling > Assembling Requirements > Optical Fiber Bend Radius

DFA Guideline [1729](#) Assembling > Assembling Requirements > Optical Fiber Clips

DFM Guideline [1345](#) Component Selection > General > Self-Adhesive Pads and Optical Fibers

DFM Guideline [1636](#) PCB Design > General > Optical Design Considerations

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DFM > Component Selection > General

Entry ID: 1304

## Conformal Coating Selection

### Information

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 1 | Content Owner: Jabil | Content Type: Information |
|--------|----------------------|---------------------------|

#### Introduction:

Certain [PCB](#) design considerations must be defined in order to determine the type of [conformal coating](#) material and application method that will be used for a specific PCB assembly. The following includes general notes and considerations.

#### Industry Standards:

For further information on defining a conformal coating process see the following:

[IPC-HDBK-830](#) - "Guidelines for Design, selection & Application of Conformal Coatings".

[IPC-CC-830B](#) - "Qualification and Performance of Electrical Insulating Compound for Printed Wiring Assemblies".

#### Considerations during the design of the product in determining the type of conformal coating that is to be used on the product:

- a.) Define Reliability and Test Requirements. Testing requirements (ALT - Accelerated Life Test).
- b.) Understand the Product Life Cycle. What is the expected life span of the product (Toy - 6 months, Consumer 3-5 yrs, Industrial 7-10, Telecom 10-20 yrs, Medical 15-20 yrs , Military - up to 50 yrs).
- c.) Define the product environment. Where will the product be used (automotive - under hood, farm equipment, washing machine, sealed medical, Military - guidance, airline - multiple), temperature range, exposure.
- d.) Assembly Material selection, i.e. PCB, components, conformal coating, etc.) Compatibility with components, mechanics - switches - mounting, connectors, sealants, LED/Lighting, CTE - mismatch, mask, fab, chemistries - [no clean flux](#).
- e.) Understand where the conformal coating application will occur in the build process. Is conformal coating the last of the PCB assembly processes prior to box build?
- f.) Define coating coverage on PCB. Develop an assembly coverage map in conjunction with the customer and the above requirements, determine [keep-out areas](#).
- g.) Understand and define rework and repair. Will the unit require repair following coating, what are the rework methods available/required for the material chosen, establishing standards for rework, determine difficulty level in selected material.

#### Common Types of Conformal Coating with IPC Designations:

- AR - Acrylic
- ER - Epoxy
- XY - Parylene
- SR - Silicone
- UR - Polyurethane

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 2 | Content Owner: Jabil | Content Type: Information |
|--------|----------------------|---------------------------|

#### Pros/Cons of Listed Materials:

|                                    | Pros   | Cons  |
|------------------------------------|--|---|
| AR - Acrylic                       | <ul style="list-style-type: none"> <li>• Very long shelf-life</li> <li>• Fair abrasion resistance and electrical characteristics.</li> <li>• Good protection from moisture and exposure to water.</li> <li>• Dry within minutes at room temperature, prepolymerized (solidification &amp; adhesion, no further cross-linking required)</li> <li>• Easy to apply and considered repairable.</li> <li>• Material is inexpensive</li> </ul> | <ul style="list-style-type: none"> <li>• Poor solvent resistivity (can be removed with acetone or alcohol).</li> <li>• Average mechanical strength and flexibility</li> <li>• Service temperature range (-65 to 125 deg C.) for most materials.</li> </ul>  |
| ER - Epoxy                         | <ul style="list-style-type: none"> <li>• Excellent solvent resistance.</li> <li>• Excellent mechanical and abrasion resistance.</li> <li>• Good humidity resistance.</li> <li>• Very rigid after it has cured.</li> </ul>  | <ul style="list-style-type: none"> <li>• Most epoxies are two parts requiring mixing and dry usually to an opaque color.</li> <li>• Two-part epoxies have a very short pot life once mixed.</li> <li>• Improper mixing can lead to a coating that is either too soft, hard or unable to cure.</li> <li>• Creates thermal expansion problems among <b>SMT</b> components due to TCE mismatch.</li> <li>• Poor repairability. Spot removal is possible; however, it is almost impossible to completely remove without destroying the board.</li> <li>• Due to its rework issues and TCE mismatch, it is one of the least used conformal coatings.</li> <li>• Service temperature range (-65 to 125 deg C.) for most materials.</li> </ul> |
| XY - Polyparaxylelene - (Parylene) | <ul style="list-style-type: none"> <li>• Excellent electrical properties and best moisture resistance of materials.</li> </ul>   | <ul style="list-style-type: none"> <li>• Most expensive process compared to other conformal coatings.</li> </ul>  |

|               | Pros   | Cons  |
|---------------|--|---|
|               | <ul style="list-style-type: none"> <li>• Uniform thin complete coating coverage due to vapor deposition.</li> <li>• Coating is very strong and durable.</li> <li>• Polymer vapor deposits, recombines and cross-links on the board area.</li> </ul>  | <ul style="list-style-type: none"> <li>• Requires expensive specialized capital equipment or outsourcing.</li> <li>• Requires labor intensive masking.</li> <li>• Difficult to remove from the entire board, requires media abrasion, plasma etching or laser burning for removal.</li> <li>• Very long cycle time (batch process)</li> </ul>   |
| SR - Silicone | <ul style="list-style-type: none"> <li>• Excellent service temperature range (up to +200 deg C.) for most materials.</li> <li>• Very low CTE and excellent flexibility.</li> <li>• High Dielectric Constant (can withstand high voltage).</li> <li>• Low surface energy makes it able to penetrate underneath components.</li> <li>• Electrical properties are constant over frequency, temperature and humidity.</li> <li>• Good moisture resistance and low water absorption.</li> </ul> | <ul style="list-style-type: none"> <li>• Poor mechanical strength and abrasion resistance.</li> <li>• Higher material cost than other coating materials.</li> <li>• Very difficult to remove 100% of the residue. Require a combination of scrubbing and solvent immersion to remove residue.</li> </ul>  |
| UR - Urethane | <ul style="list-style-type: none"> <li>• Excellent humidity resistance and electrical properties.</li> <li>• Improved mechanical strength and abrasion resistance over acrylics.</li> <li>• Improved solvent resistance over Acrylic coating.</li> </ul>   | <ul style="list-style-type: none"> <li>• For repair, can be removed through chemical stripping.</li> <li>• Many are moisture sensitive that typically require more frequent nozzle maintenance.</li> <li>• Some are two component types.</li> <li>• Limited pot life for two component types due to cross-link after mixing.</li> <li>• Service temperature range (-65 to 125 deg C.) for most materials.</li> <li>• Will shrink and harden during curing and can damage glass-bodied components. Such components may require a sleeve over them prior to coating.</li> </ul> |

## [Related Entries](#)

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DFM Guideline [1572](#) PCB Design > General > Conformal Coating

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## Supplemental Component Selection Information

### Information

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 1 | Content Owner: Jabil | Content Type: Information |
|--------|----------------------|---------------------------|

A typical [PCB](#) design begins with a schematic and set of components. The component set governs the final board layout and the processes used to manufacture it. The following includes general notes for component selection and process compatibility.

### Component Industry Standards

- EIA-PDP-100 - Catalog listing of outline drawings illustrating the dimensions of passive components.
- JEDEC-95 - Outlining document for solid state products.
- [IPC-2221 / 2222](#) - Design Standard for Rigid Printed Board and Rigid Printed Board Assemblies, Material Selection Section.

### General Component Process Considerations

- Line Balancing is a focused effort to optimize the distribution of component count and component types on each side of the board, relative to the available assembly line. The line configuration ultimately dictates the choice, consult with the workcell responsible for building the product.
- Limit the use of a component part number to one side of the board. This requires fewer reels of components, less changeover, etc. This may not be possible with high use components.
- When using programmable parts, consider designing in space for sockets on prototype builds.
- Do not use components requiring lead trimming or forming, this adds cost and additional handling.
- Fine pitch balled / leadless components like CSP and flip chip components should be reviewed with consideration given to yield impact and rework where alternate / more robust components types are available.
- Ensure that through-hole passive component lead spans match the board hole spans by selecting supplier part numbers that are complete, including the lead form and media type.
- Verify sprocket pitch of thru-hole taped/reeled or ammo pack materials are compatible with available equipment (15mm pitch is not usable at certain sites).
- Ensure consistent component orientation within the tape, particularly optical and electromechanical types.
- Whenever possible, over-molded plastic [BGA](#) components should be specified as opposed to the encapsulated type. Encapsulated BGA components allow more of the BT substrate to be exposed, resulting in increased flex during heating cycles. While normal reflow is possible, rework or replacement of these parts becomes difficult.
- Whenever possible, all devices should be selected from standard component package types. Standard types are available from multiple sources and are compatible with most processes.
- If components do not have specific orientation needs or will not be damaged using bulk-packaging, it may be an option because it can cost less and generate less waste.

## Moisture Sensitive Components

- JEDEC J-STD-020 is a classification and marking system stating how long the package can be opened under normal ambient conditions (see table).
- Longer component exposure times are more desirable for manufacturing.
- If exposure times are exceeded, the parts must be baked in a dry atmosphere based on vendor requirements to drive moisture out before they can be used again.

| Level | Conditions              | Exposure Time |
|-------|-------------------------|---------------|
| 1     | <=30 degrees C / 85% RH | Unlimited     |
| 2     | <=30 degrees C / 60% RH | 1 Year        |
| 2A    | <=30 degrees C / 60% RH | 4 Weeks       |
| 3     | <=30 degrees C / 60% RH | 168 Hours     |
| 4     | <=30 degrees C / 60% RH | 72 Hours      |
| 5     | <=30 degrees C / 60% RH | 48 Hours      |
| 5A    | <=30 degrees C / 60% RH | 24 Hours      |
| 6     | <=30 degrees C / 60% RH | Time on Label |

### Related Entries

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DFA Guideline [1167](#) Assembling > Assembling Requirements > Packaging and Re-orientation of Parts / Sub-assemblies

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DFM > Component Selection > General

Entry ID: 1345

## Self-Adhesive Pads and Optical Fibers

### Guideline

CID: 2

Content Owner: Jabil

Content Type: Requirement

Do not use self-adhesive pads (e.g. DWDM butterfly package) as a thermal solution for [optical fibers](#).

These pads are difficult to rework and will add cost. Please select a reworkable thermal solution.

### Related Entries

DFA Guideline [1726 Assembling > Assembling Requirements > Optical Fiber Routing](#)

DFM Rule [1107 Component Selection > General > Optical Fiber Connectors](#)

DFM Guideline [1108 Component Selection > General > Optical Fiber Pigtauls](#)

DFM Guideline [1124 Data and Deliverables > General > Optical Requirements in Design Drawings](#)

DFA Rule [1728 Assembling > Assembling Requirements > Optical Fiber Bend Radius](#)

DFA Guideline [1729 Assembling > Assembling Requirements > Optical Fiber Clips](#)

DFM Guideline [1636 PCB Design > General > Optical Design Considerations](#)

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DFM > Component Selection > General

Entry ID: 1738

## General Component Selection

### Guideline

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 2 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Verify component terminations / leads are compatible with the process chemistry and PCB surface finish.

- Termination / lead finishes such as matte tin, nickel palladium, gold etc. are difficult to solder and may result in tin whiskers if not compatible with the process chemistry and PCB surface finish.

Minimize thermal cycles for heat sensitive components.

- Some components can withstand a single thermal cycle but can be damaged by two thermal cycles.

Select components that can withstand lead-free thermal conditions.

- Components can be damaged if they are not rated for the thermal conditions of the soldering processes.

Select [SMT](#) crystals instead of [THMT](#) barrel crystals.

- SMT crystals don't require manual placement, are easier to handle and are more reliable.
- If THMT crystals must be used, they should not be shipped in bags due to their sensitivity to handling damage. They should be packaged in protective ESD foam and have the leads ordered to the required length to minimize handling damage.

Do not select crystals for use with ultrasonic welding.

- The ultrasonic vibrations may damage crystals so extra testing may be required to ensure they are not damaged.

Select shields that have removable pick up features.

- After the shield has been placed, having a removable pick up feature makes it easier for automated optical inspection (AOI) and rework.

Verify maximum soldered wire harness temperature.

- The wire insulation could be damaged.

Ensure orientation by selecting SMT connectors that have boss pins with different sizes that match holes in the PCB.

- This will prevent the connector being installed backwards.

If location is critical, select SMT connectors that have locator pins.

- This will ensure the connector is closely aligned with the intended location.



DFM > Component Selection > General

Entry ID: 1743

## Thermal Cycles for PCBs with OSP

### Guideline

CID: 2

Content Owner: Jabil

Content Type: Requirement

For [OSP PCBs](#): maximum thermal cycles = 3

- OSP can limit the number of thermal cycles that a product can withstand.

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DFM > Component Selection > Surface Mount

Entry ID: 1112

## Ceramic Capacitors in the Wave Solder

### Guideline

CID: 3

Content Owner: Jabil

Content Type: Requirement

Maximum ceramic package size for [capacitors](#) that are exposed to the [wave solder](#) = 2512.

- Larger packages may crack during wave soldering.

**Note:** Use C0G – X7R - Z5U - Y5U capacitor types in this order of preference to reduce susceptibility to cracking. Another option may be to use multiple components in series or parallel configurations to achieve the same functionality with smaller components.

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DFM > Component Selection > Surface Mount

Entry ID: 1561

## Chip Resistors and High Sulfur Environments

### Guideline

CID: 2

Content Owner: Jabil

Content Type: Requirement

Select sulfur resistant chip resistors for use in high sulfur environments.

Sulfur contamination may cause thick film chip resistors to increase in resistance value and in severe cases may cause an open circuit. The sulfur reacts with the silver coating on the chip terminals which results in a non-conductive silver sulfide material. Silver sulfide contamination is a latent failure mode that is undetectable at the time the resistor is manufactured and when the product is assembled.

Chip resistor manufacturers are offering parts that are sulfur resistant. These are designed mainly for use in environments exposed to high levels of sulfur contamination and may be more expensive.

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DFM > Component Selection > Surface Mount

Entry ID: 1739

## SMT Component Selection

### Guideline

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 2 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Review flip chip and COB pitch and I/O count.

- Understanding how test may impact the design is necessary for a thorough design analysis.

Do not select two pin SMT headers.

- Two pin SMT headers tend to tip over during reflow soldering.

Eliminate zero ohm resistors after NPI.

- The added BOM cost and opportunity for quality issues is unnecessary.

Avoid selecting capacitors and resistors with the same value but different tolerances.

- Multiple part numbers versus a single part number can increase BOM and assembly costs.

Select BGAs and QFNs that are compatible with the process alloy and land patterns that match the recommended layout.

- The component, process alloy and land pattern are critical to forming reliable solder joints.

Avoid HASL surface finish for less than 0.5000mm pitch QFP and 1.2700mm pitch BGA components.

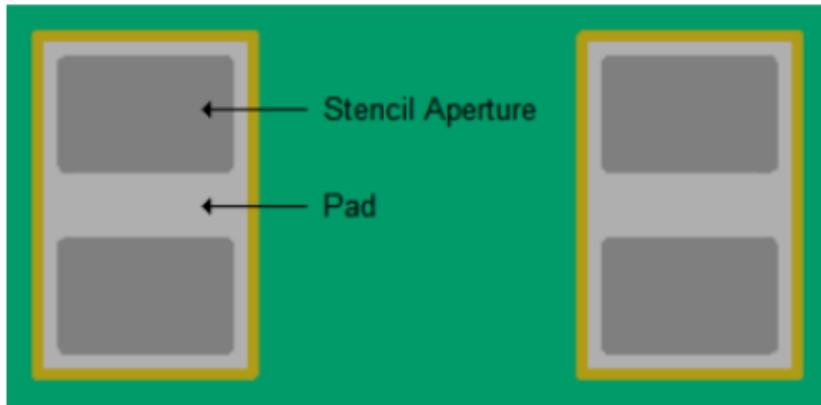
- HASL can cause a standoff between the stencil and the pad, depositing excess solderpaste causing shorts / bridging. HASL can also cause a dome shaped solder deposit on the pads and the component may slip off the pads prior to reflow.

[BGA](#) packages are preferred instead of 0.4000mm or finer pitch [QFP](#) packages.

- BGAs are more durable than QFPs and have better combined yields.
- Consideration must be given to the workcell assembly capabilities and reliability requirements of the product prior to selecting this package type.

Do not select cylinder shaped [SMT](#) components such as [MELFs](#).

- If MELFs are required, a mitigation technique to prevent movement and potential solderballing is to utilize split stencil apertures as shown below.
- Dimensions must be derived based on component diameter so that the component will not be free to roll.

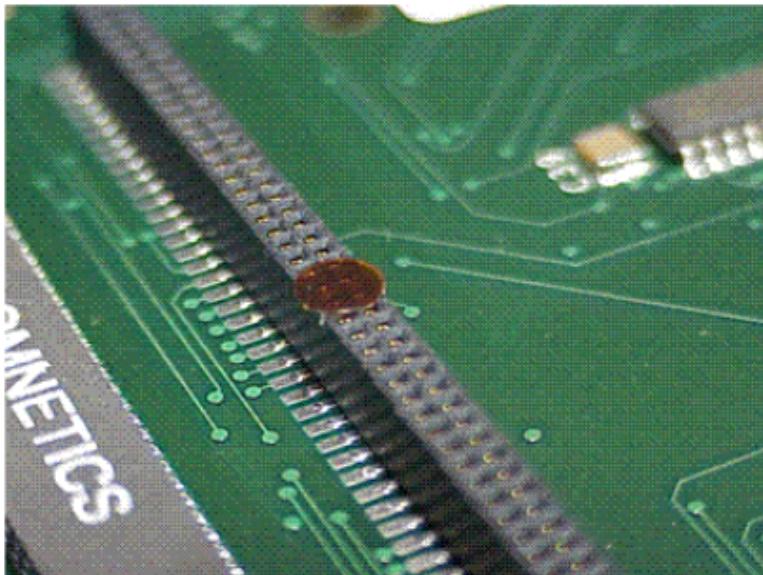


Select [SMT](#) connectors packaged in trays or reels compatible with SMT pick and place equipment.

- Incompatible packaging can require additional handling to repackage the components, potentially damaging the component pins.

Ensure vacuum pickup point tabs are specified when selecting connectors for automated placement.

- Connectors may need to have a [Kapton](#) label or metal clip added at the supplier to provide a flat area for the nozzle pickup point. Lack of a pickup point may require hand placement of the component, custom tooling or custom equipment increasing cost.



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DFM > Component Selection > Through Hole Mount

Entry ID: 1115

## DIP Component Selection

### Guideline

CID: 3

Content Owner: Jabil

Content Type: Requirement

Select [auto-inserted DIP](#) components in 7.5000mm or 15.2500mm span packages.

- Other sizes cannot be automatically inserted and may incur additional cost and quality issues.

### Related Entries

DFM Rule [1077](#) PCB Design > General > Auto-Insertion

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DFM > Component Selection > Through Hole Mount

Entry ID: 1117

## Lead Length Protrusion for THMT Soldering

### Guideline

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 3 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Minimum lead length protrusion for [wave soldering](#), [selective soldering](#), hand soldering, and robotic soldering is 0.5000mm.

- Shorter lead lengths can cause inspection issues and insufficient solder fillets. The lead tip must be visible in the solder joint.

**Note:** every effort should be made to adhere to the minimum requirement. If not possible, IPC610 section 7.3.3 Note 1 does specify the following exceptions: "For components having manufacturer's pre-established lead lengths that are less than board thickness, and the components or lead shoulders are flush to the board surface, the lead end is not required to be visible in the subsequent solder connection."

Violations that utilize this exception should be noted as a finding in the design review and called out in the assembly drawing.

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 4 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Maximum wave soldering, selective soldering, hand soldering, and robotic soldering lead length protrusion for [IPC class 2](#) = 2.5000mm and for [IPC class 3](#) = 1.5000mm

- Longer lead lengths can cause interference with the soldering equipment and possibly contribute to bridging defects.
- Maximum lead lengths can be influenced by component pitch, process requirements as well as workmanship standards ([IPC-610 class 2 and 3](#)).

**Note:** every effort should be made to adhere to the maximum requirement. If not possible, IPC610 section 7.3.3 Note 2 does specify the following exceptions: "Connector leads, relay leads, tempered leads and leads greater than 1.3000mm in diameter are exempt from the maximum length requirement provided that they do not violate minimum electrical spacing."

Utilizing these exceptions could create significant issues in the downstream design and assembly processes, especially functional and electrical safety, so diligence is necessary before allowing the exceptions.

Violations that utilize any of these exceptions should be noted as a finding in the design review and called out in the assembly drawing.

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DFM > Component Selection > Through Hole Mount

Entry ID: 1740

## THMT Component Selection

### Guideline

|        |                      |                           |
|--------|----------------------|---------------------------|
| CID: 2 | Content Owner: Jabil | Content Type: Requirement |
|--------|----------------------|---------------------------|

Do not select HASL PCB surface finish if press fit components are present.

- The hole diameter can vary more with HASL surface finish making assembly / pressing difficult.
- Large separate pins may be OK but if the placement force needs to be monitored it can cause assembly issues.

Minimum snap fit lead length protrusion = 0.2000mm

- During heating cycles the component could lift up if the leads are not long enough, tooling may be required to hold it in place.

Ensure polarity by selecting connectors that have keyed plastics that match the PCB.

- This can allow the component to be installed backwards.
- Selecting headers or connectors from suppliers with missing pins and blocking / not drilling a through hole in the PCB is another method to aid in ensuring polarity.
- Components could be prepped internally but would incur additional cost.

Avoid selecting THMT components with "kinked" leads.

- Kinked leads may prevent solder from traveling all of the way up the barrel of the THMT device, resulting in an insufficient solder hole fill.
- Kinked leads may require more insertion force to press the leads into the barrel, resulting in ergonomic issues.

**Note:** If kinked leads must be used and there is no vendor recommended hole size, research like kinds of components. If no vendor recommendations that are comparable are available, start with the standard hole size (see [Entry 1314](#)) and then follow up with testing insertion and barrel fill in assembly. Evaluate if the hole size or shape (oblong) needs to be adjusted to allow insertion and adequate solder hole fill.

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## Printed and Flexible Hybrid Electronics General Information

### Information

CID: 1

Content Owner: Jabil

Content Type: Information

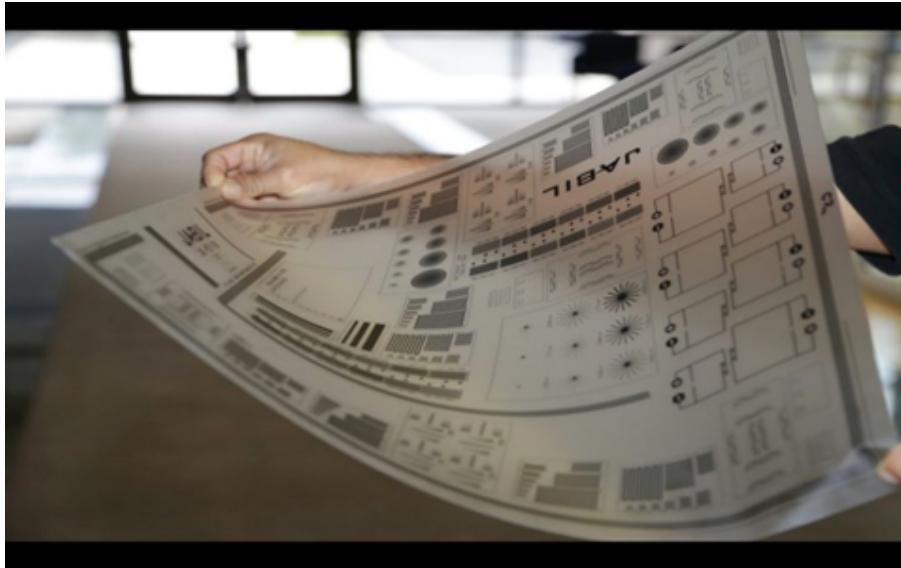
#### Introduction:

**Printed electronics (PE)** refers to a technology in which various printing methods are used to fabricate electronics for a multitude of applications. The process involves using commercial printing equipment such as [screen printing](#), [flexography](#), [gravure](#) and [inkjet](#), which are suitable for defining patterns on a material. Electrically functional inks are deposited on the substrate creating active or passive devices such as conductive traces, thin film transistors, capacitors, coil sensors and resistors. There are a vast number of materials that can be used in the field of PE, including inks such as conductive, dielectric, and non-functional, and a variety of substrates such as plastics, glass, paper, and textiles. Some examples of PE applications include E-textiles, printed batteries, membrane switch panels, heaters, cabling harnesses, and capacitive touch panels. For the fabrication of printed electronics, most standard industrial printing methods are employed to apply ink layers one atop another.

**Flexible hybrid electronics (FHE)** refers to an emerging advancement to PE which combines printed technology with traditional rigid components to develop a hybrid product. FHE facilitates the use of off-the-shelf sensors and electrical components with printed interconnects. As the field grows, printed sensors are also being developed with the advancement of inks for consumer, medical, and industrial segments. Some examples of FHE include medical devices, smart packaging and wearables.

In some applications, lower costs can be realized by system integration and high-volume fabrication. In some domains such as distributed component arrays, printing simplifies the manufacturing process and form factor. Printing on flexible and / or conformable substrates allows electronics to be placed on curved surfaces (human machine interfaces on appliances), flexible (smart packaging or medical devices) or stretchable (wearable) surfaces.

**Note:** the performance of printed devices must be evaluated to ensure it meets the criteria for the desired application.



CID: 2

Content Owner: Jabil

Content Type: Information

#### Comparison of Printing Techniques:

| Feature                            | Gravure          | Inkjet          | Flexography  | Screen Print     |
|------------------------------------|------------------|-----------------|--------------|------------------|
| Resolution                         | 15 µm            | 15 µm           | 20 µm        | 30 µm            |
| Ink Film Thickness                 | 0.02 to 12 µm    | 0.01 to 0.50 µm | 0.17 to 8 µm | 3 to 50 µm       |
| Printing Speed (meters per minute) | 8 to 100         | 0.02 to 5       | 5 to 180     | 0.6 to 100       |
| Image Carrier                      | Gravure Cylinder | Virtual Carrier | Flexo Plate  | Stencil / Screen |

## [Related Entries](#)

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DFT Guideline [1710 Electrical Requirements > General > Probe Selection for Printed Electronics](#)

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## **Missing File Attachments**

The following file attachments are referenced in the DFx content, but could not be included in the extract. Please provide copies of these files along with the content extract.

Entry 1385 - BGA Land Pattern Matrix

Entry 1838 - ECAD Design