Jabil Digital DFx Content Extract

Design For Test

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Design For Test

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DFT > Data and Deliverables > General
Entry ID: 1055

Data Requirements for FLASH and EEPROMs

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

If FLASH or EEPROM programming at ICT is required, identified devices will require HEX or S-Record files and memory maps for ICT programming. Memory maps should match the data sheets for the target device to facilitate programming.

DFT > Data and Deliverables > General
Entry ID: 1056

Data Requirements for VLSI, ASIC and Custom Devices

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

JEDEC, POF and or SVF files must be provided for devices that require programming and or testing. The supplied file must match the data sheet requirements for the target device. Lack of these files can cause delays in test development, reduced test coverage and additional costs.

Programmable devices from suppliers of VLSI, ASIC or custom devices may require these support files.

Supplied files are used internally while programming / testing or used externally for purchased programmed parts.

CID: 3	Content Owner: Jabil	Content Type: Requirement

Provide simulation vectors for all ASIC's and other semi-custom or custom parts. If simulation vectors are made available in a format that can be translated for use by the test system, test development time can be significantly reduced. Internal development time for test vectors to exercise custom devices can take long periods of time.

DFT > Data and Deliverables > General
Entry ID: 1057

Test Development Documentation

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Documentation that provides test specifications / requirements, expected performance information, and circuit schematics should be made available for each assembly to support the test development.

Documentation Requirements:

- Schematics
- BOM
- FAB Drawing
- Assembly Drawing
- Functional specifications
- Test specification
- Cad files
- Links to networks where these documents can be accessed (where available).
- Special Software Development Requirements
- Specify any additional programming requirements that may be necessary
- Programmable component identification and requirements, interfaces required, etc.
- Specify any Special Hardware Development Requirements.
- Require a minimum of one "gold board"
- Mechanical samples

DFT > Data and Deliverables > General
Entry ID: 1058

BSDL Files

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Obtain BSDL files for all boundary-scan devices in the design. The BSDL files describe the boundary-scan capabilities and attributes for the corresponding devices in VHDL syntax and are typically available from the component supplier. Different BSDL files are needed for each package type. Lack of these files can cause delays in test development, a loss in test coverage and additional costs.

An additional reference is IEEE 1149 (latest revision) regarding boundary scan requirements.

DFT > Component Selection > General
Entry ID: 1062

Boundary Scan Devices and TDI/TDO Pin Placement

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Select boundary scan devices that are designed with the TDI and TDO pins on the opposite ends or corners of the package. This will reduce the likelihood of these signals being shorted.

These devices should have power or ground pins between the TDI and TDO pins. In the event of a short these pins will create a solid "0" or "1" that can be detected. Shorts to other signals might be more difficult to detect due to their varying states.

DFT > Component Selection > General
Entry ID: 1063

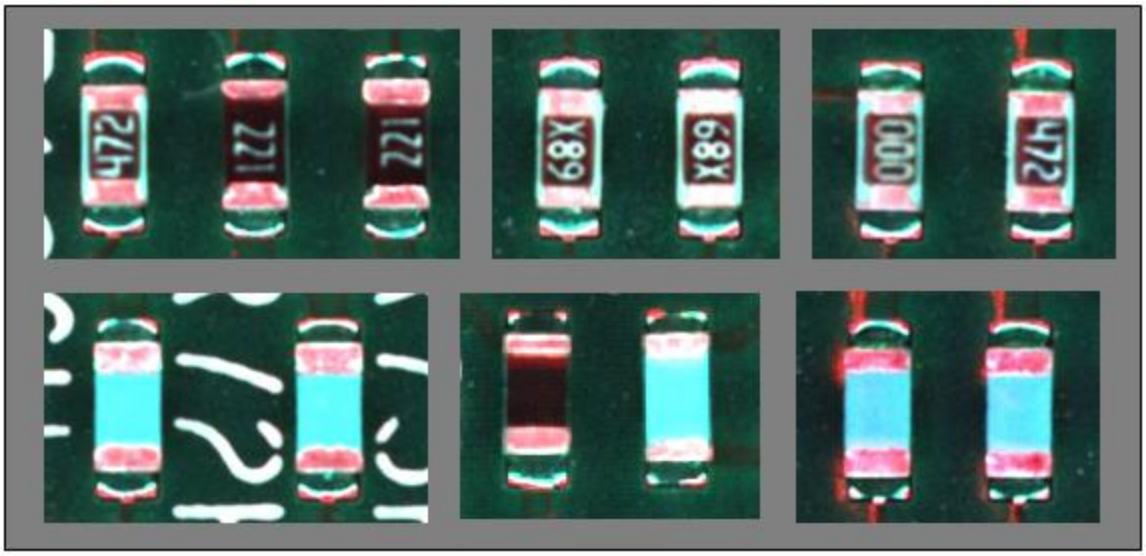
Select Chip Components with Human Readable Identifiers for AOI

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Select chip components with human readable identifiers on 0603 (1608 Metric) and larger.

AOI has the ability to verify that populated components are correct if there is a readable marking. This part verification can be used to ensure that the component has the correct value along with the correct placement position. This will allow the identification of wrong parts early in the manufacturing process, preventing a significant amount of rework and waste.



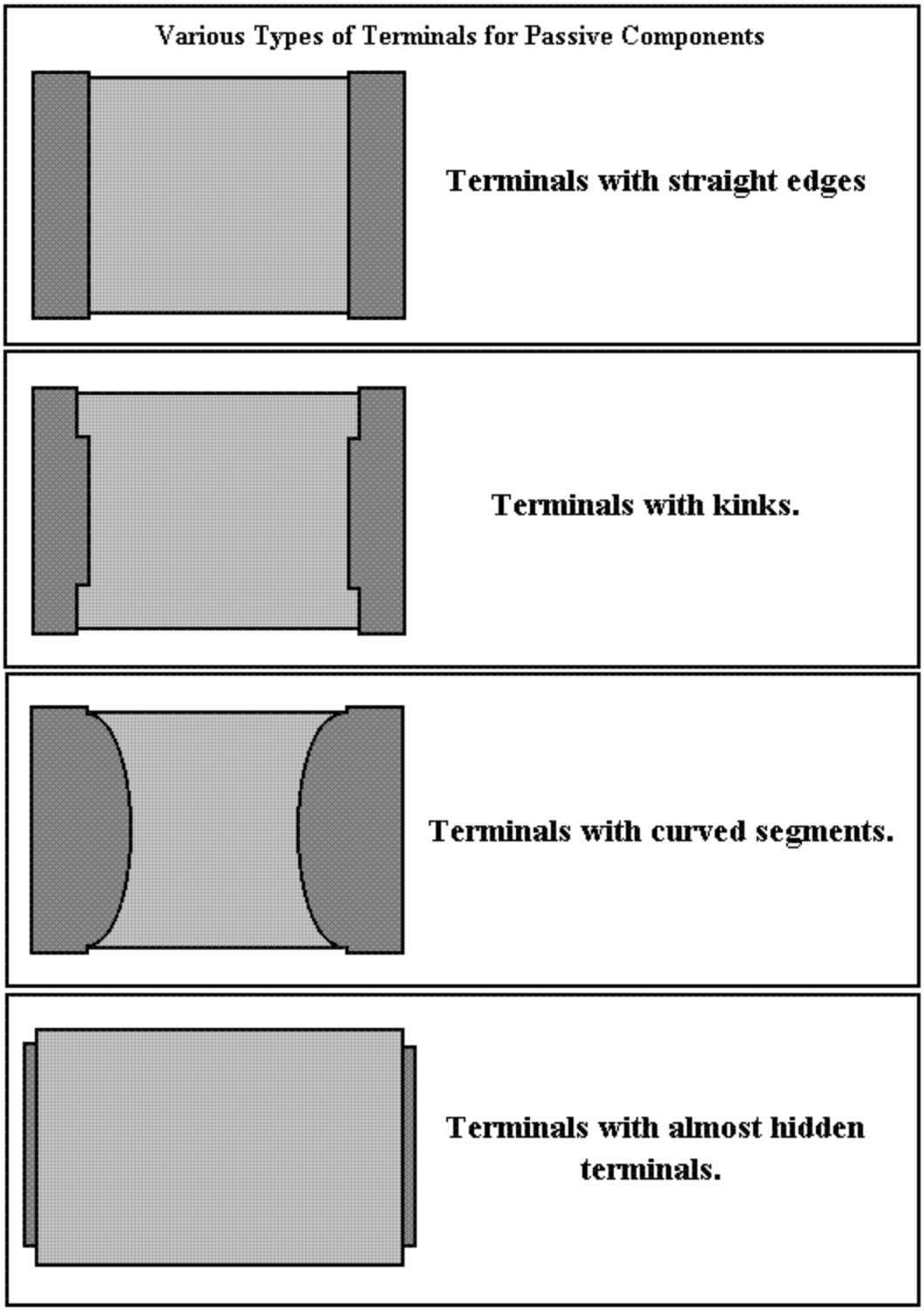
DFT > Component Selection > General
Entry ID: 1064

Select Same Component Terminal Shapes for AOI

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Select components with the same terminal shapes when utilizing AOI. It is desirable to provide terminals of the same type to reduce the variability of the components on the assembly which will reduce programming time and increase AOI repeatability.



DFT > Component Selection > General
Entry ID: 1065

Hand Soldered Components in RF Designs

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

In an RF design, do not use hand soldered components. Hand-soldered components may be sensitive to temperature, placement location, component tolerance, soldering technique, and handling. Based on the component and its sensitivity within the circuit, significant performance variation may be introduced by the above.

If hand soldered components must be utilized, a highly skilled assembler may be required to mount the components.

DFT > Component Selection > General

Entry ID: 1066

RF Circuits and Component Tolerance

Rule

CID: 2	Content Owner: Jabil	Content Type: Requirement

Careful consideration of component tolerances in sensitive circuits, such as a lumped element filter, is an important part of RF design. Passive components with a tighter tolerance (for example 1% instead of 5%) are likely to minimize performance variations such as frequency shifts. In the design phase or later during revision changes, tolerance variation should be considered to assure optimum yield in manufacturing.

The design engineer should carefully analyze components from alternate vendors because they can have the same values but still affect the RF performance of the design at the board or system level. The cumulative variation introduced by parasitics and lumped elements can have an overall effect on the complete system.

Note: Never substitute suppliers of components used in RF circuits with alternative suppliers unless approved and validated by the customer.

DFT > Component Selection > General
Entry ID: 1067

RF Amplifiers

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Design RF amplifiers for unconditional stability (impedance indifference) so that regardless of what input / output impedance or temperature variability is presented to the device under test, the device will not go into oscillation. The potential for oscillation increases with wideband, high frequency, and/or high power devices.

If the amplifier cannot be designed for unconditional stability, additional mitigation may be required for the product and / or test equipment at additional cost.

Note: In the extreme, the board may be severely damaged or un-repairable. The test equipment and/or test station are also at risk of damage.

DFT > Component Selection > General
Entry ID: 1069

Connector Output Switches in RF Designs

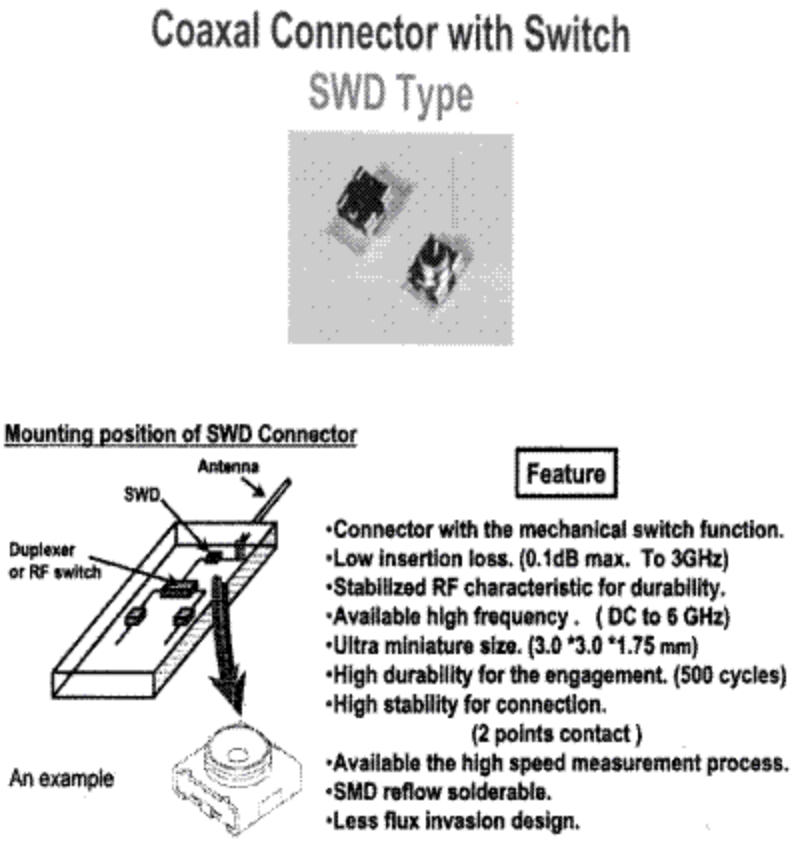
Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

To reduce ambiguities in the test measurements, RF designs require connector output switches at the antenna input/output. The connector output switches allow access to the RF signal output before radiating to the antenna.

It's easier to calibrate and accurately measure the output power level via connector rather than measuring the radiation power of the devices. Radiated power varies as a function of the factory environment because RF radiation reflects off metal.

Example of a Surface mount Wideband Duplexer (SWD) connector switch that has been used in Wireless LAN radios.



DFT > Component Selection > General
Entry ID: 1070

SMA Connectors in RF Designs

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Utilize SMA connectors to enhance testability of RF designs. Selection of the connector type for a product is determined by frequency, insertion loss, mounting requirements, size constraints, and cost. For test, SMAs are the best solution and are a good all-purpose connector with a frequency range to 18GHz.

If possible, assembly using pick and place SMT is preferred.

Strict adherence to manufacturer guidelines and data sheets for mounting tolerance and torque is critical to meeting performance specifications of the product. The higher the frequency, the more critical the tolerances.

DFT > Component Selection > General
Entry ID: 1071

Manual Tuning in RF Radio Designs

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

An ideal radio design should not require tuning such as adjusting the amplifier gain. Tuning is a time consuming process, and is not recommend for manufacturing / test. In addition, improper manual tuning from an operator will degrade the radio performance.

If tuning is required to meet performance specifications, the design should allow for digital control so an automated process can be employed. Mechanically controllable components such as capacitors should be avoided.

DFT > Component Selection > General
Entry ID: 1073

ISP Components and ICT

Guideline

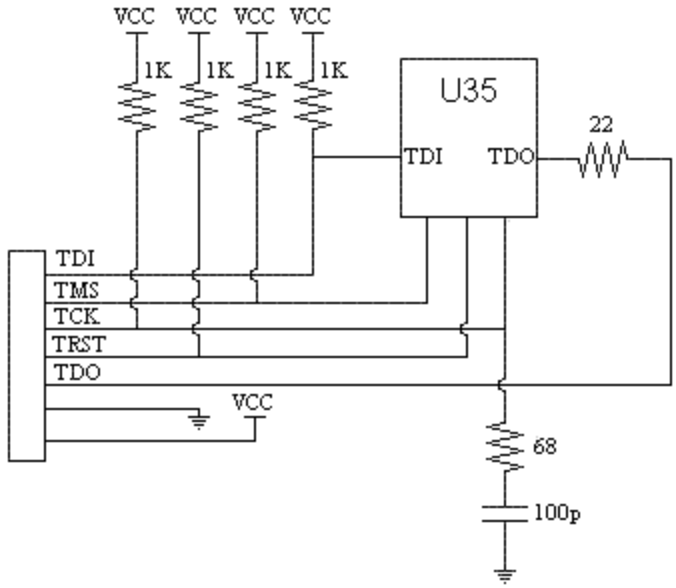
CID: 2	Content Owner: Jabil	Content Type: Requirement

Select ISP (in system programming) devices that are readily programmable at ICT.

If the device is not readily programmable, it may require modifying the circuit to enable programming at ICT. If programming at ICT is not possible, programming at functional test or at an off-line programming station may be necessary. All of which may incur additional costs.

CID: 3	Content Owner: Jabil	Content Type: Requirement

Configure the TAP (test access port) of the ISP device to be fully accessible and support programming.



DFT > Electrical Requirements > General
Entry ID: 1086

Test Probe Access and TH Leads

Guideline

CID: 2 Content Owner: Jabil Content Type: Requirement

Probing of soldered or press fit TH leads is not preferred.

If they must be probed, the minimum pad size of the TH leads must be the diameter of the probe crown + 0.004" (0.1016mm) on the test side of the PCB.

Pad sizes smaller than the test probe crown's diameter could result in contact problems due to the varying length of the lead.

Component Pitch	Crown Tip Diameter Headless	Crown Tip Diameter Headed
0.100" (2.54mm)	0.036" (0.9144mm)	0.062" (1.5748mm)
0.075" (1.9050mm)	0.025" (0.6350mm)	0.040" (1.0160mm)
0.050" (1.27mm)	0.020" (0.5080mm)	0.035" (0.8890mm)
0.039" (0.9906mm)	0.016" (0.4064mm)	n/a

DFT > Electrical Requirements > General
Entry ID: 1087

SMT Leads and Gold Fingers as Test Points

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Do not use SMT component leads as test points. The contact pressure of a test probe can cause an open or a cold solder joint to test as if electrically connected. In addition, any shift in component placement can cause a test probe to deflect off its intended target, creating fixture induced shorts and/or causing probe damage.

CID: 3	Content Owner: Jabil	Content Type: Requirement

Gold fingers should not be used as test points. The gold fingers can be damaged from sharp tipped spring probes while the round and flat tipped spring probes do not provide an acceptable electrical connection for test.

DFT > Electrical Requirements > General

Entry ID: 1088

Test Access and Bus Disable Control for Programmable Devices

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

For device programming at ICT and functional test, full test point access to FLASH devices is required. All device manufacturer programming recommendations must be followed.

CID: 3	Content Owner: Jabil	Content Type: Requirement

For stable FLASH and EEPROM programming at ICT and functional test, the ability to disable any bus connections that could negatively affect the data bus during programming should be provided.

Verify schematics and data for the devices on those busses to make sure that disable methods exist, disable pins are accessible, and without any conflicts.

DFT > Electrical Requirements > General
Entry ID: 1089

Oscillator Output Enable Pins

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Ensure all oscillators have an output enable pin that is test point accessible and pulled high or low through a pull-up or pull-down resistor.

- Oscillators must have an accessible output enable pin. Oscillators with their output enable pin tied directly to a power rail cannot be disabled and may interfere with the testing of other components. Please use pull-up or pull-down resistors on output enable pins and ensure that these pins are test point accessible so that oscillators can be disabled during manufacturing test.

Related Entries

DFT Guideline 1092 Electrical Requirements > General > Clock-Generating Devices
DFT Guideline 1764 Electrical Requirements > General > Crystals

DFT > Electrical Requirements > General
Entry ID: 1090

Output Enable Lines for ICs

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

ICs should have output enable lines so they can be controlled during test. ICs that cannot be properly controlled may be untestable and may cause interference when testing other components.

DFT > Electrical Requirements > General
Entry ID: 1091

Test Point for each Electrical Node

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Ensure a test point is provided for each electrical node.

- An electrical node without a test point assignment may not be accessible and test coverage on that node may be lost. This could result in defect escapes.
- Jumpers, fuses and switches should be treated as multiple lead components connected by multiple nodes and should therefore have separate test points assigned to each node.

Provide sufficient test point access to power and ground planes.

These test points should be evenly distributed throughout the PCB.

- Insufficient test points on GND may cause intermittencies during digital testing at ICT. Sufficient GND access can be described as enough test points to minimize ground bounce and noise during digital testing. These test points should be evenly distributed throughout the PCB, especially around digital devices. Recommend 7% of total number of nets on the PCB.
- Insufficient test points on the power plane(s) used to power up the PCB may not allow the PCB to be powered up during testing. There needs to be a minimum of two test points on any power plane that is being used to power the PCB. One sense test point plus one source test point for every 500mA required by the PCB.

Related Entries

DFM Rule 1034 PCB Design > Test Points > Test Points

DFT > Electrical Requirements > General
Entry ID: 1092

Clock-Generating Devices

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Ensure that clock-generating devices have test point access and a method to disable their outputs.

- If clock-generating devices are not disabled their clock signals could interfere with the testing of other devices. Please provide test point access to, and pull-up or pull-down resistors on the enable pin, removable jumpers or tri-state buffers on the outputs as a means to disable the clock signals.

Related Entries

DFT Guideline 1089 Electrical Requirements > General > Oscillator Output Enable Pins
DFT Guideline 1764 Electrical Requirements > General > Crystals

DFT > Electrical Requirements > General

Entry ID: 1094

RC Circuits and Digital Components

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

RC circuits used for power on reset should be isolated from digital components using an isolating resistor or a digital buffer. Digital components could cause an undesired reset. Recommend using isolation resistors or digital buffers to isolate the RC circuit.

DFT > Electrical Requirements > General
Entry ID: 1100

Control Pins

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Within individual components, ensure that control pins are not tied directly to power or ground signals.

- Control pins tied to power signals cannot be driven to desired state during manufacturing test (i.e. put device in a Hi-Z state). Add a pull-up resistor and ensure the device pin is also test point accessible.
- Control pins tied to ground signals cannot be driven to desired state during manufacturing test (i.e. put device in a Hi-Z state). Add a pull-down resistor and ensure the device pin is also test point accessible.

Within a single component, ensure that control pins are not tied together and not tied directly to power or ground signals.

- Control pins that are tied together and tied to power signals cannot be independently driven to their required states during manufacturing test. Separate each pin, add a pull-up resistor for each pin and ensure each pin is also test point accessible.
- Control pins that are tied together and tied to power signals cannot be independently driven to their required states during manufacturing test. Separate each pin, add a pull-down resistor for each pin and ensure each pin is also test point accessible.

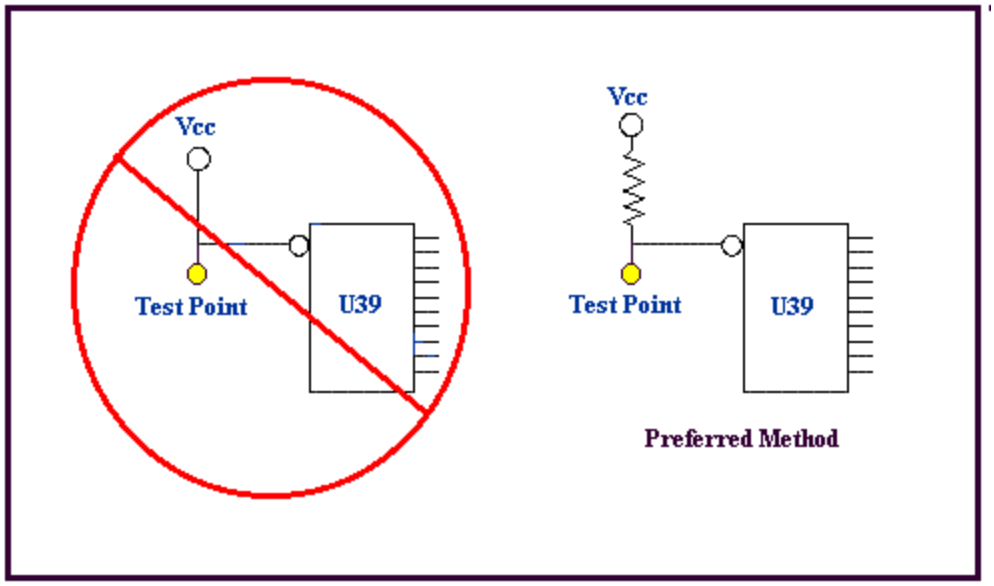
Ensure control pins for two or more devices are not tied together through a common pull-up or pull-down resistor.

- Control pins from multiple devices that are tied together do not allow for devices to be independently driven to their required states during manufacturing test. Separate each device, add a separate pull-up resistor for each pin and ensure each pin is also test point accessible.
- Control pins from multiple devices that are tied together do not allow for devices to be independently driven to their required states during manufacturing test. Separate each device, add a separate pull-down resistor for each pin and ensure each pin is also test point accessible.

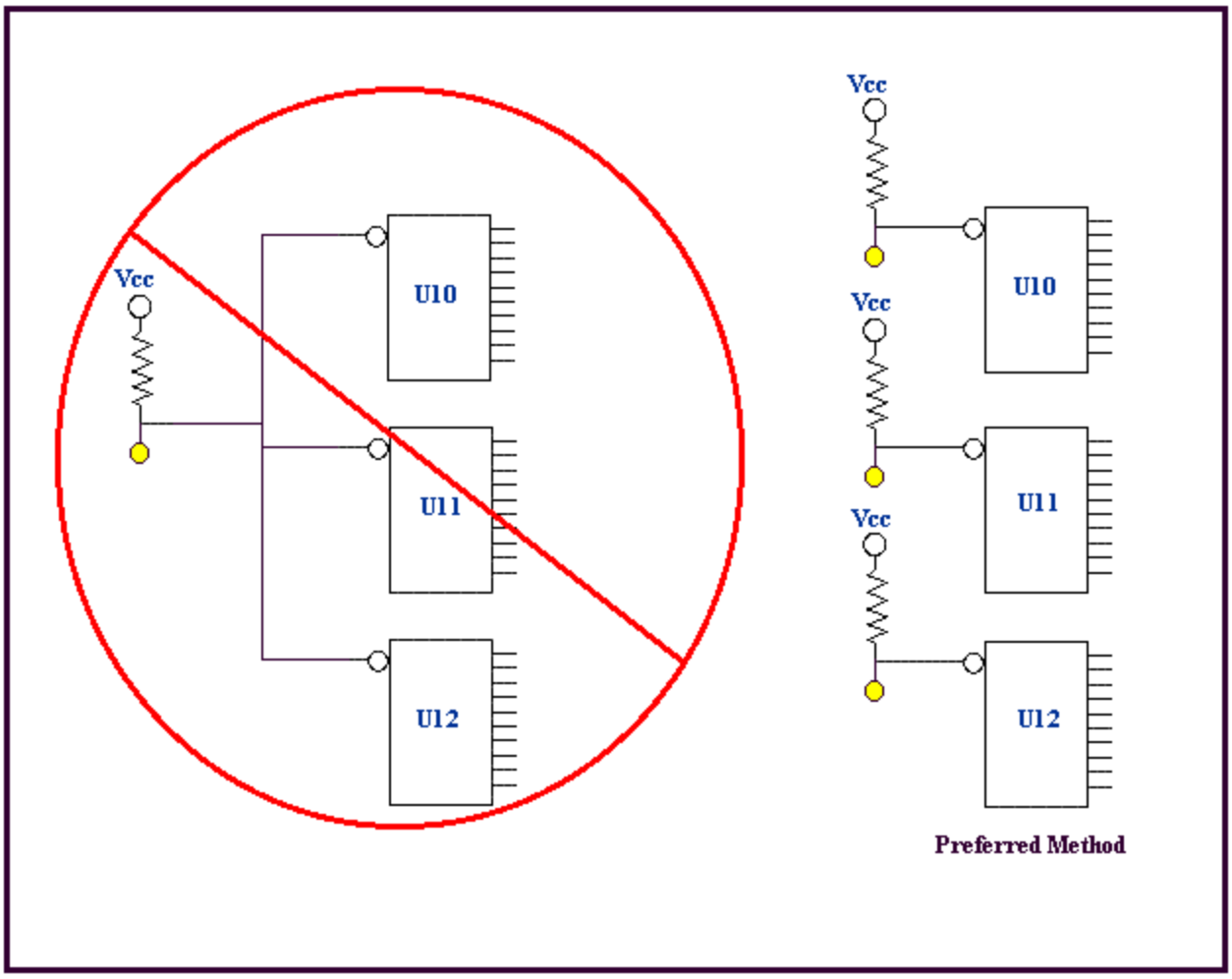
Within individual components, pull-up or pull-down resistors require less than 50mA to change state.

- Pull-up resistor values need to follow the connected device manufacturer recommendations. Low value (requires more than 50mA to drive to the opposite state) pull-up resistors limit the ability of test tools to drive control pins to desired state during manufacturing test (i.e. put device in a Hi-Z state). Please replace pull-up resistors with a larger value resistor.
- Pull-down resistor values need to follow the connected device manufacturer recommendations. Low value (requires more than 50mA to drive to the opposite state) pull-down resistors limit the ability of test tools to drive control pins to

desired state during manufacturing test (i.e. put device in a Hi-Z state). Please replace pull-down resistors with a larger value resistor.



Control Line Termination



Control Line Termination

DFT > Electrical Requirements > General
Entry ID: 1101

PAL Design Guidelines for ICT

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

When PALs are used in the circuit, the following guidelines should be observed at ICT.

- Registers in a PAL should be able to be externally initialized.
- An input pin should be provided to control any Tri-state outputs.
- Where possible, unused terms should be reserved for testing purposes. These terms can sometimes be used to make the testing of other devices more reliable.
- If the PALs have feedback paths, a method of disabling these paths should be incorporated into the circuit. This makes it possible to drive the input of the PAL to a known state and held there without interference from the output.
- All unused bi-directional pins should be tied to a known state rather than left floating.

DFT > Electrical Requirements > General
Entry ID: 1102

Circuit Sections in RF Designs

Guideline

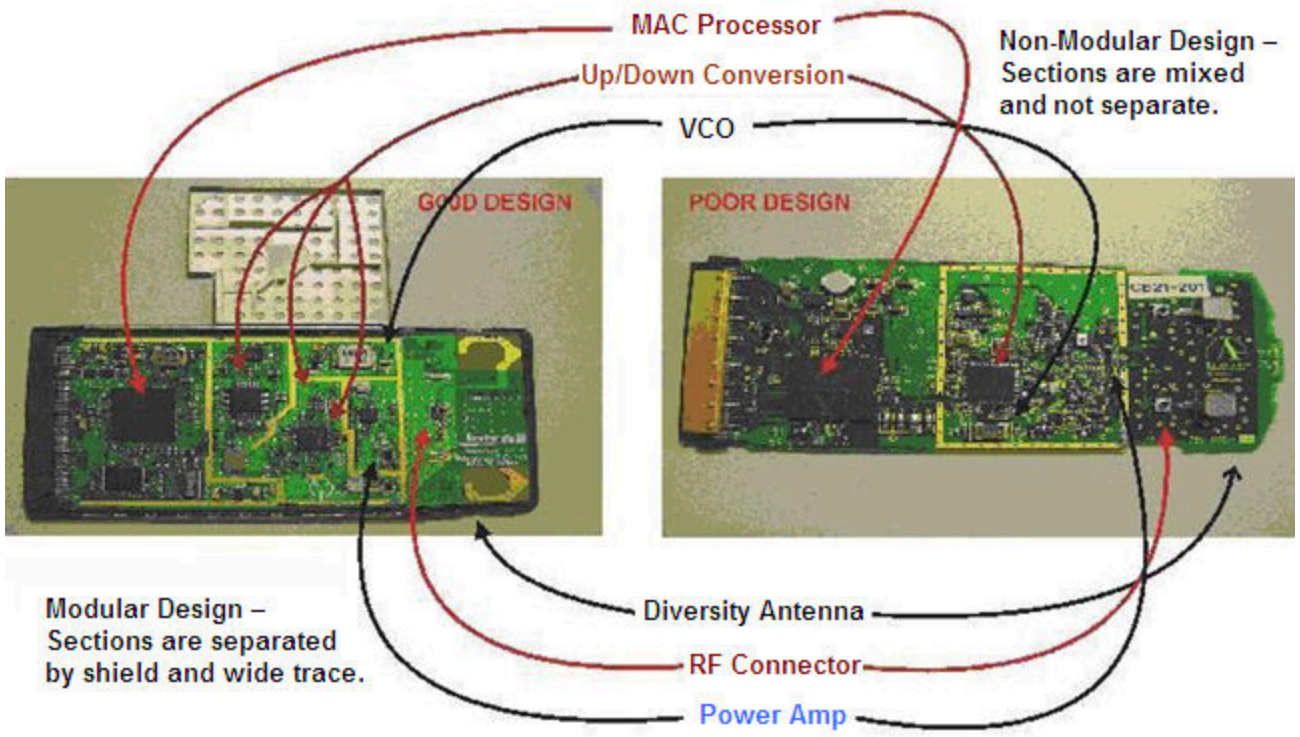
CID: 2 Content Owner: Jabil Content Type: Requirement

In an RF design, modularize circuit sections to minimize noise, spurious signals, and EMI.

Separate the MAC Processor from the RF circuit to minimize noise, spurious signals and EMI.

Isolate in a modular section the following to minimize noise, spurious signals and EMI:

- VCO circuit
- Synthesizer circuit
- Up/Down conversion circuit
- Power amplifier and LNA circuits
- Output connector and antenna circuits



DFT > Electrical Requirements > General
Entry ID: 1420

Testing Higher Frequencies at ICT

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

For oscillators above the 60MHz/100MHz threshold, consider adding a clock divider circuit for test purposes. The divided frequency can be measured to ensure that the higher frequency is correct. In the event the clock divider cannot be designed into the board, it can be added to the ICT fixture to allow measurement.

CID: 3	Content Owner: Jabil	Content Type: Requirement

For clock distribution devices with a test mode, ensure that the select pins used to enter test mode are accessible and not tied directly to power or ground. Frequently these select pins are directly connected to power or ground for normal operation. Add pull up or pull down resistors to allow control of the select pins.

The test mode divides the input frequency down to a lower range for measurement on an ICT system. This test mode is frequently controlled by select pins or by programming a register in the device.

CID: 4	Content Owner: Jabil	Content Type: Requirement

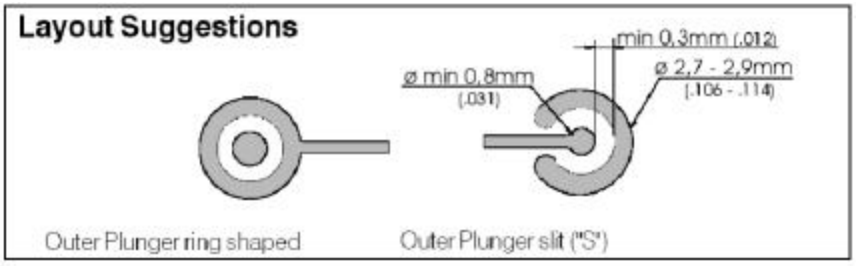
Ensure that all active frequency generating devices can be placed in tri-state mode and test access is available for the enable/disable pin.

Active frequency generating devices if not disabled will interfere with In Circuit Test techniques. A free running oscillator can cause noise in unrelated circuits causing intermittent test failures.

CID: 5	Content Owner: Jabil	Content Type: Requirement

If frequencies higher than 100 MHz are to be measured with external instrumentation, the Unit Under Test should provide a coaxial test point matching the requirements of the coaxial probe of choice.

Two example layouts:



DFT > Electrical Requirements > General
Entry ID: 1421

Test Points for RF Designs

Guideline

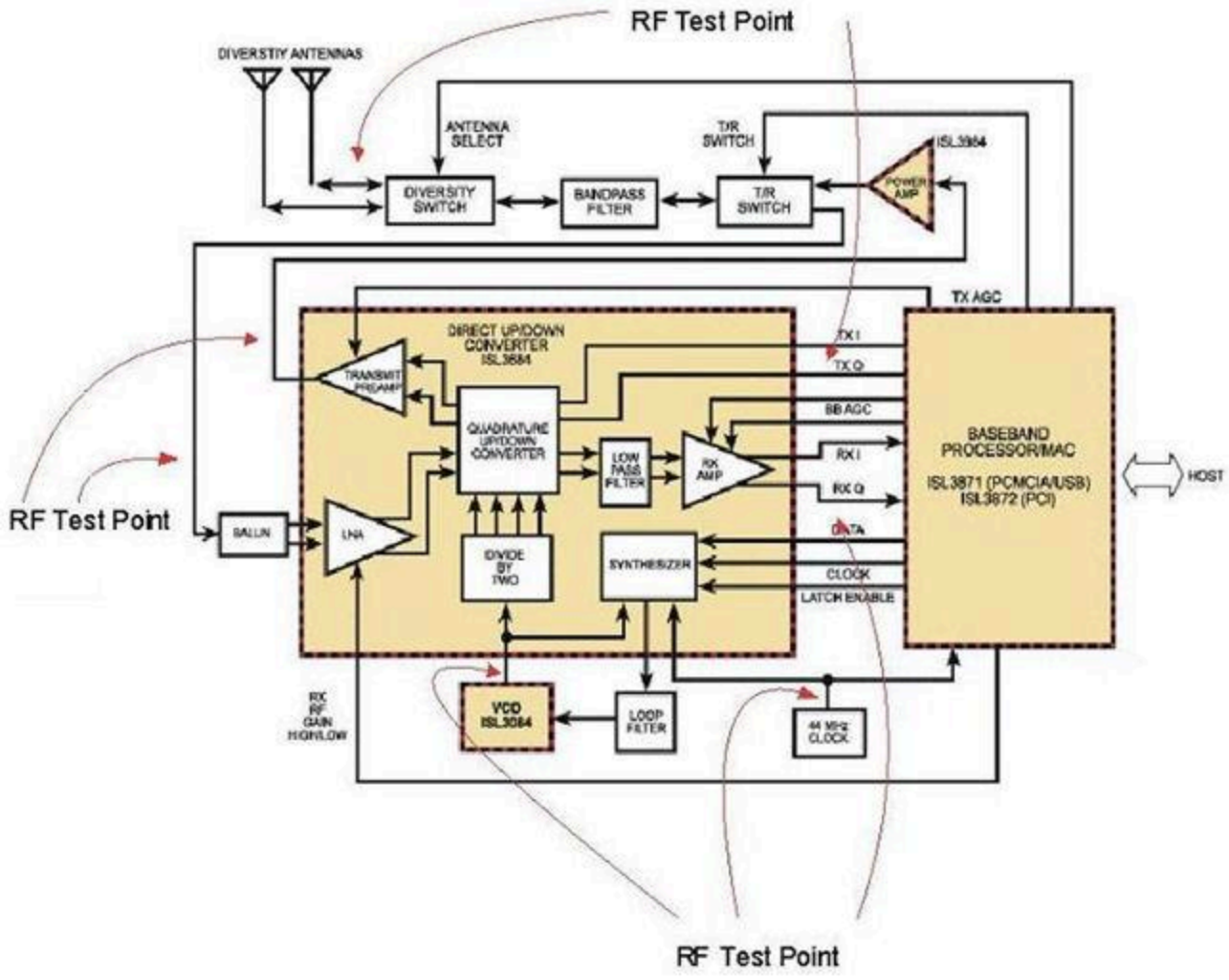
CID: 2	Content Owner: Jabil	Content Type: Requirement

In general, test points should be added to allow for fault isolation down to the component level, improving failure detection.

The test points will add cost and cause impedance variations in the RF circuit and need to be taken into account to avoid performance issues. The tradeoff between testability and performance impact needs to be considered when test points are designed into the product.

Examples of typical RF test points:

- TX I/Q - For verification of transmitted base band signal
- VCO Output - For verification of the frequency stability of the VCO
- Clock Output - For verification of the integrity of the clock signal
- Pre-Amp Output - For verification of the Pre-Amp signal level
- Power Amp Output - For verification of the output power of the device
- LNA input - For verification of the receiver input signal
- RX I/Q - For verification of the receiver base band signal
- Data/Clock/Latch enable - For verification of proper I/O communication between MAC processor and Synthesizer



These are sample test points based on a typical radio block diagram. The actual test points will vary, depending on the design of the product.

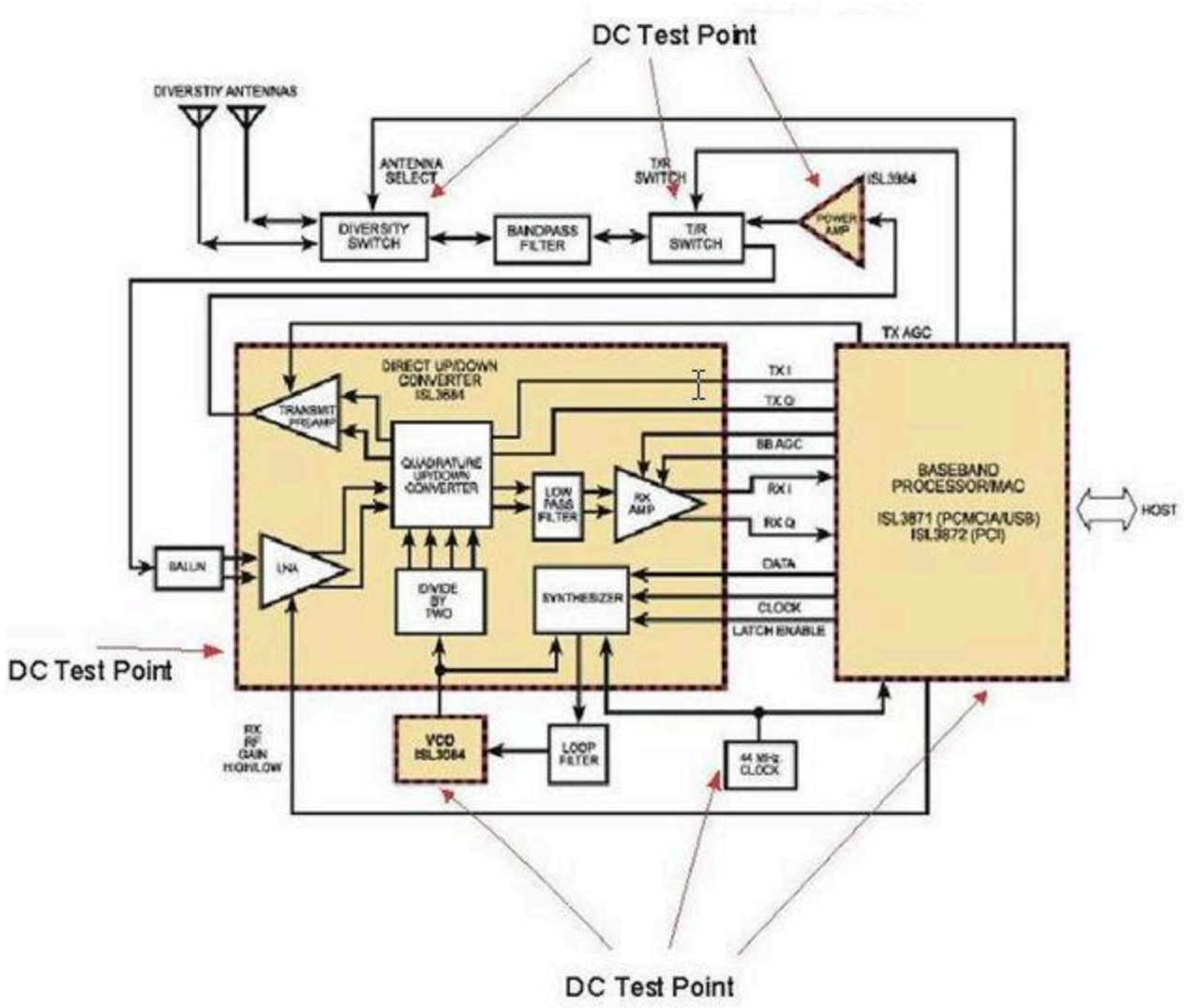
CID: 3	Content Owner: Jabil	Content Type: Requirement

RF DC test points allow ICT, or other test methods, to check for proper DC distribution and bias to the active components, and whether shorts or opens are present before continuing to the next process step. These DC checks are critical and prevent the risk of damage to the RF components. DC test points should be designated to the following.

Examples of where typical RF DC test points should be placed:

- DC Power Supply
- Voltage Regulator
- MAC Base-Band Processor IC DC input
- Up/Down Conversion IC DC input
- Clock DC input
- VCO DC input
- Synthesizer DC input

- Power Amplifier DC input
- T/R Switch DC input
- Diversity Switch DC input



These are sample test points based on the block diagram provided. The actual test points will vary, depending on the design of the product.

DFT > Electrical Requirements > General
Entry ID: 1422

Test Point Access

Rule

CID: 2 Content Owner: Jabil Content Type: Requirement

Provide optimum access for test points; every functioning (used and unused) pin and non-functioning unused pin on components. Test access to these pins is required because shorts and opens between them and other pins can cause test failures at the ICT and Functional level.

Aspect	Specification
Test Access	Required - One test point for every functioning pin, functioning unused pin, and non-functioning unused pin.
	Acceptable Alternate 1 - One test point for every functioning pin and functioning unused pin.
	Acceptable Alternate 2 - One test point for every functioning pin.

CID: 3 Content Owner: Jabil Content Type: Requirement

Access to the following signals is required and should not be selected for nodal reduction. These critical signals enable the use of alternate test methods such as Boundary Scan, Nandtree, and also allow for easy disabling / control of devices on the board.

If nodal reduction is being considered, test points on the following signals are critical:

- CS - Chip Select
- CE - Chip Enable
- TDI - Test Data Input
- TDO - Test Data Output
- TMS - Test Mode Select
- TCK - Test Clock
- TRST - Test Reset
- OE - Output Enable
- Nandtree Test Pins

DFT > Electrical Requirements > General
Entry ID: 1710

Probe Selection for Printed Electronics

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

For printed electronics, spring loaded probe testing using silver inks: select flat headed probes with a large surface area and extra force.

- This probe style and force setting provides the lowest resistance measurements during testing.

Related Entries

DFM	Guideline	1801	Printed Electronics > General > Layout for Screen Printed and Flexible Hybrid Electronics
DFM	Guideline	1621	Printed Electronics > General > Thermoformed Printed Electronics
DFM	Information	1564	Printed Electronics > General > Printed and Flexible Hybrid Electronics General Information

DFT > Electrical Requirements > General
Entry ID: 1762

Flip-Flop Devices

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Ensure that flip-flop devices can be controlled. CLR and PRE pins should not be tied to power or ground rails and must have test point access.

- Flip-flop devices cannot be initialized and all states cannot be tested when CLR and PRE pins are tied to power and ground rails. Please use pull-up or pull-down resistors on these pins and ensure they are test point accessible so flip-flops can be fully tested during manufacturing test.

DFT > Electrical Requirements > General
Entry ID: 1763

Digital Devices

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Ensure that all digital devices have a method of disabling or conditioning their outputs with test point access.

- Devices without disable methods will interfere with adjacent device tests causing unreliable conditions. If on-board FLASH programming is required, then each device on data and address busses common to the FLASH device must have a method so they can be disabled.

Related Entries

DFT Guideline 1090 Electrical Requirements > General > Output Enable Lines for ICs
DFT Guideline 1127 Electrical Requirements > Boundary Scan > Access for Memory Devices
DFT Guideline 1100 Electrical Requirements > General > Control Pins

DFT > Electrical Requirements > General
Entry ID: 1764

Crystals

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Verify that crystals have a buffered output and test point access.

- Unbuffered crystals may be untestable resulting in a loss of test coverage.
- Lack of test point access will result in a loss of test coverage and defect escapes.

Related Entries

DFT Guideline 1089 Electrical Requirements > General > Oscillator Output Enable Pins
DFT Guideline 1092 Electrical Requirements > General > Clock-Generating Devices

DFT > Electrical Requirements > Boundary Scan
Entry ID: 1118

ASICS and Other High Pin Count Packages

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Test ASICS and other high pin count packages using Boundary scan with vectorless test. If boundary scan is unavailable, employ NandTree with vectorless test. If NandTree is unavailable, employ Custom Simulation Vectors with vectorless test as a final option. Custom simulation vectors are not preferred due to the long development times required.

In order to increase test coverage, the addition of vectorless Testing methods including TestJet, VTEP, and OpensExpress should be used on high pin count packages.

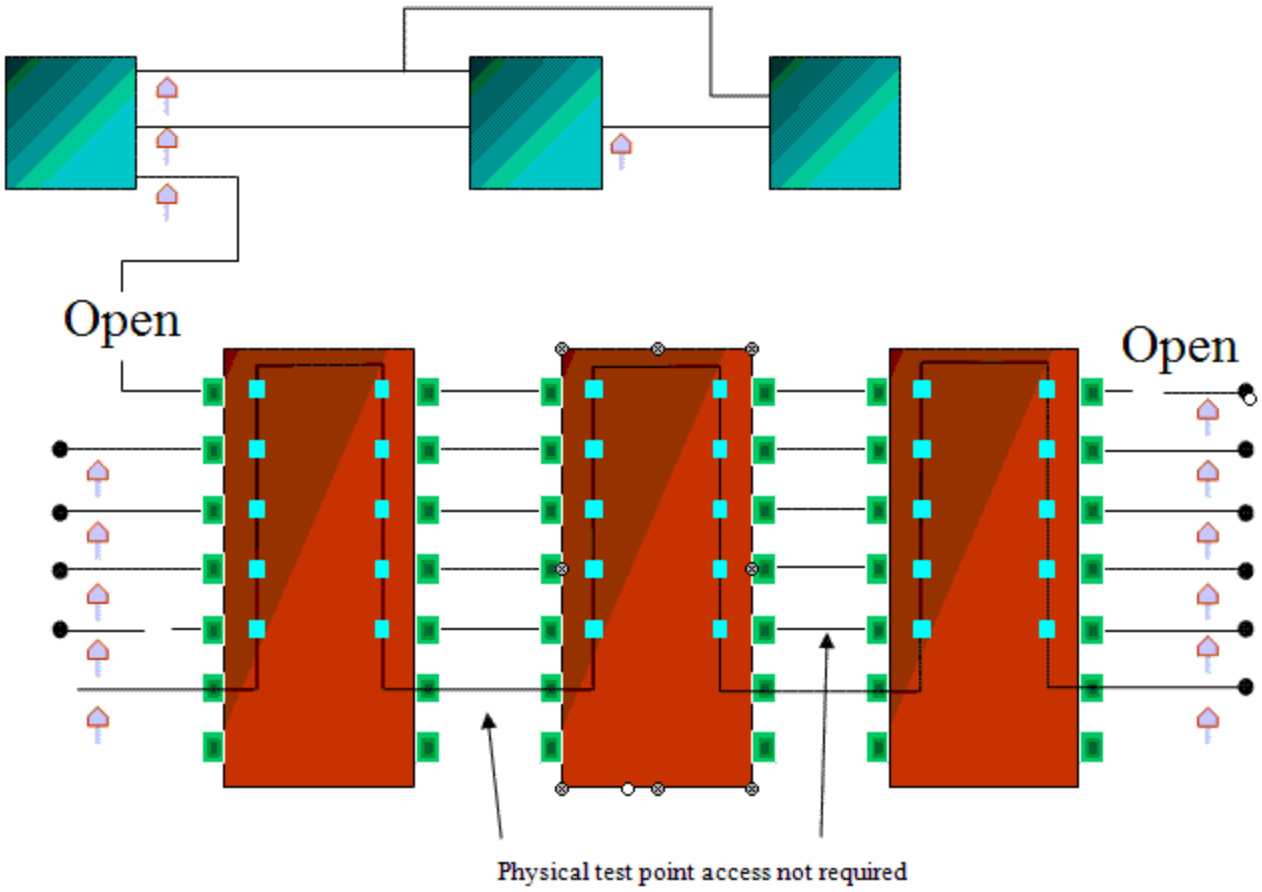
DFT > Electrical Requirements > Boundary Scan
Entry ID: 1119

Maximize Test Coverage

Guideline

CID: 2 Content Owner: Jabil Content Type: Requirement

Provide test point access for all pins on boundary scan devices. If test point count reduction is needed due to tester limitations or board real estate issues, interconnect pins (pins directly connected from one boundary scan device to another) may have test point access eliminated. This test method employs what are known as "virtual" test points.



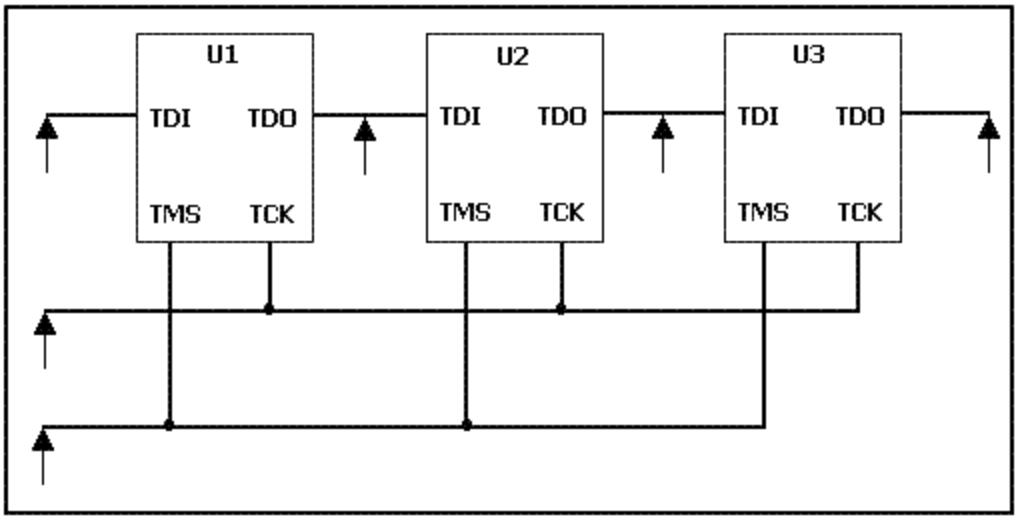
Interconnect Pins

CID: 3 Content Owner: Jabil Content Type: Requirement

Use chaining to optimize test coverage when access is limited. Test access limitations can be caused by the lack of board real estate, tester resource limitations, etc.

Chaining allows for test point count reduction by enabling the use of virtual test points between chained boundary scan devices and provides for the testing of multiple devices with a single Test Access Port.

To configure a boundary scan chain, Connect TDO of device U1 to TDI of device U2, TDO of device U2 to TDI of device U3, etc. TMS and TCK of all devices in the chain should be connected in parallel. Buffers may be required for TMS, TRST and TCK if chaining more than 3 devices.

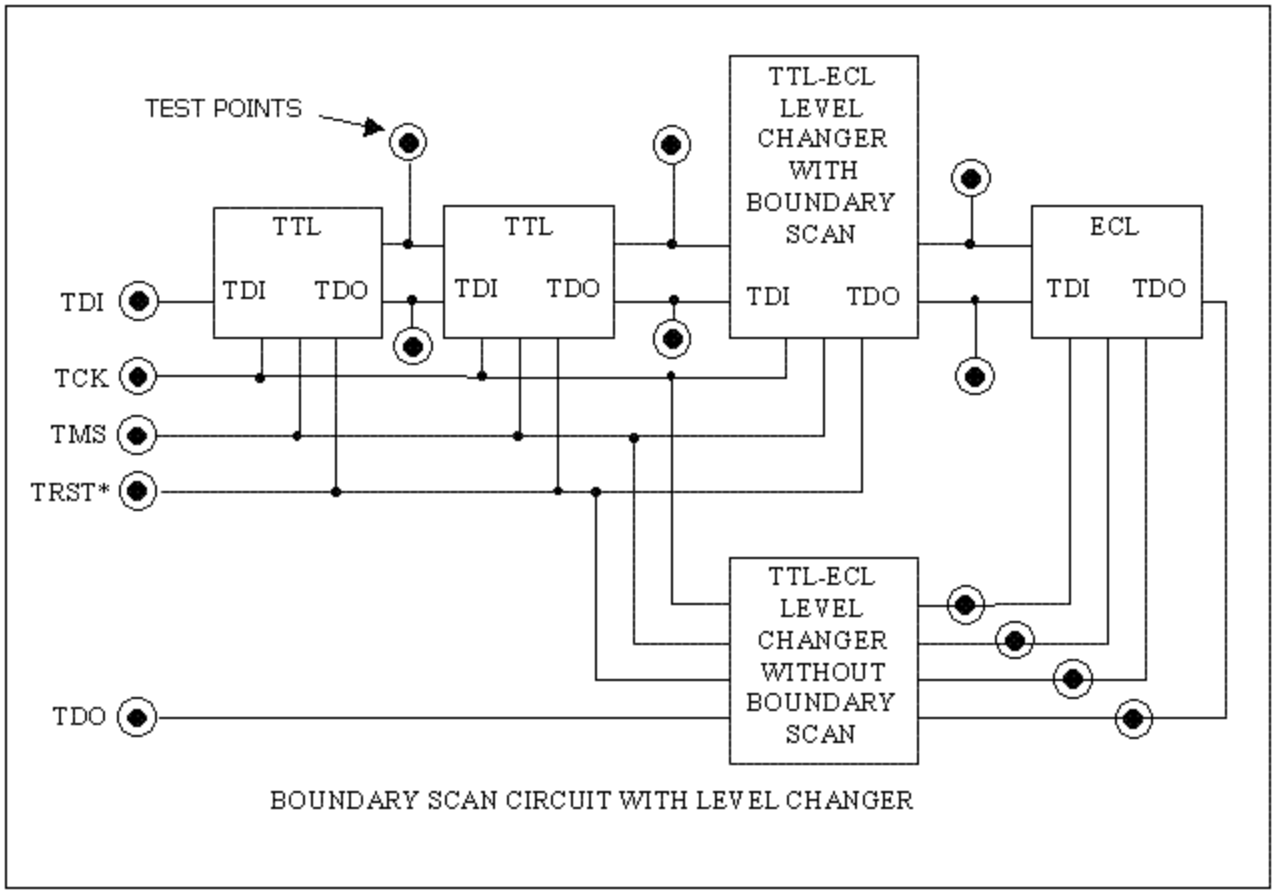


CID: 4	Content Owner: Jabil	Content Type: Requirement

Place flash memory devices that require programming in an isolated boundary scan chain to minimize the chain length during programming and allow the flash chain to run at its maximum speed.

CID: 5	Content Owner: Jabil	Content Type: Requirement

Different voltage technologies such as ECL and TTL on one board require a separate chain for each technology. If a separate chain is not possible, a logic level converter (changer) will be necessary.



CID: 6	Content Owner: Jabil	Content Type: Requirement

A cluster test that utilizes an optical link requires an isolated chain.

CID: 7	Content Owner: Jabil	Content Type: Requirement

If the cluster components require a separate clock for testing, an isolated chain must be utilized.

CID: 8	Content Owner: Jabil	Content Type: Requirement

Boundary scan cells which control non-boundary scan buffers, tri-state enable pins, boundary scan enable signals, etc. must be part of an isolated chain.

CID: 9	Content Owner: Jabil	Content Type: Requirement

Boundary scan components should be fully IEEE 1149.1 compliant. If only partially compliant, they may cause interference and need to be in their own isolated chain.

CID: 10	Content Owner: Jabil	Content Type: Requirement

When utilizing vendor JTAG proprietary software tools for in system programming of CPLDs and/or in system emulation (DSP), an isolated chain is required.

DFT > Electrical Requirements > Boundary Scan
Entry ID: 1120

Component and Attribute Selection

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Select devices with the following attributes to enhance fault detection during boundary scan test:

- Devices that generate control signals such as OE, CS, DIR, etc. should be selected for boundary scan. Control signals are also often generated by PLDs, use boundary scan compatible CPLDs when available.
- Devices that provide access to a majority of the components on the board should be selected for boundary scan. Typically this will include the CPU with access to the address bus, data bus, and control lines to which many other components are connected.

CID: 3	Content Owner: Jabil	Content Type: Requirement

During the selection of boundary scan devices, consider that a fault on a net can be detected provided the following attributes are implemented:

- At least one boundary scan output and input cell are connected to the net.
- At least one boundary scan cell and a memory pin are connected to the net.
- The net is connected to another net via a transparent device, such that the two nets are logically equivalent if the device is replaced by a wire. Both nets must have at least one boundary scan cell connected to it. **Note:** Transparent devices may be passive or active. Passive transparent devices are series resistors and jumpers. An example of an active transparent device is a buffer.
- At least one boundary scan cell and physical access to a test point on the same net.

These options state the minimum requirements for fault detection and are sufficient for detecting net faults. However, the diagnostic resolution is improved when more boundary scan pins are present on the same net. A high diagnostic resolution minimizes the repair time in production.

Ensure boundary scan components are fully IEEE 1149.1 compliant.

- Boundary scan components that are not fully IEEE 1149.1 compliant do not support JTAG testing and may cause interference with other JTAG components.
- Please use components that are fully compliant or place this partially compliant component in an isolated chain.

Ensure that high-speed AC coupled interconnecting signal nets support IEEE 1149.6 on all device pins.

- If a driver or receiver device pin on a high-speed AC coupled interconnecting signal net does not support IEEE 1149.6, open fault coverage will be lost resulting in reduced test coverage.

DFT > Electrical Requirements > Boundary Scan
Entry ID: 1121

Programming Requirements for Boundary Scan

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

In order to program a CPLD using boundary scan, the Program Enable pin should be made accessible over an unused boundary scan pin or can be made active via a jumper or dedicated connector pin.

CID: 3	Content Owner: Jabil	Content Type: Requirement

To allow testing of a PLD without boundary scan functionality possible, add a transparent mode to its logic function that can be switched on by an unused boundary scan pin.

Optionally, boundary scan functionality can be added temporarily if the PLD can accommodate the additional code.

CID: 4	Content Owner: Jabil	Content Type: Requirement

The output of non-boundary scan compliant devices should not drive boundary scan nets. These devices are called parallel devices which can be uncontrollable and negatively affect the boundary scan test. Isolate boundary scan nets from non-boundary scan compliant devices.

DFT > Electrical Requirements > Boundary Scan

Entry ID: 1122

Non-Boundary Scan Compliant Active Components

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Non boundary scan compliant active components that drive a boundary scan net need to be placed in tri-state mode to prevent multiple drivers on the net. Place the device in tri-state mode by utilizing unused boundary-scan pins from PLDs or FPGAs or by direct access to a connector pin.

DFT > Electrical Requirements > Boundary Scan
Entry ID: 1123

Boundary Scan Clusters

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

When utilizing boundary scan to apply test vectors to a cluster, the logical depth of the cluster should be limited to a single non-boundary scan compliant component. If the cluster has been simulated with the help of a fault simulator, reuse the input stimuli and the output values that have been generated.

DFT > Electrical Requirements > Boundary Scan
Entry ID: 1125

Functional Mode Following Power-on or Reset

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Circuitry assuring device functional mode rather than boundary scan mode should be provided. Some devices may initialize in an unknown boundary scan state after reset or power up. Functional mode of any boundary scan compliant device is guaranteed by applying at least 5 TCK cycles while holding TMS high. Additional TCK cycles after 5 have no effect if TMS is high.

Another option is to apply a low to the asynchronous reset TRST when supported. TRST should not be tied to the master board reset as this may adversely effect boundary scan testing. Another boundary scan device should not be used to drive the TRST signal inputs.

DFT > Electrical Requirements > Boundary Scan
Entry ID: 1127

Access for Memory Devices

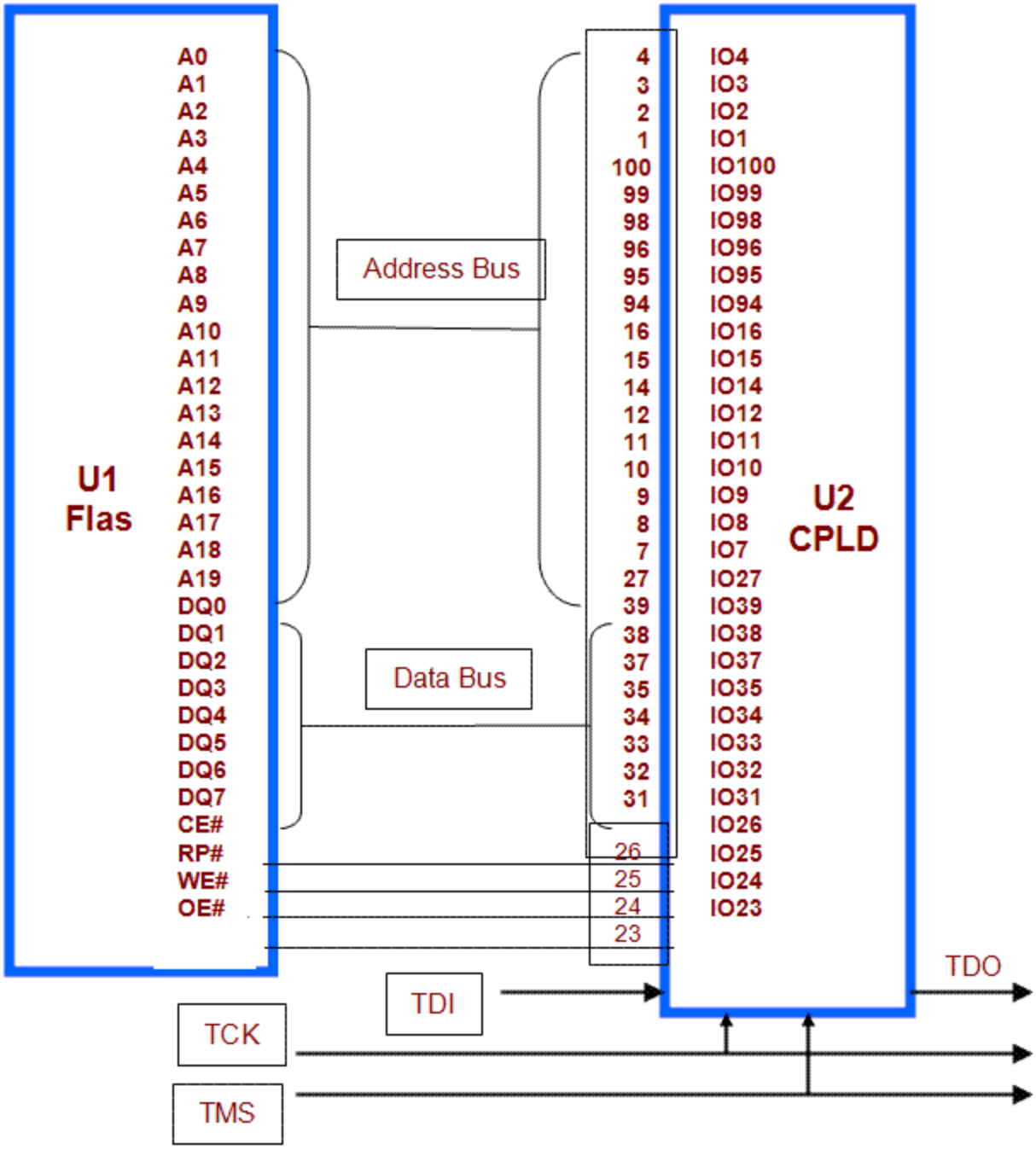
Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Connect all memory address lines, data lines and control lines (including clocks) to boundary scan pins. This makes it possible to test and program FLASH using the boundary scan chain.

An independent tri-state boundary scan pin should be used to access the write-enable pin on FLASH devices and be directly accessible through the TAP connector.

When testing DRAM devices, the RAS/CAS signals should be directly accessible via the scan chain.If the signals are not directly accessible, shifting in a large chain combined with a slow TCK might not meet the timing requirements resulting in a loss of data.



DFT > Electrical Requirements > Boundary Scan
Entry ID: 1765

Boundary Scan Requirements

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Ensure that a verified BSDL file is available for each JTAG device.

- A BSDL file describes how the boundary scan architecture has been implemented in a device. The information in the file is used to determine how to access and test the device in a JTAG chain.

Identify compliance enable pins or conditions for each JTAG device.

- Compliance enable pins are pins that need to be controlled in a specific way to allow the device to operate in JTAG mode.

Avoid tying compliance enable pins directly to power and ground planes.

- Compliance enable pins should not be tied directly to power or ground to achieve the compliance condition.
- The compliance enable condition should be implemented in the design by pulling the pin low or high with a resistor.

Ensure that compliance enable pins are test point accessible.

- Compliance enable pins should be accessible through test points so they can be forced to the correct level for JTAG testing when the PCB is placed on a test fixture.

CID: 3	Content Owner: Jabil	Content Type: Requirement

Ensure that all JTAG signals for each boundary scan chain are physically accessible, ideally through a connector or alternatively through isolated test points.

- There is no established standard for the actual pin-out or mechanical definition for a JTAG TAP connector. Best practice, at a minimum, is to expose each JTAG signal used in the chain (TDI, TDO, TMS, TCK, TRST) through a PCB mounted mechanical connector or through isolated test points.

Ensure that TDI starts from the TAP connector and runs to TDI of the first device then daisy-chains from the TDO pin to TDI of the next device and continues in this fashion for each device in the boundary scan chain. TDO from the last device should return to TDO of the TAP connector.

- Boundary scan devices can be chained together.

Ensure that a low value series termination resistor is in-line between the TDO pin of the last device in the boundary scan chain and the TAP connector.

- A 33ohm series resistor should be placed as close as possible to the TDO pin of the last device in the chain to drive the line toward the boundary scan controller.

Ensure that all devices in the boundary scan chain are running at the same voltage level.

- All signal levels at the TAP controller interface must be consistent.

Ensure that the input and output translation voltage pins of voltage translator ICs are connected to the correct power rails where the respective JTAG devices are connected.

- Logic level translator ICs are used in multi-voltage systems for signal transfers between devices operating at different voltage levels.

Ensure that TMS runs from the TAP connector and connects in parallel to TMS of each IC in the JTAG chain.

- TMS must run from the TAP port and connect in parallel to TMS of each IC in the JTAG chain.
- When there are a large number of JTAG devices in the chain, it may be necessary to buffer TMS to provide separate "copies" of TMS to individual devices to reduce the signal loading.

When TMS is distributed to a JTAG device on the chain that is running at a translated voltage, ensure that the TMS signal has been run through a voltage translator IC so it matches the operating voltage of the JTAG device.

- Operating voltage levels can vary between devices in a scan chain. The TMS signal must be run through a voltage level translator IC when connecting to the TMS pin of a JTAG device running at different voltage level on the same chain.

Ensure that TCK runs from the TAP connector and connects in parallel to TCK of each IC in the JTAG chain.

- TCK must run from the TAP port and connect in parallel to TCK of each IC in the JTAG chain.
- When there are a large number of JTAG devices in the chain, it may be necessary to buffer TCK to provide separate "copies" of TCK to individual devices to reduce the signal loading.

When TCK is distributed to a JTAG device on the chain that is running at a translated voltage, ensure that the TCK signal has been run through a voltage translator IC so it matches the operating voltage of the JTAG device.

- Operating voltage levels can vary between devices in a scan chain. The TCK signal must be run through a voltage level translator IC when connecting to the TCK pin of a JTAG device running at a different voltage level on the same chain.

Ensure that TRST runs from the TAP connector and connects in parallel to any JTAG devices in the chain that support TRST.

- TRST must run from the TAP port and connect in parallel to TRST of any device in the JTAG chain that supports TRST.

- When there are a large number of JTAG devices in the chain, it may be necessary to buffer TRST to provide separate "copies" of TRST to individual devices to reduce the signal loading.

When TRST is distributed to a JTAG device on the boundary scan chain that is running at a translated voltage, ensure that the TRST signal has been run through a voltage translator IC so it matches the operating voltage of the JTAG device.

- Operating voltage levels can vary between devices in a scan chain. The TRST signal must be run through a voltage level translator IC when connecting to the TRST pin of a JTAG device running at a different voltage level on the same chain.

Ensure that TRST is NOT tied to GND, VCC, or any other active signal on the PCB.

- Designers should avoid connecting TRST to other signals so the device is not dropped from JTAG mode during boundary scan testing.

Ensure that all intermediate TAP pins (TDO to TDI connections) on the boundary scan chain have test point access.

- All intermediate points along the scan chain should have test point access to allow the scan chain to be easily broken up and / or simplified for diagnostic purposes or management of non-responsive JTAG device conditions.

CID: 4	Content Owner: Jabil	Content Type: Requirement

Things to consider for the guidelines below:

- Are external termination resistors in the design oriented in the same direction as the internal termination resistors inside the JTAG device? (e.g. external termination resistor is a pull-up on TDI line which matches the internal pull-up resistor on TDI pin of JTAG device).
- Do external termination resistor values fall in the range suggested by device vendors?
- When device vendor recommendations are vague or not available, default to the termination recommendations in EID 1126 (which are what the IEEE 1149.1 spec recommends). **Note:** device vendor termination recommendations often deviate wildly from the 1149.1 termination suggestions.
- When you run across a conflict, best practice is to stick with the device vendor recommendations keeping in mind that a boundary scan chain that works is the end goal.
- Another approach to consider when insurmountable termination conflicts occur is placing pads for BOTH a pull-up and a pull-down resistor for each TAP pin.
- Place the termination resistor on one and leave the other open. This provides the option for customer to try both and see which works best during prototyping.

Ensure that external TAP port pins TDI, TCK, TMS, and TRST require external termination resistors.

- External termination resistors are recommended for JTAG TAP pins TDI, TCK, TMS, and TRST unless all devices in this scan chain have internal termination resistors and external terminations are not recommended by the vendors.

Ensure that external termination resistors in the design are oriented in the same direction as the internal termination resistors inside the JTAG device.

- External termination resistors for JTAG TAP pins TDI, TCK, TMS, and TRST should be oriented (pulled-up or pulled-down) to match the direction of the internal termination resistors of devices on the scan chain.

Ensure that external TAP termination resistor values for TDI, TCK, TMS, and TRST are within the range suggested by device vendors.

- Device vendor TAP termination recommendations often deviate from the IEEE 1149.1 standard termination guidance. Best practice is to follow with the resistor values and orientations that the device vendor recommends.

DFT > General Test > Functional Test
Entry ID: 1011

Product Functionality and External Connections

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

An assembly that will require functional test should be designed to allow its functionality to be verified through external connections. All power, stimuli and responses should be applied and measured through connectors.

Any internal node requiring examination during testing should have an access point compatible with mechanical fixturing used in a production environment. It is not acceptable to clip or solder directly onto components in order to gain access to a node. A lack of connectors may cause a reduction in test coverage and may increase the cost of fixturing. Through connector module designs may also increase the cost of fixturing.

DFT > General Test > Functional Test
Entry ID: 1012

Adjust-on-Test Techniques

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

The use of adjust-on-test techniques should be avoided, unless absolutely essential to achieve a tolerance value necessary for a transfer function. In cases where this technique is unavoidable, easy access to adjustable components should be provided.

DFT > General Test > Functional Test
Entry ID: 1013

BIST and Board Level Diagnostics

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

In cases where BIST or board level diagnostics are utilized, the test code should be designed to allow the test equipment or program to have complete control over the startup and each step. This will allow the test equipment to be completely in sync with the assembly and additional processing between steps. The test equipment should control the code through a command line interface, or a sequence of hardware prompts.

DFT > General Test > Functional Test
Entry ID: 1014

Stored State Device Reset

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Reset all stored state devices into a known state in one step during initialization of the assembly. Doing so allows the test equipment to bring the assembly to a known state at any time during testing. The ability to perform this in one step allows a shorter test time. An exception is any device that needs several clock cycles to fully reset.

DFT > General Test > Functional Test
Entry ID: 1141

Control of Significant Circuits

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Provide software control of analog switches to maximize the flexibility of Functional test and to decrease test times.

CID: 3	Content Owner: Jabil	Content Type: Requirement

Sample and hold circuits driven by on board oscillators should have a means of being turned constantly on to increase the flexibility of functional test and reduce test time.

CID: 4	Content Owner: Jabil	Content Type: Requirement

Emergency circuits, such as over-temperature trips, should have a means of forced operation to enhance control at functional test.

DFT > General Test > Functional Test
Entry ID: 1142

Design for Diagnostics

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

Test Access should be provided to critical signals such as Clocks, Resets, and Read/Write Enables when the product is in the final assembly stage. This will prevent unnecessary disassembly if troubleshooting is required.

CID: 3	Content Owner: Jabil	Content Type: Requirement

To reduce the risk of introducing power to ground shorts, ensure they are not routed to adjacent terminations (e.g. pins, jumpers, leads, resistor networks).

CID: 4	Content Owner: Jabil	Content Type: Requirement

For complex systems with limited access, design a debug chassis to ensure easy signal probing access to the topside and bottom side of the PCB. The debug chassis should maintain normal operation of the unit.

CID: 5	Content Owner: Jabil	Content Type: Requirement

If the final product consists of multiple assemblies, tests should be written to allow each subassembly to be tested in a standalone configuration.

CID: 6	Content Owner: Jabil	Content Type: Requirement

Manufacturing diagnostics should be designed to provide remote troubleshooting (e.g. Ethernet, RS232, Coaxial, USB).

DFT > General Test > Functional Test
Entry ID: 1144

Emulator Assisted Diagnostic Recommendations

Guideline

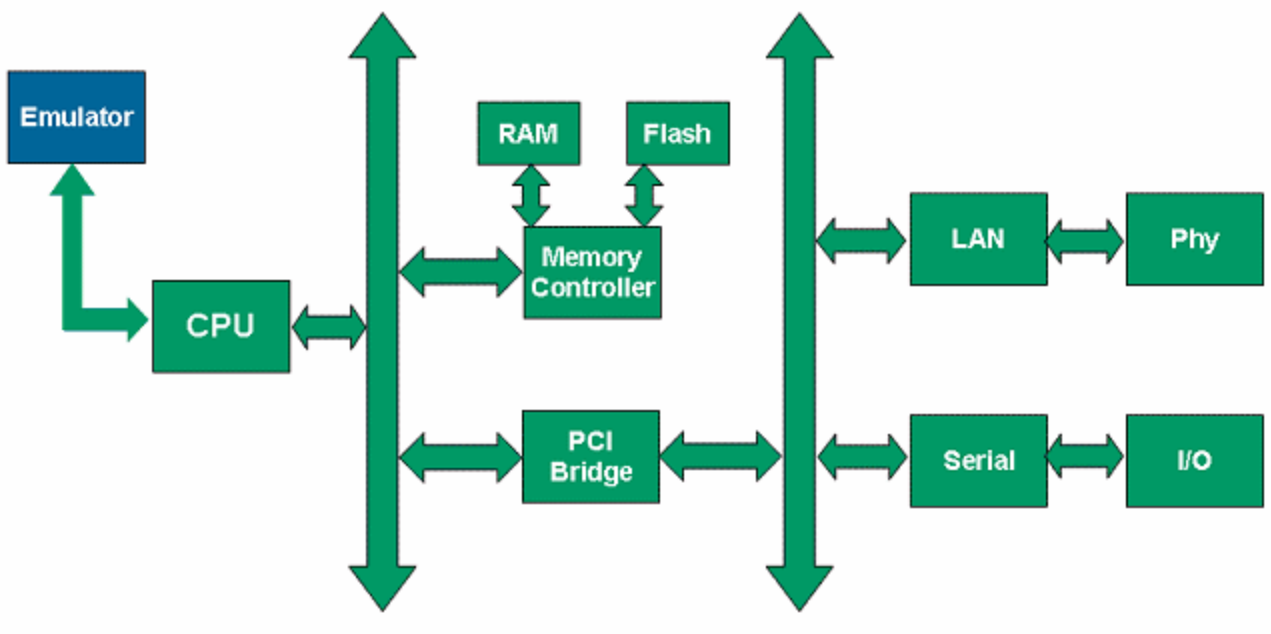
CID: 2	Content Owner: Jabil	Content Type: Requirement

Utilize the following emulator assisted diagnostic recommendations:

Debug systems: Used to isolate problems to root cause in the design environment should be made available for manufacturing test and debug. This includes any stand alone Boundary Scan, Emulation or other tools design engineers use during the development stage.

Boot process: In the event that a defective board can partially boot, an error output should be provided (e.g. Port 80 code, Led blinking, Heartbeat, etc.).

Control: Diagnostics should start with the simplest functional block and expand towards other devices. The diagram below gives an example of a simplified block diagram of a CPU based system. The test would start by exercising the CPU and work its way through the functional blocks of the assembly.



Functional Blocks

DFT > Software Requirements > General
Entry ID: 1150

Unused Addresses in ROMs and EPROMs

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

When ROMs and EPROMs are included in the design, designated unused addresses should be used to store software revision information. Revision addresses should not change from revision to revision. If revision information is not consistently located at the same address, additional test development will be required.

Any additional unused addresses should be used to provide test patterns on data outputs. If test patterns are available, it will simplify testing of the device as the patterns are already in place and will not have to be created.

DFT > Software Requirements > General
Entry ID: 1151

Functional Test Software Failure Reporting Standards

Guideline

CID: 2 Content Owner: Jabil Content Type: Requirement

Failure message output should be in a form that is easy to parse for automated data collection. Data for a failing test should contain:

- The executed test that failed
- Expected result
- Detected result (why the test failed)
- Specific environmental and operating conditions, temperature readings, fan speed, voltage, etc. if applicable.
- To maximize coverage and fault isolation, diagnostic requirements should be addressed during the conceptual design phase. This will ensure that higher granularity test steps are defined and will provide better diagnosis and data collection.

Below is an example of a granular test step error message:

```
Error Code:             84
Packet Size:            1518
Data Pattern:           0x00
Access Type:            Byte
Mode Type:              Complement
Increment Value:        0x01
No Of Packets:          32
Bay Number:             3
Port Number:            1
Loopback Level:         2
Circulate:              Yes
Pause:                  3
Simultaneous:           No
Run Count:              1
Test Fail Count:        1
Error Count:            1
Fail Address:           0x81001BA8
Data Expected:          0x00000020
Data Read:              0x00000000
Error Message:          RX_TIMEOUT_ERROR
Total test time:        12s
```

A reference table should be provided for any coded error messages. This table will help technicians understand the meaning of the error codes.

If possible, the ability for a single test to stop-on-fail, loop-on-fail and loop-until-fail should be available for effective troubleshooting.

If capabilities for voltage and frequency margining exist, on-board diagnostics should exercise this capability.

DFT > Software Requirements > General
Entry ID: 1152

On-Board Product Diagnostic Software Recommendations

Guideline

CID: 2	Content Owner: Jabil	Content Type: Requirement

On-board product diagnostic software recommendations:

- After software initialization, provide a Command Line Interface (CLI) to enable communication with the firmware and diagnostic software.
- During initialization of the board, short deterministic tests such as POST should be executed to provide initial results about the health of the PCB before doing any more comprehensive tests.
- Use multiple levels of on-board diagnostics with software options to enable or disable specific diagnostic output information. This will provide diagnostic technicians with the ability to select the appropriate amount of output information while still providing easy parsing for automated test data collection.
- Utilize peek and poke type commands that allow access to memory locations and CPU registers to enable low level troubleshooting.