3. How did the testbench test your implementation for part 1? (3 pts)

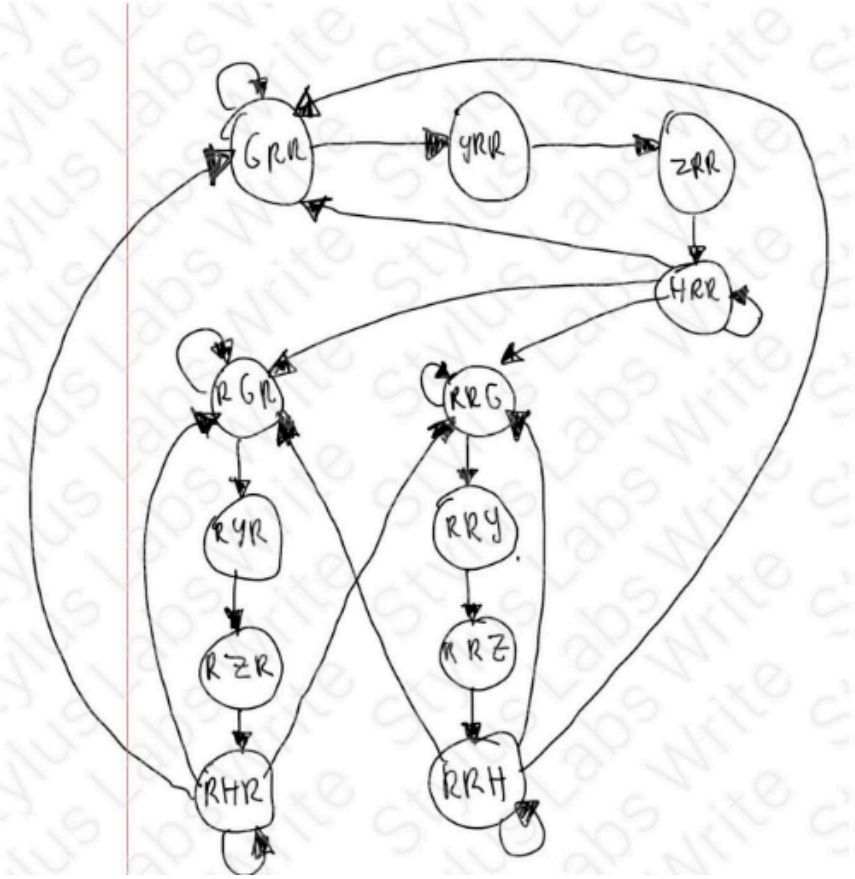
Word limit: 300 words

The testbench has a controller named “traffic_light_controller1” based on a clock signal. The controller can reset to red state, see which direction sensors are triggered, and display correct state (colors). The testbench makes 4 test cases. For each test case, a list of active sensors, resulting traffic light color, and timestamps, are printed into a .txt file. All Red states are blank lines.

State machine diagram part 1

It can be a picture or digital image. Please have a state for every state in the starter code (You can find the enums starting line 17 in traffic_light_controller1.sv)

TODO

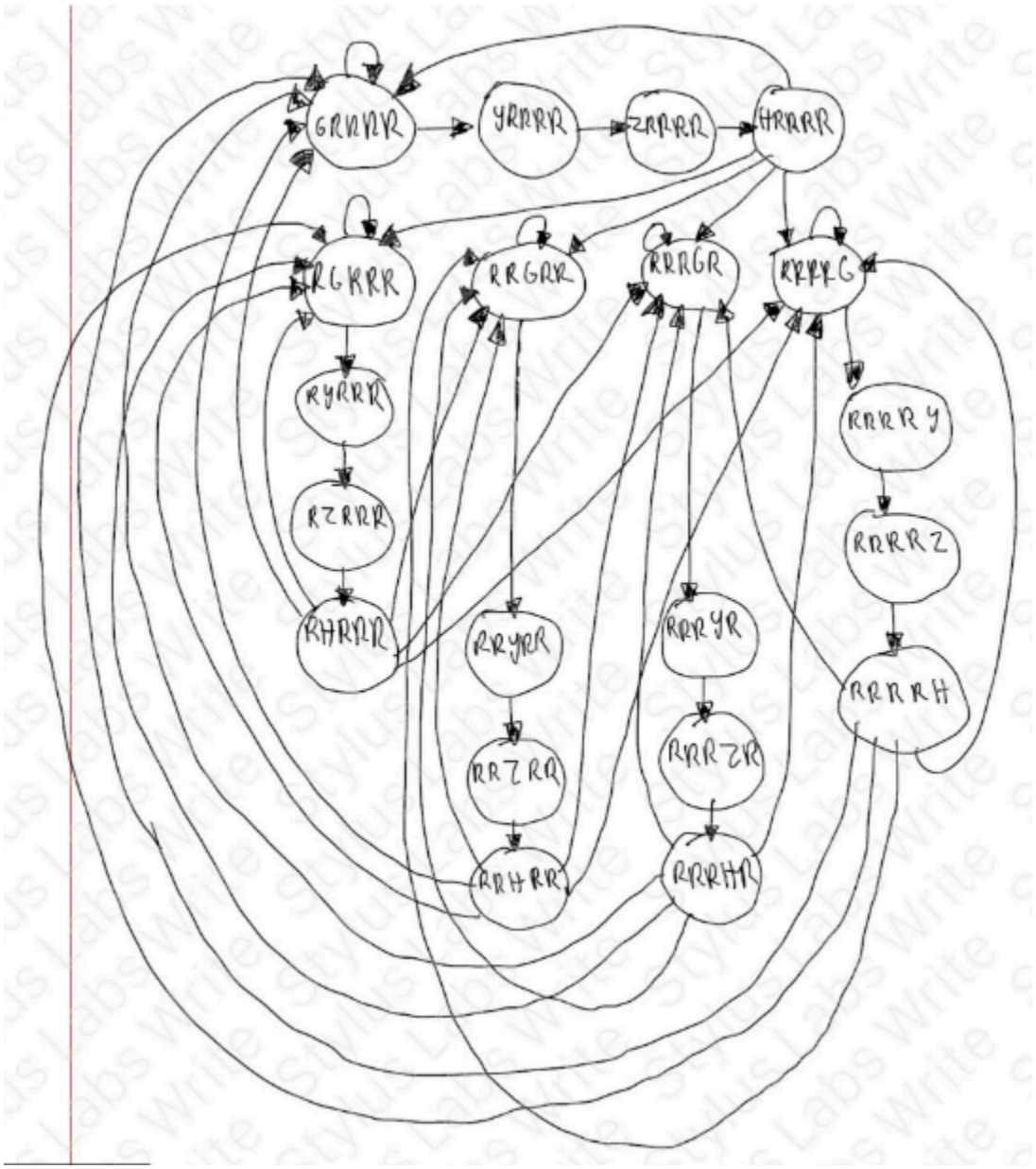


4. How did the testbench test your implementation for part 2? (3 pts)

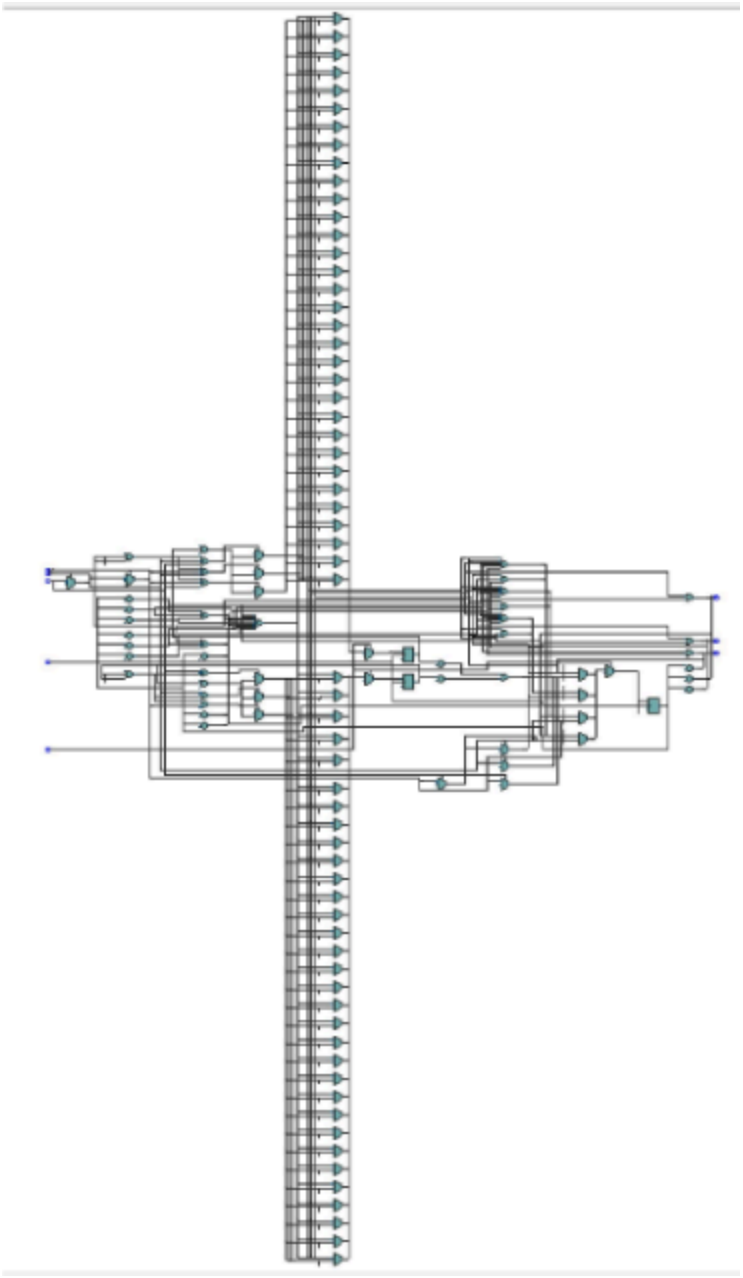
Word limit: 300 words

TODO:This testbench is similar to the 1st testbench, the controller works the same way. But more sensors and more states are needed. More testcases are introduced. The output.txt file is similar to the 1st one.

State machine diagram part 2:

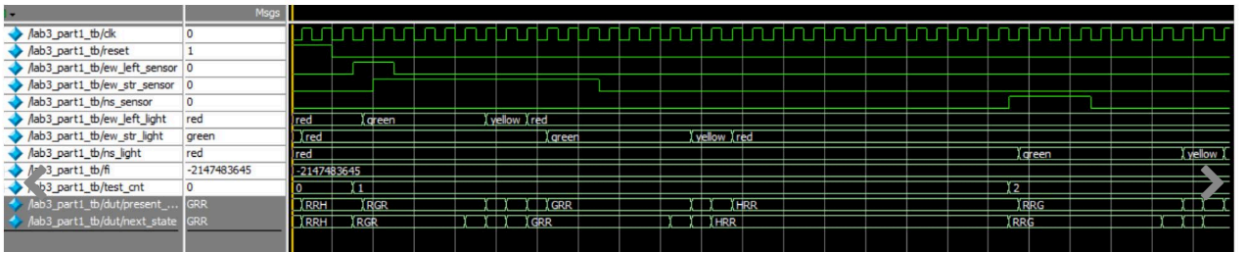


Part 1 waveform+rtl

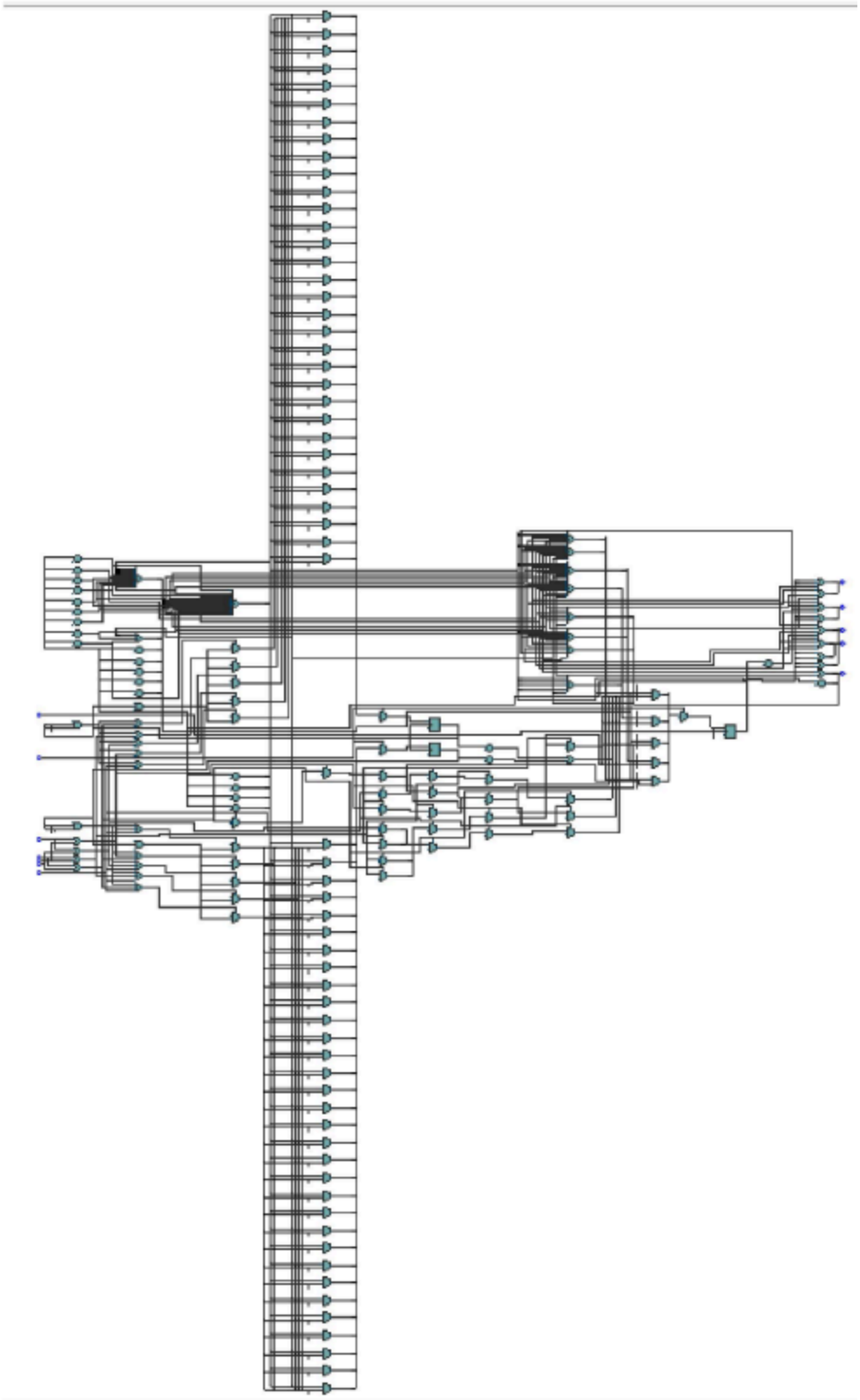


Screenshot of your waveform viewer, showing the presence of traffic and the states of the traffic signals. (3 pts)

TODO



Part 2 waveform+rtl



Screenshot of your waveform viewer, showing the presence of traffic and the states of the traffic signals. (3 pts)

TODO