module Lab3(input [0:3] X0, X1, input s, output [0:6] X0\_output, X1\_output, output [0:3] final, output [0:6] final\_output, output count, output [0:6] count\_output, h2,h4);

```
assign h2 = 7'b111111111;
assign h4 = 7'b11111111;
```

FourBitAdder f1(X0, X1, 0, final, count, s);

// Displaying X0\_output

 $\begin{array}{l} assign \ XO\_output[6] = \sim ((\sim X0[0] \ \& \ \sim X0[1] \ \& \ X0[2] \ \& \ \sim X0[3]) \ | \ (\sim X0[0] \ \& \ \sim X0[1] \ \& \ X0[2] \ \& \ X0[3]) \ | \ (\sim X0[0] \ \& \ X0[1] \ \& \ \sim X0[2] \ \& \ \times X0[3]) \ | \ (\sim X0[0] \ \& \ \times X0[1] \ \& \ \sim X0[2] \ \& \ \sim X0[2] \ \& \ \sim X0[3]) \ | \ (X0[0] \ \& \ \sim X0[3]) \ | \ (X0[0] \ \& \ \sim X0[3]) \ | \ (X0[0] \ \& \ \times X0[2] \ \& \ \sim X0[3])); \end{array}$ 

 $\begin{array}{l} assign \ XO\_output[4] = \sim ((\sim X0[0] \ \& \ \sim X0[1] \ \& \ \sim X0[2] \ \& \ X0[3]) \ | \ (\sim X0[0] \ \& \ \sim X0[1] \ \& \ \sim X0[2] \ \& \ \times X0[2] \ \& \ \sim X0[2] \ \& \ \times X0[2]$ 

 $\begin{array}{l} \operatorname{assign} \ X0\_\operatorname{output}[3] = \sim ((\sim X0[0] \ \& \ \sim X0[1] \ \& \ X0[2] \ \& \ \sim X0[3]) \ | \ (\sim X0[0] \ \& \ \sim X0[1] \ \& \ X0[2] \ \& \ \sim X0[3]) \ | \ (\sim X0[0] \ \& \ \sim X0[1] \ \& \ \sim X0[2] \ \& \ \sim X0[3]) \ | \ (\times X0[2] \ \& \ \sim X0[3]) \ | \ (\times X0[2] \ \& \ \sim X0[3]) \ | \ (\times X0[2] \ \& \ \sim X0[3]) \ | \ (\times X0[2] \ \& \ \sim X0[3]) \ | \ (\times X0[2] \ \& \ \sim X0[3]) \ | \ (\times X0[2] \ \& \ \sim X0[3]) \ | \ (\times X0[2] \ \& \ \sim X0[3]) \ | \ (\sim X0[2] \ \& \ \sim X0[3])); \end{array}$ 

 $\begin{array}{l} {\rm assign} \ XO\_{\rm output}[2] = \sim ((\sim X0[0] \ \& \ \sim X0[1] \ \& \ X0[2] \ \& \ \sim X0[3]) \ | \ (\sim X0[0] \ \& \ X0[1] \ \& \ X0[2] \ \& \ \sim X0[3]) \ | \ (X0[0] \ \& \ \sim X0[1] \ \& \ X0[2] \ \& \ \sim X0[3]) \ | \ (X0[0] \ \& \ \sim X0[1] \ \& \ X0[2] \ \& \ \sim X0[3]) \ | \ (X0[0] \ \& \ X0[1] \ \& \ \sim X0[2] \ \& \ X0[3]) \ | \ (X0[0] \ \& \ X0[1] \ \& \ \sim X0[2] \ \& \ \sim X0[3])); \end{array}$ 

 $\begin{array}{l} \operatorname{assign} \ XO_{\text{output}[1]} = & \sim & ((\sim X0[0] \& \ X0[1] \& \ \sim & \times \\ X0[2] \& \ \sim & \times \\ X0[3]) \mid & (\sim X0[0] \& \ X0[1] \& \ \times \\ X0[2] \& \ \sim & \times \\ X0[3]) \mid & (\times \\ X0[2] \& \ \sim & \times \\ X0[3]) \mid & (\times \\ X0[2] \& \ \sim & \times \\ X0[3]) \mid & (\times \\ X0$ 

 $assign \ X0\_output[0] = (\sim X0[0] \& \sim X0[1] \& \sim X0[2]) \mid (\sim X0[0] \& \ X0[1] \& \ X0[2] \& \ X0[3]) \mid (X0[0] \& \ X0[1] \& \sim X0[2] \& \sim X0[3]);$ 

 $\begin{array}{l} assign \ X1\_output[6] = \sim ((\sim X1[0] \& \sim X1[1] \& \ X1[2] \& \sim X1[3]) \ | \ (\sim X1[0] \& \ \sim X1[1] \& \ X1[2] \& \ X1[3]) \ | \ (\sim X1[0] \& \ X1[1] \& \ \sim X1[2] \& \ X1[3]) \ | \ (\sim X1[0] \& \ X1[1] \& \ \sim X1[2] \& \ \times X1[2] \& \ \times X1[2] \& \ \sim X1[2] \& \ \sim X1[2] \& \ \times X1[2] \& \ \sim X1[2] \& \ \times X1[2] \& \ \times X1[2] \& \ \sim X1[2] \& \ \sim X1[2] \& \ \times X1[2] \& \ \sim X1[2] \&$ 

 $\begin{array}{l} \operatorname{assign} \ X1_{-} \operatorname{output}[5] = & \sim ((\sim X1[0] \& \sim X1[1] \& \sim X1[2] \& X1[3]) \mid (\sim X1[0] \& \sim X1[1] \& X1[2] \& \sim X1[3]) \mid (\sim X1[0] \& \sim X1[1] \& X1[2] \& X1[3]) \mid (\sim X1[0] \& \times X1[1] \& \sim X1[2] \& \sim X1[3]) \mid (\sim X1[0] \& \sim X1[1] \& \sim X1[2] \& \sim X1[2]$ 

 $\begin{array}{l} \operatorname{assign} \ X1_{-} \operatorname{output}[4] = & \sim (\sim X1[0] \ \& \ \sim X1[1] \ \& \ \sim X1[2] \ \& \ X1[3]) \ | \ (\sim X1[0] \ \& \ \times X1[1] \ \& \ \sim X1[2] \ \& \ \times X1[2] \ \& \ \sim X1[2] \ \& \ \times X1[2] \ \&$ 

 $\begin{array}{l} \operatorname{assign} \ X1_{-} \operatorname{output}[3] = & \sim ((\sim X1[0] \& \sim X1[1] \& X1[2] \& \sim X1[3]) \mid (\sim X1[0] \& \sim X1[1] \& X1[2] \& X1[3]) \mid (\sim X1[0] \& X1[1] \& \sim X1[2] \& \sim X1[3]) \mid (\times X1[2] \& \sim X1[3]) \mid (\sim X1[2] \& \sim X1[3])); \end{array}$ 

 $\begin{array}{l} \operatorname{assign} \ X1\_\operatorname{output}[2] = \sim ((\sim\!X1[0]\ \&\ \sim\!X1[1]\ \&\ X1[2]\ \&\ \sim\!X1[3])\ |\ (\sim\!X1[0]\ \&\ X1[1]\ \&\ X1[2]\ \&\ \sim\!X1[3])\ |\ (X1[0]\ \&\ \sim\!X1[1]\ \&\ X1[2]\ \&\ \sim\!X1[3])\ |\ (X1[0]\ \&\ \sim\!X1[1]\ \&\ X1[2]\ \&\ \times\!X1[2]\ \&\ X1[2]\ \&\ \times\!X1[2]\ \&\ \times\!X1[2]\ \&\ \sim\!X1[2]\ \&\ \sim\!X1$ 

 $\begin{array}{l} \operatorname{assign} X1\_\operatorname{output}[1] = & \sim ((\sim X1[0] \& X1[1] \& \sim X1[2] \& \sim X1[3]) \mid (\sim X1[0] \& X1[1] \& \sim X1[2] \& X1[3]) \mid (\sim X1[0] \& X1[1] \& X1[2] \& \sim X1[3]) \mid (X1[0] \& \sim X1[1] \& \sim X1[2] \& \sim X1[3]) \mid (X1[0] \& \sim X1[1] \& \times X1[2] \& \sim X1[3]) \mid (X1[0] \& \sim X1[1] \& X1[2] \& \sim X1[3]) \mid (X1[0] \& \times X1[3]) \mid (X1[0] \& \sim X1[3]) \mid (X1[0] \& \sim X1[3]) \rangle \\ (\sim X1[0] \& \sim X1[1] \& \sim X1[2] \& \sim X1[3]); \end{array}$ 

```
assign count_output[6] = 1;
assign count_output[5] = \sim(count & \sims);
assign count_output[4] = \sim(count & \sims);
assign count_output[3] = 1;
assign count_output[2] = 1;
```

assign count\_output[1] = 1;

// Displaying count\_output

assign count\_output[0] =  $\sim$ ( $\sim$ count & s);

 $assign \ final\_output[6] = (((\sim final[0] \& \sim final[1] \& \sim final[2] \& \ final[3]) \mid (\sim final[0] \& \ final[1] \& \sim final[2] \& \ final[3]) \mid (final[0] \& \ final[1] \& \ final[2] \& \ final[3]) \mid (\Leftrightarrow \ final[1] \& \ final[2] \& \ final[3]) \mid (\sim final[0] \& \ final[1] \& \ final[2] \& \ final[3]) \mid (\Leftrightarrow \ fi$ 

 $\begin{array}{l} assign \ final\_output[5] = (((\sim final[0] \& \ final[1] \& \ \sim final[2] \& \ final[3]) \mid (\sim final[0] \& \ count[2] \& \ \sim final[3]) \mid (\sim final[0] \& \ \sim final[3]) \mid (\sim fi$ 

 $\begin{array}{l} assign \; final\_output[4] = (((\sim final[0] \; \& \; \sim final[1] \; \& \; final[2] \; \& \; \sim final[3]) \; | \; (final[0] \; \& \; final[1] \; \& \; \sim final[3]) \; | \; (final[0] \; \& \; final[1] \; \& \; \sim final[3]) \; | \; (final[0] \; \& \; final[2] \; \& \; \sim final[3]) \; | \; (\sim final[1] \; \& \; \sim final[3]) \; | \; (\sim final[0] \; \& \; \sim final[1] \; \& \; \sim final[3]) \; | \; (\sim final[0] \; \& \; \sim final[3]) \; | \; (\sim final[0] \; \& \; \sim final[3]) \; | \; (\sim final[0] \; \& \; \sim final[3]) \; | \; (\sim final[3]) \; | \; ($ 

 $assign \ final\_output[3] = (((\sim final[0] \& \sim final[1] \& \sim final[2] \& \ final[3]) \mid (\sim final[0] \& \ final[1] \& \sim final[2] \& \ final[3]) \mid (\sim final[0] \& \ final[2] \& \ final[3]) \mid (\sim final[1] \& \ final[2] \& \ final[3]) \mid (\sim final[1] \& \ final[2] \& \ final[3]) \mid (\sim final[1] \& \ final[2] \& \ final[3]) \mid (\sim final[1] \& \ final[3]) \mid (\sim fi$ 

 $assign \ final\_output[2] = (((\sim final[0] \& \sim final[1] \& \sim final[2] \& \ final[3]) \mid (\sim final[0] \& \sim final[1] \& \ final[2] \& \ final[3]) \mid (\sim final[0] \& \ final[1] \& \sim final[2] \& \ final[3]) \mid (\sim final[0] \& \ final[1] \& \sim final[2] \& \ final[3]) \mid (\sim final[0] \& \ final[3]) \mid (\sim final[0] \& \ final[3]) \mid (\sim final[3]) \mid (\sim$ 

 $assign \ final\_output[1] = (((\sim final[0] \& \sim final[1] \& \sim final[2] \& \ final[3]) \mid (\sim final[0] \& \sim final[1] \& \ final[2] \& \sim final[3]) \mid (\sim final[0] \& \ final[2] \& \ final[3]) \mid (\sim final[0] \& \ final[3]) \mid (\sim final[1] \& \ final[3]) \mid (\sim final[3]) \mid ($ 

 $\begin{array}{l} assign \; final\_output[0] = (((\sim final[0] \; \& \; \sim final[1] \; \& \; \sim final[2]) \; | \; (\sim final[0] \; \& \; final[1] \; \& \; \sim final[2] \; \& \; \sim$ 

endmodule

```
\begin{split} & \text{module FourBitAdder(input } [0:3] \text{ X0, X1, input cin, output } [0:3] \text{ r, output count, input s);} \\ & \text{wire w1, w2, w3, w4, w5, w6, w7;} \\ & \text{xor(w7, X1[3], s);} \\ & \text{xor(w6, X1[2], s);} \\ & \text{xor(w5, X1[1], s);} \\ & \text{xor(w4, X1[0], s);} \\ & \text{FA f1(X0[3], w7, s, r[3], w1);} \\ & \text{FA f2(X0[2], w6, w1, r[2], w2);} \\ & \text{FA f3(X0[1], w5, w2, r[1], w3);} \\ & \text{FA f4(X0[0], w4, w3, r[0], count);} \\ & \text{endmodule} \\ \\ & \text{module FA(input X0, X1, cin, output r, count);} \\ & \text{assign } r = \text{X0} \land \text{X1} \land \text{cin;} \\ & \text{assign count} = (\text{X0} \land \text{X1}) \& \text{cin} \mid \text{X0 \& X1;} \\ \\ & \text{endmodule} \\ \\ \end{split}
```