Lab 5 report

Lab5.v module

The main module, lab5, serves as the control hub. It comprises several components, including clock dividers, counter instances, and logic to select and display counter outputs. The clock signal used for counting can be either slow or fast based on the value of SW9. It operates as intended, allowing users to select and observe the behavior of various counters via LEDR outputs.

Question: Are the synthesized circuits as you expected? Yes, when examining the synthesized circuits using the RTL viewer, we checked that the synthesized hardware corresponds to your intended functionality, appropriate clock domains, proper timing and hierarchy.

SlowClock.v module

The SlowClockDivider module serves as a clock frequency divider, producing a slower clock output from the input clock signal.It uses a 32-bit counter (count) to divide the input clock. It divides the frequency by a predetermined value (D) and generates a toggling output signal.

clk_out toggles its state each time the counter reaches (D-1), creating a slower clock signal with a period based on the input clock frequency division.

FastClock.v module

The FastClockDivider module functions as a clock frequency divider, producing a faster clock output from the input clock signal. It divides the frequency by a specified value (D) and generates a toggling output signal. The count increments on every rising edge of the input clock.

The expected relationships between counter outputs based on their operation in different clock domains (fast and slow) are primarily determined by the clock frequencies applied to each counter. Over longer observation periods, the disparities in count rates due to the differing clock speeds will become more pronounced, confirming the expected relationships between the counter outputs.