Verification of AXI RAM on VexRiscv

Write Scenario: -

Writing to the RAM works in both burst and individual writes at the indicated addresses so long as the addresses are word aligned.

Read Scenario: -

BURST

Read happens in burst mode AXI, by specification, does not support FIFO in burst reads so we get the data but if addresses are random, the read data can be random too instead of sequential as in the case for writes. To avoid data loss, make sure the burst length exactly matches the size of the required data transfer.

Individual Reads (Undesired behavior in some cases)

When reading from a memory address individually, data is read the first time but fails to read data from the same address if read a second time or more times. Individual data reads only happen once and data is not read again from an address that has already been read from even if a write happens to change the data on that address. The VexRiscv CPU fails to issue the address valid signal to the AXI interconnect and hence it never reads the same address again.

The writes can happen in the addresses spaced by one word, but individual reads from consecutive memory addresses is uncontrolled in the sense that it tries to read two words in a single transaction but if there is no data in that second consecutive address, the system will simply refuse to read any data and move on to the next instruction.

This is the block diagram for the complete system under consideration: -