FUJITSU

CMOS Gate Array

GENERAL INFORMATION

The Fujitsu CMOS gate array family consists of twenty-eight device types which are fabricated with advanced silicon gate CMOS technology. And more than 14 devices are coming. Fujitsu CMOS gate array are configured in a matrix of Basic Cells arranged in columns positioned side by side and Input/Output Cells on the device periphery. One Basic Cell is equivalent to a 2-input gate. The custom logic function is realized by interconnecting Unit Cells with double-layer metalization or triple-layer for largest arrays.

The Fujitsu CMOS gate array family contains four technology options: "H", "VH", "AV", and "UH".

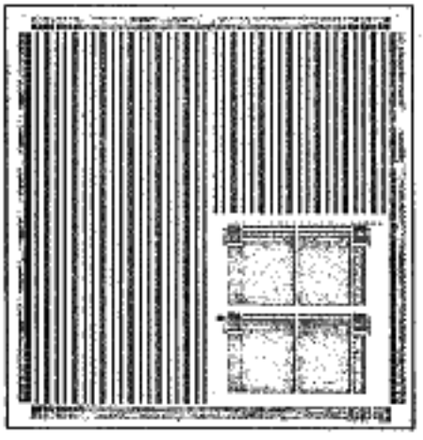
The "H" is high performance and provides STTL speed. Two versions using this technology are prepared: "H" and "HB". The complexity of "H" ranges from 440 gates up to 3900. The "HB" version can provide high output drive capability because of its special output buffer design. The complexity ranges from 440 to 1440 gates.

The "VH" is very high performance and provides ECL speed with CMOS power consumption. There are three options from 2640 to 8000 gate sizes.

The "AV" is the advanced "VH" technology. And there are three versions making use of this technology: "AV", "AVM", and "AVB". The "AV" version consists of 5 devices with their complexity of 2640 to 8000 gates. The "AVM" version is a gate array with a memory block on a chip. The device size ranges from 1584 to 4087 gates with 1K or 2K RAM, or 2K or 4K ROM. Just as "HB", the "AVB" version can supply high drive capability. The device size has variety of 357 gates to 2052 gates.

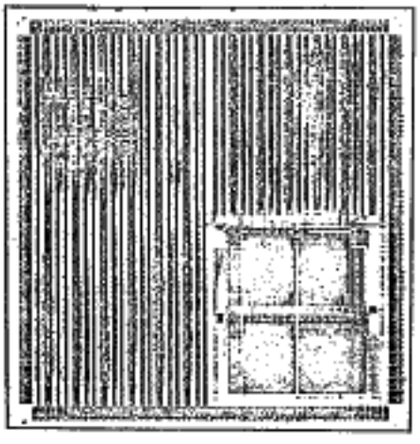
The "UH" technology can provide ultra high speed by its fine gate length. There are also two versions for "UH": "UH" and "UM". The complexity of "UH" is 20160. The lower density "UH" devices are now under development. The "UM", just as "AVM", integrates gate array and memory on one chip. The complexity of "UM" array is 10080 gates or 15120 gates with 12K or 6K-bit RAM, respectively.

To assure quick, simple and error-free implementation of the metal interconnection routing, Fujitsu utilizes a unique Computer Aided Design (CAD) system which fully automates LSI design. The CAD system performs a complete logic simulation, incorporating AC parameters based on the mask design, prior to the device fabrication. Because of this design process, error-free LSI can be developed quickly.



C-15006UM Die, Before Metalization

C-2000AVB Die, Before Metalization

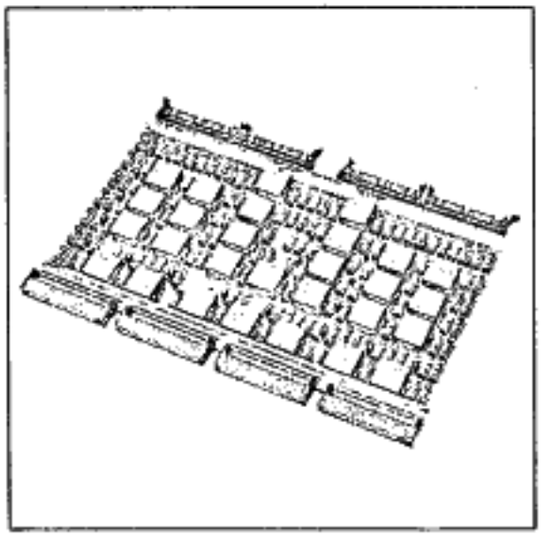


C-15006UM Die, After Metalization

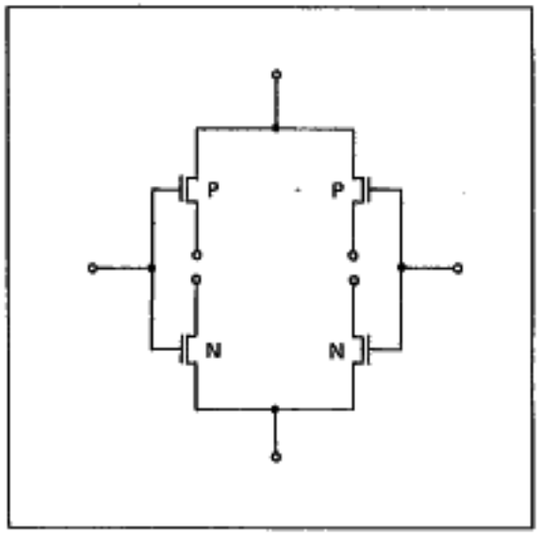
C-2000 AVB Die, After Metalization

FEATURES

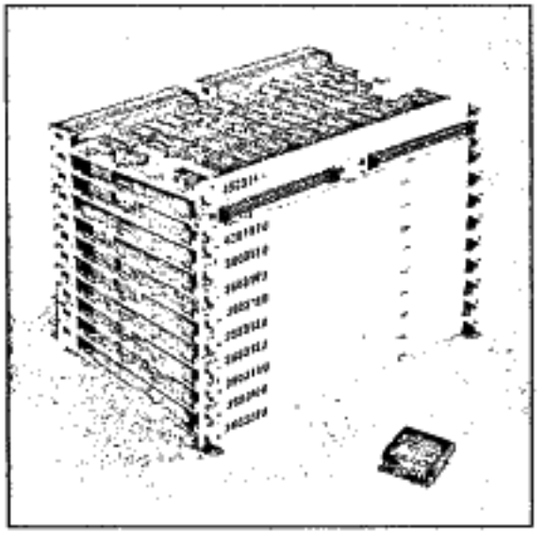
- 28 array types and more array types to come
- High-speed Silicon Gate CMOS process
- Double-layer metalization, or Triple-layer metalization for C-20000UH, C-15006UM, and C-10012UM
- Variety of software macros called "F-MACRO", equivalent to MSI Functions
- TTL compatible Input/Output, CMOS Input and Schmitt-Trigger Input
- High drive capability Output Buffer for "HB", "AVB", "UH", and "UM"
- Input pull-up/pull-down options for "HB" and "AVB"
- Predesigned Memory Macros for "AVM" and "UM"
- +5V single power supply
- Fast turn-around on design
- Simplified customer interface (only logic design and test pattern information required)
- Fully supported by Fujitsu CAD system (logic validation, physical layout, metal interconnection and test program)
- Design Support on major CAE workstations
- Wide variety of packaging options
- C-440H, C-700H, C-1275H, C-2000H, C-3900H, C-2600VH, C-3900VH, and C-8000VH are alternate sourced by Texas Instruments Incorporated, USA.



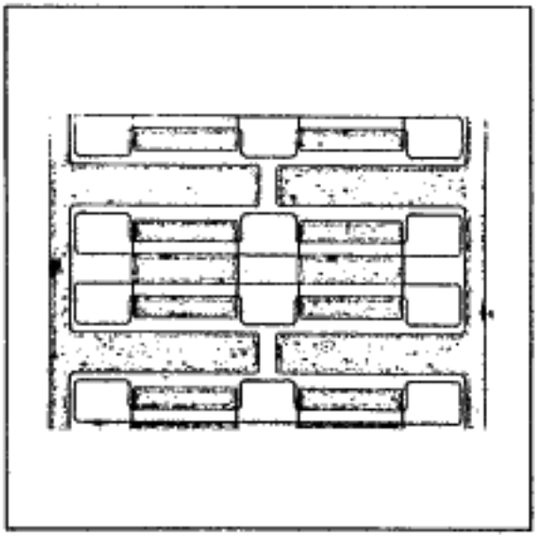
High Density PC Board with Fujitsu Gate Arrays



Basic Cell Equivalent Circuit



Fujitsu Gate Array, Replacing a Lot of MSI/SSI



Basic Cell Topology

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DEVICE DESCRIPTION

Tech-nology	Device Name	Part Number	Complexity[1]	Cell[2] Propagation Delay	Max. Number of Signal Pins	I/O Options	Supply[3] Voltage	Operating[4] Temp. Range
H	C-440H	MB 64Hxxx	440 gates	4 ns	54	Input: Normal Buffer Clock Driver Schmitt-Trigger CMOS Input Input pull-up/ pull-down available for "HB" Output: Normal Buffer 3-state Bidirectional Driver Output available for "HB"	5V±5%	0 to 70°C
	C-770H	MB 62Hxxx	900 gates	4 ns	74			
	C-1275H	MB 63Hxxx	1440 gates	4 ns	80			
	C-2000H	MB 60Hxxx	2000 gates	4 ns	68			
	C-3900H	MB 61Hxxx	3900 gates	4 ns	68			
	C-440HB	MB 64HBxxx	440 gates	4 ns	52			
	C-770HB	MB 62HBxxx	900 gates	4 ns	72			
	C-1275HB	MB 63HBxxx	1440 gates	4 ns	88			
VH	C-2600VH	MB 60VHxxx	2640 gates	2.2 ns	106			
	C-3900VH	MB 61VHxxx	3900 gates	2.2 ns	127			
	C-8000VH	MB 66VHxxx	8000 gates	2.2 ns	160			

1: 2-input gate equivalent.
2: F/O = 2, 2-input NAND gate.
3: 5V ± 10% or 4.5V ± 20% operation possible. For details, please contact Fujitsu.
4: Wider temperature operation possible. For details, please contact Fujitsu.

PACKAGE OPTIONS

Tech-nology	Device Name	Dual In-line Package										Flat Package				
		16	18	20	22	24	28	40	42	48	64	16	20	24	28	48
H	C-440H	♦■	♦■	♦■	♦■	♦■	♦■▮	♦■	■▮		▮	■	■	■	■	■
	C-770H				♦	♦■	♦■▮	♦■	♦■▮	♦■	▮			■	■	■
	C-1275H					♦■	♦■	♦■	♦■▮	♦■▮	▮					■
	C-2000H						♦	♦■	♦ ▮	♦■▮	▮					■
	C-3900H															
	C-440HB	♦■	♦■	♦■	♦■	♦■	♦■▮	♦■	♦■▮	▮	▮	■	■	■	■	■
	C-770HB					♦■	♦■▮	♦■	♦■▮	♦■▮	▮					■
	C-1275HB					♦■	♦■	♦■	♦■▮	♦■▮	▮					■
VH	C-2600VH					■	♦■	♦■	♦■▮	♦■▮	▮					■
	C-3900VH					■		♦■	♦■	♦ ▮	▮					■
	C-8000VH															

Power Dissipation at 10MHz	DC Characteristics					Turn-[6] around Time	Device Name	Technology
	Output High Voltage	Output Low Voltage	Input High[5] Voltage	Input Low[5] Voltage	Input Leakage Current			
50mW typ.	4.2V min. at I_{OH} = −0.4mA	0.4V max. at I_{OL} = 2.0mA	2.0V min.	0.8V max.	±10μA max. for Input Buffer and 3-state Output	5 weeks	C-440H	H
50mW typ.						5 weeks	C-770H	
50mW typ.						5 weeks	C-1275H	
50mW typ.						5 weeks	C-2000H	
100mW typ.						5 weeks	C-3900H	
50mW typ.		0.4V max. at I_{OL} = 2.0mA or 0.8V max. at I_{OL} = 10.0mA available for Driver Output				5 weeks	C-440HB	
50mW typ.						5 weeks	C-770HB	
50mW typ.						5 weeks	C-1275HB	
50mW typ.	4.2V min. at I_{OH} = −0.4mA	0.4V max. at I_{OL} = 3.2mA	2.2V min.	0.8V max.	±10μA max. for Input Buffer and 3-state Output	5 weeks	C-2600VH	VH
100mW typ.						5 weeks	C-3900VH	
150mW typ.						5 weeks	C-8000VH	

5: Values for Normal Buffer and Clock Driver.
6: From the customer's design approval to engineering sample shipment.

Flat Package				Leadless Chip Carrier			J-Leaded Chip Carrier				Pin Grid Array Package						Device Name
64	70	80	100	28	48	64	28	44	68	84	64	88	136	179	208	256	
■	■			♦	♦	♦	■	■			♦						C-440H
■		■		♦	♦	♦	■	■			♦	♦					C-770H
■	■	■			♦	♦	■	■	■		♦	♦					C-1275H
■		■			♦	♦		■	■		♦	♦					C-2000H
						♦					♦	♦					C-3900H
■				♦	♦	♦	■	■			♦						C-440HB
■		■			♦	♦	■	■	■		♦	♦					C-770HB
■		■	■		♦	♦	■	■	■	■	♦	♦					C-1275HB
■		■	■		♦	♦	■	■	■	■	♦	♦	♦				C-2600VH
■		■	■		♦	♦		■	■	■	♦	♦	♦				C-3900VH
						♦					♦	♦	♦	♦			C-8000VH

Note: ♦: Ceramic package
■: Plastic package
▮: Plastic (Shrink type DIP: Lead Spacing center to center: 0.07")
Plastic PGA packages and more than 100-pin plastic Flat packages are under development. Contact Fujitsu for availability.

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DEVICE DESCRIPTION

Tech-nology	Device Name	Part Number	Complexity[1]	Cell[2] Propagation Delay	Max.[3] Number of Signal Pins	I/O Options	Supply[4] Voltage	Operating[5] Temp. Range
AV	C-2600AV	MB 654xxx	2640 gates	1.4 ns	106	Input: Normal Buffer Clock Driver Schmitt-Trigger CMOS Input Input pull-up/ pull-down available for "AVB" Output: Normal Buffer 3-state Bidirectional Driver Output available for "AVB"	5V±5%	0 to 70°C
	C-3900AV	MB 653xxx	3900 gates	1.4 ns	127			
	C-5000AV	MB 652xxx	5022 gates	1.4 ns	127			
	C-6600AV	MB 651xxx	6664 gates	1.4 ns	160			
	C-8000AV	MB 650xxx	8000 gates	1.4 ns	160			
	C-350AVB	MB 675xxx	357 gates	1.4 ns	38 (42)			
	C-540AVB	MB 674xxx	549 gates	1.4 ns	48 (50)			
	C-850AVB	MB 673xxx	852 gates	1.4 ns	58 (60)			
	C-1200AVB	MB 672xxx	1245 gates	1.4 ns	68 (68)			
	C-1600AVB	MB 671xxx	1674 gates	1.4 ns	74 (76)			
	C-2000AVB	MB 670xxx	2052 gates	1.4 ns	88 (92)			

1: 2-input gate equivalent.
2: F/O = 2, 2-input NAND gate.
3: The values in parenthesis show the maximum number of signal pins when no high driving capability (I_{OL} = 10.0 mA) is used.
4: 5V ± 10% operation possible. For details, please contact Fujitsu.
5: Wider temperature operation possible. For details, please contact Fujitsu.

PACKAGE OPTIONS

Tech-nology	Device Name	Dual In-line Package										Flat Package				
		16	18	20	22	24	28	40	42	48	64	16	20	24	28	48
AV	C-2600AV					■	◆■	◆■	◆■▮	◆■▮	▮					■
	C-3900AV					■		◆■	◆■	◆ ▮	▮					■
	C-5000AV							■			▮					
	C-6600AV															
	C-8000AV															
	C-350AVB	◆■	◆■	◆■	◆■	◆■	◆■▮	◆■	■▮	▮		■	■	■	■	■
	C-540AVB	◆■	◆■	◆■	◆■	◆■	◆■▮	◆■	■▮	▮	▮	■	■	■	■	■
	C-850AVB			■	◆■	◆■	◆■▮	◆■	■▮	▮	▮			■	■	■
	C-1200AVB				◆■	◆■	◆■▮	◆■	◆■▮	◆■▮	▮			■	■	■
	C-1600AVB				◆■	◆■	◆■▮	◆■	◆■▮	◆■▮	▮					■
	C-2000AVB					■	◆■	◆■	◆■▮	◆■▮	▮					■

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CMOS Gate Array

DEVICE DESCRIPTION

Tech-nology	Device Name	Part Number	Complexity[1]	Cell[2] Propagation Delay	Max[3] Number of Signal Pins	I/O Options	Supply[4] Voltage	Operating[5] Temp. Range
AV	C-1502AVM	MB 662xxx	1564 gates with 2K RAM or 4K ROM	1.4 ns	114	Input: Normal Buffer Clock Driver Schmitt-Trigger CMOS Input Output: Normal Buffer 3-state Bidirectional	5V ± 5%	0 to 70°C
	C-2301AVM	MB 661xxx	2375 gates with 1K RAM or 2K ROM	1.4 ns	124			
	C-4002AVM	MB 660xxx	4087 gates with 2K RAM or 4K ROM	1.4 ns	127			

1: 2-input gate equivalent.
2: F/O = 2, 2-input NAND gate, 26 ns RAM access time.
3: Including 7 RAM Test Pins or 5 ROM Test Pins.
4: 5V ± 10% operation possible. For details, please contact Fujitsu.
5: Wider temperature operation possible. For details, please contact Fujitsu.

PACKAGE OPTIONS

Tech-nology	Device Name	Dual In-line Package										Flat Package				
		16	18	20	22	24	28	40	42	48	64	16	20	24	28	48
AV	C-1502AVM					■	■	♦ ■	♦ ■ ▮	♦ ▮	▮					■
	C-2301AVM					■		♦ ■	♦ ■	♦ ▮	▮					■
	C-4002AVM															

DEVICE DESCRIPTION

Tech-nology	Device Name	Part Number	Complexity[1]	Cell[2] Propagation Delay	Max. Number of Signal Pins	I/O Options	Supply[3] Voltage	Operating[4] Temp. Range
UH	C-20000UH	MB 600xxx	20160 gates	1.0 ns	220	Input: Normal Buffer Clock Driver Output: Normal Buffer 3-state Bidirectional Driver Output	5V±5%	0 to 70°C
	C-15006UM	MB 610xxx	15120 gates with 6K RAM	1.0 ns 15 ns RAM access time	219			
	C-10012UM	MB 611xxx	10080 gates with 12K RAM	1.0 ns 15 ns RAM access time	219			

1: 2-input gate equivalent.
2: F/O = 2, 2-input NAND gate.
3: 5V ±10% operation possible. For details, please contact Fujitsu.
4: Wider temperature operation possible. For details, please contact Fujitsu.

PACKAGE OPTIONS

Tech-nology	Device Name	Dual In-line Package										Flat Package				
		16	18	20	22	24	28	40	42	48	64	16	20	24	28	48
UH	C-20000UH															
	C-15006UM															
	C-10012UM															

2600 D-05

Power Dissipation at 10MHz	DC Characteristics					Turn-[7] around Time	Device Name	Tech-nology
	Output High Voltage	Output Low Voltage	Input High[6] Voltage	Input Low[6] Voltage	Input Leakage Current			
100mW typ.	4.2V min at I_{OH} = −0.4mA	0.4V max. at I_{OL} = 3.2mA	2.2V min.	0.8V max.	±10μA max. for Input Buffer and 3-state Output	5 weeks	C-2600AV	AV
100mW typ.						5 weeks	C-3900AV	
100mW typ.						5 weeks	C-5000AV	
150mW typ.						5 weeks	C-6600AV	
150mW typ.						5 weeks	C-8000AV	
50mW typ.		0.4V max. at I_{OL} = 3.2mA or 0.5V max. at I_{OL} = 10.0mA available for Driver Output				5 weeks	C-350AVB	
50mW typ.						5 weeks	C-540AVB	
50mW typ.						5 weeks	C-850AVB	
50mW typ.						5 weeks	C-1200AVB	
100mW typ.						5 weeks	C-1600AVB	
100mW typ.						5 weeks	C-2000AVB	

6: Values for Normal Buffer and Clock Driver

7: From the customer's design approval to engineering sample shipment.

Flat Package				Leadless Chip Carrier			J-Leaded Chip Carrier				Pin Grid Array Package						Device Name
64	70	80	100	28	48	64	28	44	68	84	64	88	135	179	208	256	
■		■	■		♦	♦	■	■	■	■	♦	♦	♦				C-2600AV
■		■	■		♦	♦		■	■	■	♦	♦	♦				C-3900AV
		■	■		♦	♦			■	■	♦	♦	♦				C-5000AV
						♦					♦	♦	♦	♦			C-6600AV
						♦					♦	♦	♦	♦			C-8000AV
				♦	♦		■	■									C-350AVB
■				♦	♦	♦	■	■			♦						C-540AVB
■				♦	♦	♦	■	■			♦						C-850AVB
■		■		♦	♦	♦	■	■			♦						C-1200AVB
■		■		♦	♦	♦	■	■	■		♦	♦					C-1600AVB
■		■	■		♦	♦		■	■		♦	♦					C-2000AVB

Note: ♦: Ceramic package

■: Plastic package

▮: Plastic (Shrink type DIP: Lead Spacing center to center: 0.07")

Plastic PGA packages and more than 100-pin plastic Flat packages are under development. Contact Fujitsu for availability.

Power Dissipation at 10MHz	DC Characteristics					Turn-[7] around Time	Device Name	Tech-nology
	Output High Voltage	Output Low Voltage	Input High[6] Voltage	Input Low[6] Voltage	Input Leakage Current			
100mW typ.	4.2V min. at I_{OH} = −0.4mA	0.4V max. at I_{OL} = 3.2mA	2.2V min.	0.8V max.	±10μA max. for Input Buffer and 3-state Output	5 weeks	C-1502AVM	AV
100mW typ.						5 weeks	C-2301AVM	
150mW typ.						5 weeks	C-4002AVM	

6: Values for Normal Buffer and Clock Driver.
7: From the customer's design approval to engineering sample shipment.

Flat Package				Leadless Chip Carrier			J-Leaded Chip Carrier				Pin Grid Array Package						Device Name
64	70	80	100	28	48	64	28	44	68	84	64	88	135	179	208	256	
■		■	■		♦	♦		■	■	■	♦	♦	♦				C-1502AVM
■		■	■		♦	♦		■	■	■	♦	♦	♦				C-2301AVM
						♦					♦	♦	♦				C-4002AVM

Note: ♦: Ceramic package
■: Plastic package
▮: Plastic (Shrink type DIP: Lead Spacing center to center: 0.07")
Plastic PGA packages and more than 100-pin plastic Flat packages are under development. Contact Fujitsu for availability.

Power Dissipation at 10MHz	DC Characteristics					Turn-[6] around Time	Device Name	Tech-nology
	Output High Voltage	Output Low Voltag	Input High[5] Voltage	Input Low[5] Voltage	Input Leakage Current			
500mW typ.	4.0V min. at I_{OH} = −0.4mA	0.4V max. at I_{OL} = 3.2mA or 0.4V max. at I_{OL} = 6.4mA available for Driver Output	2.2V min.	0.8V max.	±10μA max. for Input Buffer or ±40μA max. for 3-state	10 weeks	C-20000UH	UH
500mW typ.						10 weeks	C-15006UM	
500mW typ.						10 weeks	C-10012UM	

5: Values for Normal Buffer and Clock Driver
6: From the customer's design approval to engineering sample shipment.

Flat Package				Leadless Chip Carrier			J-Leaded Chip Carrier				Pin Grid Array Package						Device Name
64	70	80	100	28	48	64	28	44	68	84	64	88	135	179	208	256	
													♦	♦	♦	♦	C-20000UH
													♦	♦	♦	♦	C-15006UM
													♦	♦	♦	♦	C-10012UM

Note
♦: Ceramic package
■: Plastic package
▮: Plastic (Shrink type DIP: Lead Spacing center to center: 0.07")
256-pin PGA: 50 mil and 100 mil pin center to center are available.

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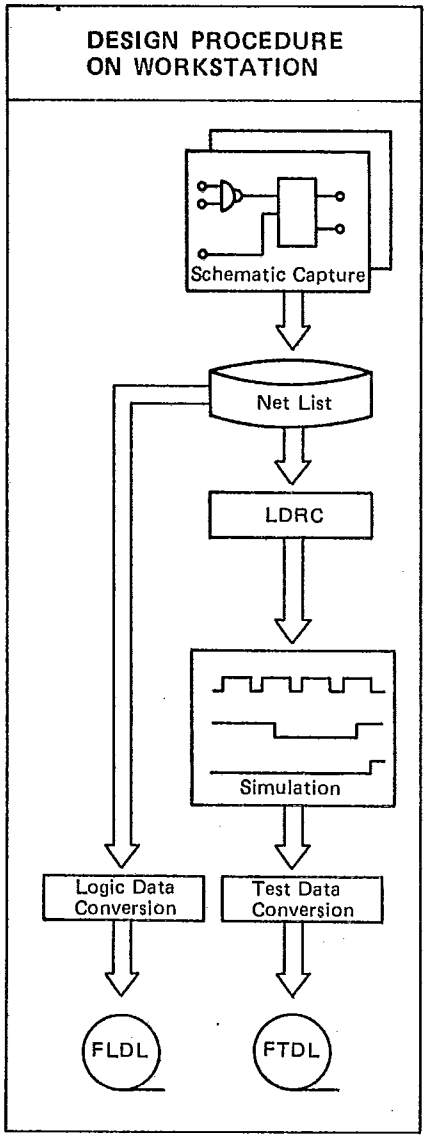
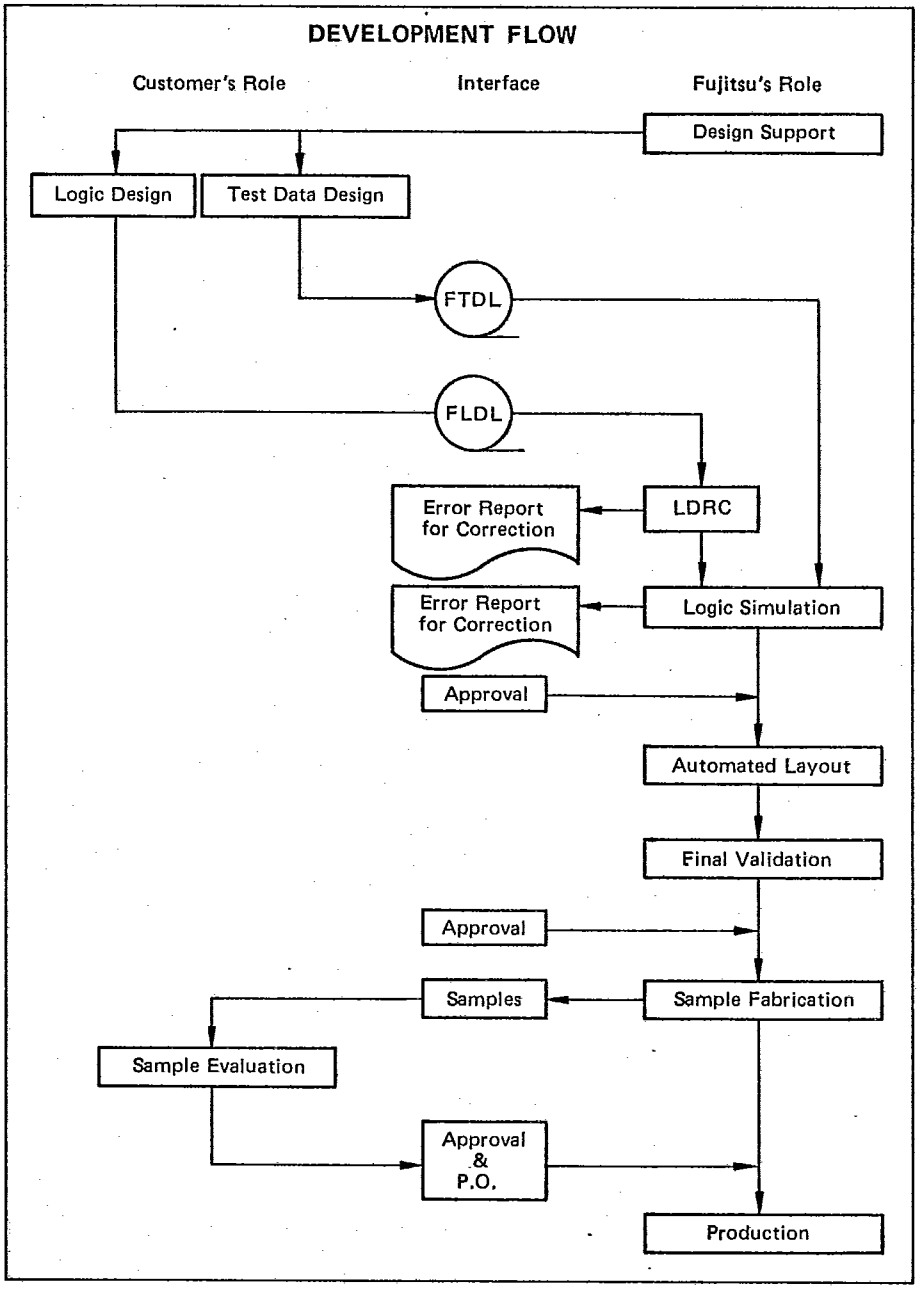
CMOS Gate Array

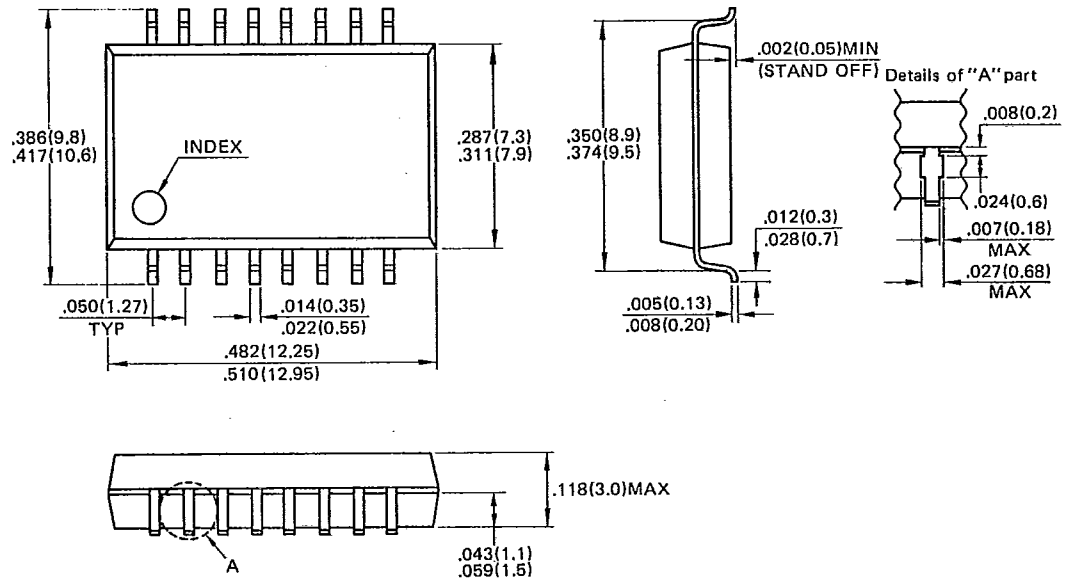
CUSTOMER/FUJITSU INTERFACE





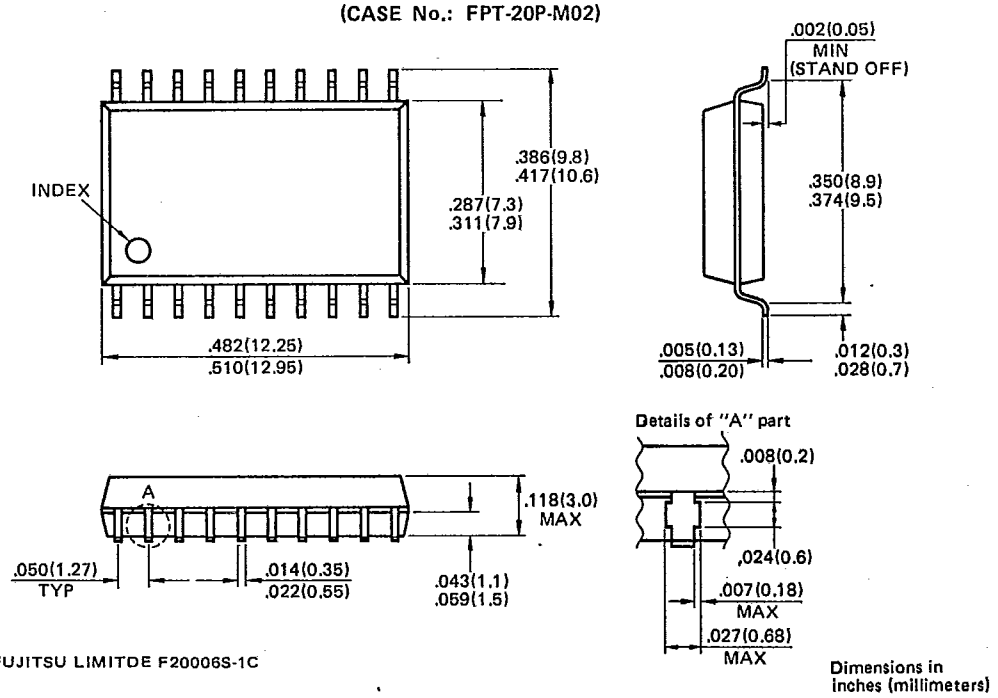
NEW PACKAGE FOR GATE ARRAY

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M03)



Dimensions in
inches (millimeters)

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M02)



Dimensions in
inches (millimeters)

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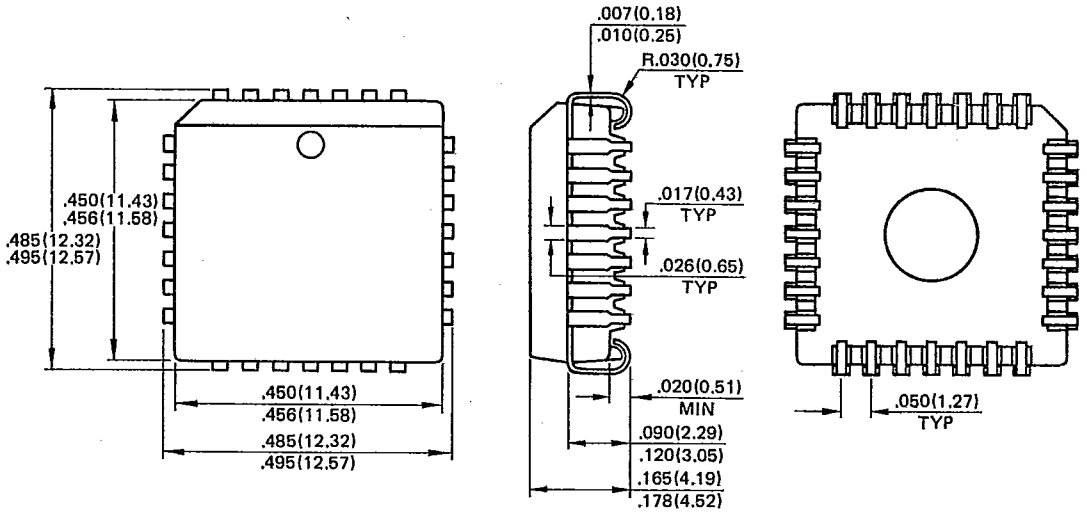
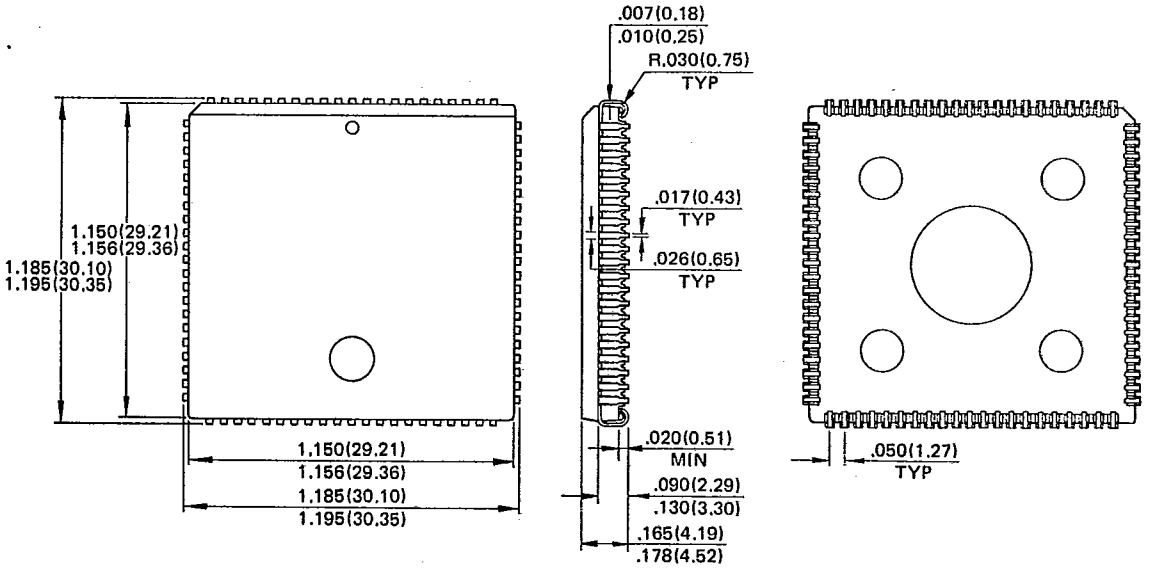
NEW PACKAGE FOR GATE ARRAY (Cont'd)

28-LEAD PLASTIC CHIP CARRIER
(CASE NO.: LCC-28P-M01)



Dimensions in
inches (millimeters)

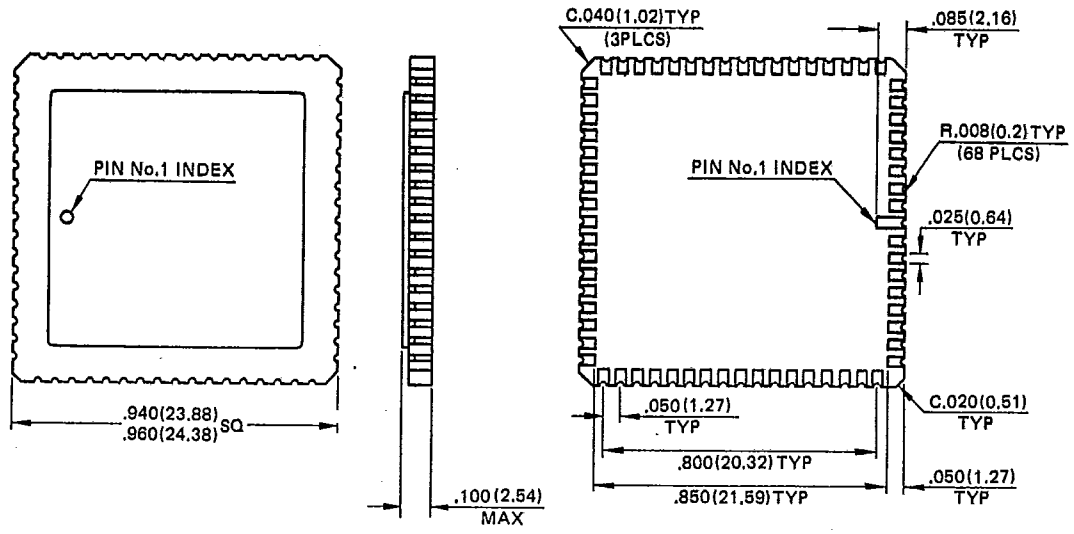
84-LEAD PLASTIC CHIP CARRIER
(CASE NO.: LCC-84P-M01)



Dimensions in
inchies (millimeters)

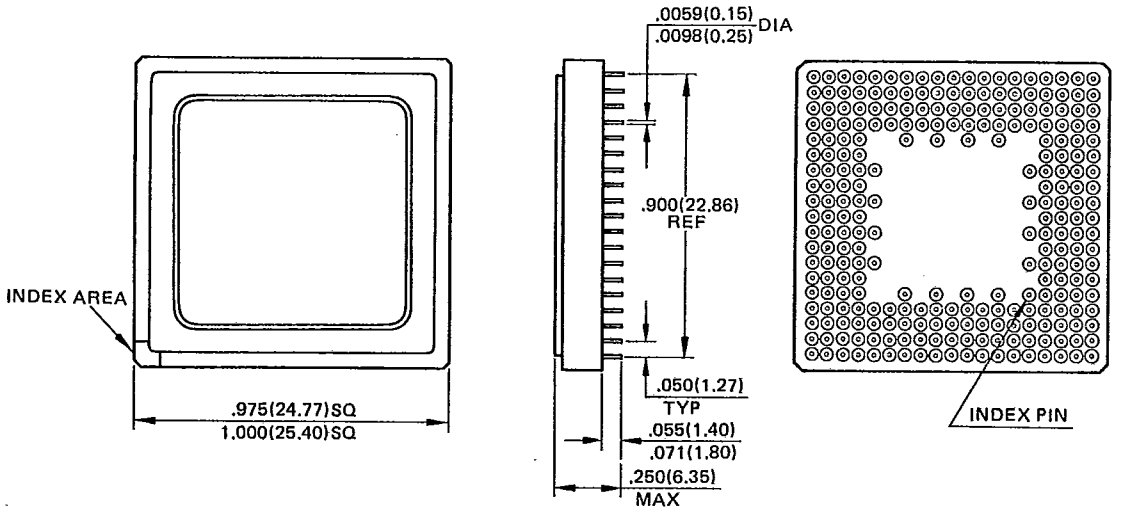
NEW PACKAGE FOR GATE ARRAY (Cont'd)

68-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-68C-A02)



Dimensions in
inches (millimeters)

256-LEAD CERAMIC (METAL SEAL) PIN GRID ARRAY PACKAGE
(CASE No.: PGA-256C-A01)



Dimension in
inches (millimeters)

FUJITSU CMOS Gate Array

LOGIC CELL FAMILY

(1) Inverter, Clock Buffer Family

Name	Function	Number of Basic Cells					
		UH/UM	AV/AVM	AVB	VH	H	HB
V1N	Inverter	1	1	1	1	1	1
V2B	Power Inverter	1	1	1	1	1	1
V1L	Double Power Inverter	2	–	–	–	–	–
B1N	True Buffer	1	–	–	–	–	–
B1B	True Power Buffer	2*	–	–	–	–	–
B1L	Double Power Buffer	3*	–	–	–	–	–
B1H	Quadruple Power Buffer	5*	–	–	–	–	–
K1B	Clock Buffer	2	2	2	2	2	2
K2B	Power Clock Buffer	3	3	3	3	3	3
K3B	Gated Clock (AND) Buffer	2	3	3	3	3	3
K4B	Gated Clock (OR) Buffer	2	3	3	3	–	–
K5B	Gated Clock (NAND) Buffer	3	–	–	–	–	–
K6B	Gated Clock Buffer (D24 + V2B)	3*	–	–	–	–	–
KAB	Block Clock (OR) Buffer	3	–	–	–	–	–
KBB	Block Clock (OR x 10) Buffer	30	–	–	–	–	–
KCB	Block Clock Buffer (Non-inverting)	–	11	11	11	–	–

(2) NAND/AND Family

Name	Function	Number of Basic Cells					
		UH/UM	AV/AVM	AVB	VH	H	HB
N2N	2-input NAND	1	1	1	1	1	1
N2P	Power 2-input AND	2	2	2	2	–	–
N2B	Power 2-input NAND	3	3	3	3	–	–
N2K	Power 2-input NAND	2	–	–	–	–	–
N3N	3-input NAND	2	2	2	2	2	2
N3P	Power 3-input AND	3	3	3	3	–	–
N3B	Power 3-input NAND	3	3	3	3	–	–
N4N	4-input NAND	2	2	2	2	2	2
N4P	Power 4-input AND	3	3	3	3	–	–
N4B	Power 4-input NAND	4	4	4	4	–	–
N6B	Power 6-input NAND	5	5	5	5	5	5
N8P	Power 8-input AND	6	–	–	–	–	–
N8B	Power 8-input NAND	6	6	6	6	6	6
N9B	Power 9-input NAND	8	7	7	7	7	7
NCB	Power 12-input NAND	10	9	9	9	9	9
NGB	Power 16-input NAND	12	11	11	11	11	11

FUJITSU

CMOS Gate Array

(6) OR-AND-Inverter Family

Name	Function	Number of Basic Cells					
		UH/UM	AV/AVM	AVB	VH	H	HB
G23	2-wide 2-OR 3-input OAI	2	2	2	2	2	2
G14	2-wide 3-OR 4-input OAI	2	2	2	2	2	2
G24	2-wide 2-OR 4-input OAI	2	2	2	2	2	2
G34	3-wide 2-OR 4-input OAI	2	2	2	2	2	2
G44	2-wide 2-AND 2-OR 4-input OAI	–	2	2	2	2	2

(7) Multiplexer Family

Name	Function	Number of Basic Cells					
		UH/UM	AV/AVM	AVB	VH	H	HB
T24	Power 2-AND 4-wide Multiplexer	6	6	6	6	6	6
T26	Power 2-AND 6-wide Multiplexer	10	9	9	9	9	9
T28	Power 2-AND 8-wide Multiplexer	12	11	11	11	11	11
T32	Power 3-AND 2-wide Multiplexer	5	5	5	5	5	5
T33	Power 3-AND 3-wide Multiplexer	8	7	7	7	7	7
T34	Power 3-AND 4-wide Multiplexer	10	9	9	9	9	9
T42	Power 4-AND 2-wide Multiplexer	6	6	6	6	6	6
T43	Power 4-AND 3-wide Multiplexer	10	9	9	9	9	9
T44	Power 4-AND 4-wide Multiplexer	12	11	11	11	11	11
T54	Power 4-2-3-2 AND 4-wide Multiplexer	10	–	–	–	–	–
U24	Power 2-OR 4-wide Multiplexer	–	6	6	6	6	6
U26	Power 2-OR 6-wide Multiplexer	–	9	9	9	9	9
U28	Power 2-OR 8-wide Multiplexer	–	11	11	11	11	11
U32	Power 3-OR 2-wide Multiplexer	–	5	5	5	5	5
U33	Power 3-OR 3-wide Multiplexer	–	7	7	7	7	7
U34	Power 3-OR 4-wide Multiplexer	–	9	9	9	9	9
U42	Power 4-OR 2-wide Multiplexer	–	6	6	6	6	6
U43	Power 4-OR 3-wide Multiplexer	–	9	9	9	9	9
U44	Power 4-OR 4-wide Multiplexer	–	11	11	11	11	11

(8) Transmission Gate Data Selector Family

Name	Function	Number of Basic Cells					
		UH/UM	AV/AVM	AVB	VH	H	HB
T2B	2:1 Selector	–	2	2	2	2	2
T2C	Dual 2:1 Selector	–	4	4	4	4	4
T2D	2:1 Selector	–	2	2	2	2	2
V3A	1:2 Selector	–	2	2	2	–	–
V3B	Dual 1:2 Selector	–	3	3	3	–	–
T5A	4:1 Selector	–	5	5	5	5	5

(3) NOR/OR Family

Name	Function	Number of Basic Cells					
		UH/UM	AV/AVM	AVB	VH	H	HB
R2N	2-input NOR	1	1	1	1	1	1
R2P	Power 2-input OR	2	2	2	2	–	–
R2B	Power 2-input NOR	3	3	3	3	–	–
R2K	Power 2-input NOR	2	–	–	–	–	–
R2W	Double Power 2-input OR	3*	–	–	–	–	–
R3N	3-input NOR	2	2	2	2	2	2
R3P	Power 3-input OR	3	3	3	3	–	–
R3B	Power 3-input NOR	3	3	3	3	–	–
R4N	4-input NOR	2	2	2	2	2	2
R4P	Power 4-input OR	3	3	3	3	–	–
R4B	Power 4-input NOR	4	4	4	4	–	–
R6B	Power 6-input NOR	5	5	5	5	5	5
R8P	Power 8-input OR	6	–	–	–	–	–
R8B	Power 8-input NOR	6	6	6	6	6	6
R9B	Power 9-input NOR	8	7	7	7	7	7
RCB	Power 12-input NOR	10	9	9	9	9	9
RGB	Power 16-input NOR	12	11	11	11	11	11

(4) ENOR/EOR Family

Name	Function	Number of Basic Cells					
		UH/UM	AV/AVM	AVB	VH	H	HB
X1N	Exclusive NOR	3	–	–	–	–	–
X1B	Power Exclusive NOR	4	4	4	4	4	4
X2N	Exclusive OR	3	–	–	–	–	–
X2B	Power Exclusive OR	4	4	4	4	4	4
X3N	3-input Exclusive NOR	5	–	–	–	–	–
X3B	Power 3-input Exclusive NOR	6	–	–	–	–	–
X4N	3-input Exclusive OR	5	–	–	–	–	–
X4B	Power 3-input Exclusive OR	6	–	–	–	–	–

(5) AND-OR-Inverter Family

Name	Function	Number of Basic Cells					
		UH/UM	AV/AVM	AVB	VH	H	HB
D23	2-wide 2-AND 3-input AOI	2	2	2	2	2	2
D14	2-wide 3-AND 4-input AOI	2	2	2	2	2	2
D24	2-wide 2-AND 4-input AOI	2	2	2	2	2	2
D34	3-wide 2-AND 4-input AOI	2	2	2	2	2	2
D36	3-wide 2-AND 6-input AOI	3	–	–	–	–	–
D44	2-wide 2-OR 2-AND 4-input AOI	–	2	2	2	2	2

Note: 1 C47 is not available for C-350AVB, C-540AVB, C-440H, C-770H, C-440HB, and C-770HB.
2 SM1 and SM2 must not be used together in one chip.
* under development
– not available

(9) Flip-Flop Family

Name	Function	Number of Basic Cells					
		UH/UM	AV/AVM	AVB	VH	H	HB
FD2	Power DFF	–	8	8	8	8	8
FD3	Power DFF with PRESET	–	9	9	9	9	9
FD4	Power DFF with CLEAR and PRESET	–	10	10	10	10	10
FD5	Power DFF with CLEAR	–	9	9	9	9	9
FD6	DFF	–	7	7	7	7	7
FD7	DFF with CLEAR	–	8	8	8	8	8
FD8	DFF and Latch	–	9	9	9	9	9
FDD	Positive edge clocked Power DFF with CLEAR and PRESET	–	11	11	11	11	11
FDE	Positive edge clocked Power DFF with CLEAR	–	10	10	10	10	10
FDG	Positive edge clocked DFF with CLEAR	–	9	9	9	9	9
FDM	DFF	–	6	6	6	6	6
FDN	DFF with SET	–	7	7	7	7	7
FDO	DFF with RESET	–	7	7	7	7	7
FDP	DFF with SET and RESET	–	8	8	8	8	8
FDQ	4-bit DFF	–	21	21	21	21	21
FDR	4-bit DFF with CLEAR	–	26	26	26	26	26
FDS	4-bit DFF	–	20	20	20	–	–
FJ4	Power JKFF with CLEAR	–	11	11	11	11	11
FJ5	Power JKFF with CLEAR and PRESET	–	12	12	12	12	12
FJD	Positive edge clocked Power JKFF with CLEAR	–	12	12	12	12	12
SDH	SCAN 2-input DFF with Clear and Clock-Inhibit	14	–	–	–	–	–
SDJ	SCAN 4-input DFF with Clear and Clock-Inhibit	16	–	–	–	–	–
SDK	SCAN 6-input DFF with Clear and Clock-Inhibit	16	–	–	–	–	–
SJH	SCAN J-K FF with Clear and Clock-Inhibit	16	–	–	–	–	–
SDD	SCAN 2-input DFF with Clear, Preset, and Clock-Inhibit	16	–	–	–	–	–
SDA	SCAN 1-input DFF with Clock-Inhibit	12	–	–	–	–	–
SDB	SCAN 1-input 4-bit DFF with Clock-Inhibit	42	–	–	–	–	–
SHA	SCAN 1-input 8-bit DFF with Clock-Inhibit	68	–	–	–	–	–
SHB	SCAN 1-input 8-bit DFF with Clock-Inhibit and Q Output	62	–	–	–	–	–
SHC	SCAN 1-input 8-bit DFF with Clock-Inhibit and XQ Output	62	–	–	–	–	–
SHJ	SCAN 8-bit DFF with Clock-Inhibit and 2-to-1 Data Multiplexer	78	–	–	–	–	–
SHK	SCAN 8-bit DFF with Clock-Inhibit and 3-to-1 Data Multiplexer	87	–	–	–	–	–
SD1	1-bit SCAN DFF with CLEAR	–	–	–	–	14	14

Note: 1 C47 is not available for C-350AVB, C-540AVB, C-440H, C-770H, C-440HB, and C-770HB.
2 SM1 and SM2 must not be used together in one chip.
* under development
– not available

(10) Latch Family

Name	Function	Number of Basic Cells					
		UH/UM	AV/AVM	AVB	VH	H	HB
LT1	S-R Latch with CLEAR	–	4	4	4	4	4
LT2	1-bit Data Latch	–	4	4	4	4	4
LT3	4-bit Data Latch	–	15	15	15	15	15
LT4	4-bit Data Latch	–	13	13	13	13	13
LTK	Data Latch	–	4	4	4	4	4
LTL	Data Latch with CLEAR	–	5	5	5	5	5
LTM	4-bit Data Latch with CLEAR	–	15	15	15	15	15

(11) Shift Register Family

Name	Function	Number of Basic Cells					
		UH/UM	AV/AVM	AVB	VH	H	HB
FS1	4-bit Serial-in Parallel-out Shift Register	–	18	18	18	18	18
FS2	4-bit Shift Register with Synchronous Load	–	30	30	30	30	30
FS3	4-bit Shift Register with Asynchronous Load	–	34	34	34	34	34
FS4	4-bit Serial-in Parallel-out Shift Register with SCAN, Clear	36*	–	–	–	–	–

(12) Counter Family

Name	Function	Number of Basic Cells					
		UH/UM	AV/AVM	AVB	VH	H	HB
C11	Flip-Flop for Counter	–	11	11	11	11	11
C41	4-bit Binary Asynchronous Counter	–	24	24	24	24	24
C42	4-bit Binary Synchronous Counter	–	32	32	32	32	32
C43	4-bit Binary Synchronous Up Counter	–	48	48	48	48	48
C45	4-bit Binary Synchronous Up Counter	–	48	48	48	48	48
C47	4-bit Binary Synchronous Up/Down Counter	–	68	68	68	68	68
SC7	4-bit Synchronous Binary Up Counter with Parallel Load	62	–	–	–	–	–
SC8	4-bit Synchronous Binary Down Counter with Parallel Load	66	–	–	–	–	–
SC1	1-bit Counter with SCAN and CLEAR	–	–	–	–	15	15

(13) Adder Family

Name	Function	Number of Basic Cells					
		UH/UM	AV/AVM	AVB	VH	H	HB
A1A	1-bit Half Adder	5	–	–	–	–	–
A1N	1-bit Full Adder	8	8	8	8	8	8
A2N	2-bit Full Adder	16	16	16	16	16	16
A4H	4-bit Full Adder	48	50	50	50	50	50
AC1	Carry Look Ahead for 4-bit Full Adder	*	–	–	–	–	–
AL1	4-bit ALU	94*	–	–	–	–	–

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(14) Others

Name	Function	Number of Basic Cells					
		UH/UM	AV/AVM	AVB	VH	H	HB
MC4	4-bit Magnitude Comparator	–	42	42	42	42	42
DE2	2:4 Decoder	–	5	5	5	5	5
DE3	3:8 Decoder	–	15	15	15	15	15
SM1 2	Schmitt-Trigger Input	–	8	8	8	8	8
SM2 2	Schmitt-Trigger Input	–	7	7	7	7	7
BD3	Buffer (Delay Cell)	–	5	5	5	–	–
BD4	Buffer (Delay Cell)	4	–	–	–	–	–
BD5	Buffer (Delay Cell)	–	9	9	9	–	–
BD6	Buffer (Delay Cell)	–	17	17	17	–	–
PE5	5-bit Even Parity Generator/Checker	12	–	–	–	–	–
PO5	5-bit Odd Parity Generator/Checker	12	–	–	–	–	–
PE8	8-bit Even Parity Generator/Checker	18	–	–	–	–	–
PO8	8-bit Odd Parity Generator/Checker	18	–	–	–	–	–
PE9	9-bit Even Parity Generator/Checker	22	–	–	–	–	–
PO9	9-bit Odd Parity Generator/Checker	22	–	–	–	–	–
P24	4 wide 2 to 1 Data Selector	12	–	–	–	–	–
DE4	2 to 4 Decoder with Enable	8	–	–	–	–	–
DE6	3 to 8 Decoder with Enable	30	–	–	–	–	–
T2E	Dual 2:1 Selector	4	–	–	–	–	–
T2F	Fourfold 2:1 Selector	7	–	–	–	–	–
T4E	Dual 4:1 Selector	8*	–	–	–	–	–
T4F	Fourfold 4:1 Selector	16*	–	–	–	–	–
T4A	4:1 Selector with Enable	6*	–	–	–	–	–
T4B	Fourfold 4:1 Selector with Enable	18*	–	–	–	–	–
T4C	Ninefold 4:1 Selector with Enable	40*	–	–	–	–	–
KD2	Load Gate Fan-in = 2	1	–	–	–	–	–
ST0	0 Stuck Gate	1	–	–	–	–	–
ST1	1 Stuck Gate	1	–	–	–	–	–
Z00	0 Clip	0	0	0	0	0	0
Z01	1 Clip	0	0	0	0	0	0
YN1	Special Cell (N2P & R2N)	3	–	–	–	–	–
YN2	Special Cell (N2N & R2P)	3	–	–	–	–	–
YN3	Special Cell (2-cascade NAND)	2	–	–	–	–	–
YN4	Special Cell (N2P, R2N, N2N, & R2P)	6	–	–	–	–	–
YL9	Special Cell (9-bit Latch)	30	–	–	–	–	–

Note: 1 C47 is not available for C-350AVB, C-540AVB, C-440H, C-770H, C-440HB, and C-770HB.
2 SM1 and SM2 must not be used together in one chip.
* under development
– not available

FUJITSU

CMOS Gate Array

(15) Memory Macros

For C-1502AVM & C-4002AVM

Name	Function
R610	64w x 36b Single Port static RAM
R711	128w x 18b Single Port Static RAM
R87	256w x 9b Single Port Static RAM

For C-2301AVM

Name	Function
R51	32w x 32b Single Port Static RAM
R61	64w x 16b Single Port Static RAM
R71	128w x 8b Single Port Static RAM
R83	256w x 4b Single Port Static RAM
YRn	256w x 8b ROM

For C-15006UM & C-10012UM

Name	Function
R64	64w x 24b Single Port RAM with Address SCAN
R65	64w x 18b Dual Port RAM with Address SCAN
R75	128w x 18b Dual Port RAM with Address SCAN
R76*	128w x 24b Dual Port RAM with Address SCAN
R77	128w x 18b Three Port RAM with Address SCAN

(16) I/O Cell Family

Name	Function	Number of Basic Cells					
		UH/UM	AV/AVM	AVB	VH	H	HB
O1B	Output Buffer (Inverter)	0	–	–	–	–	–
O1L	Power Output Buffer (Inverter)	0	–	–	–	–	–
O2B	Output Buffer (True)	0	0	0	0	0	0
O2L	Power Output Buffer (True)	0	–	0	–	–	0
O2T	3-input AND Tri-state Output Buffer	0	–	–	–	–	–
O2W	Power 3-input AND Tri-state Output Buffer	0	–	–	–	–	–
O3T	Tri-state Output Buffer (Inverter)	0	–	–	–	–	–
O3W	Power Tri-state Output Buffer (Inverter)	0	–	–	–	–	–
O4B	3-input AND Output Buffer	0	–	–	–	–	–
O4T	Tri-state Output Buffer (True)	–	0	0	0	0	0
O4W	Power Tri-state Output Buffer (True)	–	–	0	–	–	0
O4L	Power 3-input AND Output Buffer	0	–	–	–	–	–
O6T	Tri-state Output Buffer (True)	0	–	–	–	–	–
O6W	Power Tri-state Output Buffer (True)	0	–	–	–	–	–
H4T	Tri-state Output (True), Input (True) Buffer	0	–	–	–	–	–
H4W	Power Tri-state Output (True), Input (True) Buffer	0	–	–	–	–	–
H6T	Tri-state Output and Input Buffer (True)	–	0	0	0	0	0
H6TU	H6T with Input Pull-up	–	–	0	–	–	0
H6TD	H6T with Input Pull-down	–	–	0	–	–	0
H6W	Power Tri-state Output and Input Buffer (True)	–	–	0	–	–	0
H6WU	H6W with Input Pull-up	–	–	0	–	–	0
H6WD	H6W with Input Pull-down	–	–	0	–	–	0
H6C	Tri-state Output and CMOS Interface Input Buffer (True)	–	–	0	–	–	0
H6CU	H6C with Input Pull-up	–	–	0	–	–	0
H6CD	H6C with Input Pull-down	–	–	0	–	–	0
H6E	Power Tri-state Output and CMOS Interface Input Buffer (True)	–	–	0	–	–	0
H6EU	H6E with Input Pull-up	–	–	0	–	–	0
H6ED	H6E with Input Pull-down	–	–	0	–	–	0

(16) I/O Cell Family (Cont'd)

Name	Function	Number of Basic Cells					
		UH/UM	AV/AVM	AVB	VH	H	HB
I1B	Input Buffer (Inverter)	0	–	–	–	–	–
I2B	Input Buffer (True)	0	0	0	0	0	0
I2BU	I2B with Input Pull-up	–	–	0	–	–	0
I2BD	I2B with Input Pull-down	–	–	0	–	–	0
I2C	CMOS Interface Input Buffer (True & Inverter)	–	0	0	0	0	0
I2CU	I2C with Input Pull-up	–	–	0	–	–	0
I2CD	I2C with Input Pull-down	–	–	0	–	–	0
I5B	Input Buffer (Complementary Output)	0	–	–	–	–	–
IAB	Fixed-location IKB (Inverter)	0	–	–	–	–	–
IBB	Fixed-location ILB (True)	0	–	–	–	–	–
IKB	Clock Input Buffer (Inverter)	0	0	0	0	0	0
IKBU	IKB with Input Pull-up	–	–	0	–	–	0
IKBD	IKB with Input Pull-down	–	–	0	–	–	0
ILB	Clock Input Buffer (True)	0	0	0	0	0	0
ILBU	ILB with Input Pull-up	–	–	0	–	–	0
ILBD	ILB with Input Pull-down	–	–	0	–	–	0
IT1	Input Buffer for Schmitt-Trigger Input	–	0	0	0	0	0
IT1U	IT1 with Input Pull-up	–	–	0	–	–	0
IT1D	IT1 with Input Pull-down	–	–	0	–	–	0

(17) I/O Buffer Family for Testing RAM

Name	Function	Number of Basic Cells					
		UH/UM	AV/AVM	AVB	VH	H	HB
O2M	Output Buffer (True)	0*	–	–	–	–	–
O3M	Tri-state Output Buffer (Inverter)	0	–	–	–	–	–
O3N	Power Tri-state Output Buffer (Inverter)	0	–	–	–	–	–
O6M	Tri-state Output Buffer (True)	0	–	–	–	–	–
O6N	Power Tri-state Output Buffer (True)	0	–	–	–	–	–
H4M	Tri-state Output (True), Input (True) Buffer	0	–	–	–	–	–
H4N	Power Tri-state Output (True), Input (True) Buffer	0	–	–	–	–	–
I1M	Input Buffer (Inverter)	0	–	–	–	–	–
I2M	Input Buffer (True)	0	–	–	–	–	–
I3M	Input Buffer (Inverter)	0	–	–	–	–	–
I4M	Input Buffer (True)	0	–	–	–	–	–

Note: 1 C47 is not available for C-350AVB, C-540AVB, C-440H, C-770H, C-440HB, and C-770HB.
2 SM1 and SM2 must not be used together in one chip.
* under development
– not available

FUJITSU

CMOS Gate Array

F-MACRO FAMILY

F-MACRO Family

Name	Function Equivalent	No. of BCs
F00	74LS00	*
F02	74LS02	*
F04	74LS04	*
F08	74LS08	*
F10	74LS10	*
F11	74LS11	*
F20	74LS20	*
F21	74LS21	*
F25	7425	*
F27	74LS27	*
F30	74LS30	*
F32	74LS32	*
F42	74LS42	32
F43	7443A	32
F44	7444A	32
F51	74LS51	7
F54	74LS54	9
F55	74LS55	6
F56	74LS56	*
F57	74LS57	*
F64	74S64	9
F68	74LS68	89
F69	74LS69	79
F73	74LS73A	*
F74	74LS74A	*
F75	74LS75	32
F76	74LS76A	*
F77	74LS77	18
F78	74LS78A	*
F82	7482	16
F83	74LS83A	50
F85	74LS85	42
F86	74LS86	*
F87	74H87	*
F90	74LS90	41
F91	74LS91	43
F92	74LS92	64
F93	74LS93	33
F94	7494	47
F95	74LS95B	42
F96	74LS96	56

Name	Function Equivalent	No. of BCs
F97	7497	*
F98	54L98	36
F99	54L99	*
F100	74100	60
F101	74H101	*
F102	74H102	*
F103	74H103	*
F106	74H106	*
F107	74LS107	*
F108	74H108	*
F109	74LS109A	*
F112	74LS112A	*
F113	74LS113	*
F114	74LS114A	*
F116	74116	82
F120	74120	34
F135	74S135	*
F137	74LS137	48
F138	74LS138	28
F139	74LS139	26
F147	74LS147	49
F148	74LS148	53
F150	74150	112
F151	74LS151	54
F152	74LS152	29
F153	74LS153	24
F154	74154	96
F155	74LS155	29
F157	74LS157	23
F158	74LS158	23
F160	74LS160A	82
F161	74LS161A	48
F162	74LS162A	83
F163	74LS163A	48
F164	74LS164	70
F165	74LS165	73
F166	74LS166	80
F168	74S168	111
F169	74LS169B	74
F171	74LS171	*
F174	74LS174	46

Name	Function Equivalent	No. of BCs
F175	74LS175	32
F176	74176	76
F177	74177	72
F178	74178	63
F179	74179	71
F180	74180	33
F181	74LS181	*
F182	74182	49
F183	74LS183	36
F190	74LS190	106
F191 [1]	74LS191	73
F192	74LS192	92
F193	74LS193	82
F194	74LS194A	78
F195	74LS195A	51
F198	74198	132
F199	74199	98
F260	74S260	*
F261	74LS261	107
F273	74LS273	*
F278	74278	46
F279	74LS279	18
F280	74LS280	57
F283	74LS283	50
F290	74LS290	45
F293	74LS293	33
F298	74LS298	36
F352	74LS352	28
F375	74LS375	18
F377	74LS377	71
F378	74LS378	55
F379	74LS379	39
F381	74LS381	192
F382	74LS382	201
F386	74LS386	*
F390	74LS390	82
F393	74LS393	52
F396	74LS396	60
F398	74LS398	37
F399	74LS399	37

Note: * under development
[1] not available for C-350AVB, C-540AVB, C-440H, C-770H, C-440HB, and C-770HB.