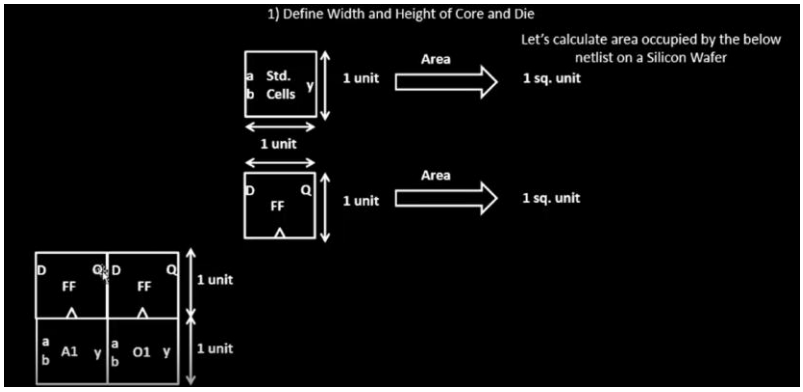
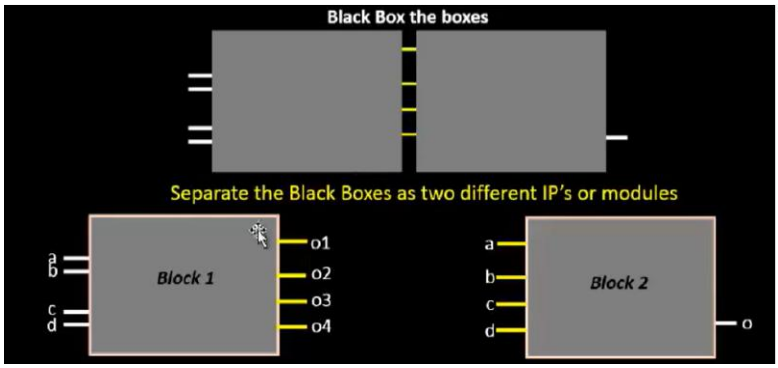
Day 2 - Sky130 Day 2 - Good floorplan vs bad floorplan and introduction to library cells [24 April – 7 May, 2024]

This series highlights the concept of floorplan and the placement of library cell. To understand the die utilization factor and aspect ratio, it is important to know about the width and length of the core and die. The following example shows standard cell and FF contains each 1 unit and its area is 1 sq.unit.



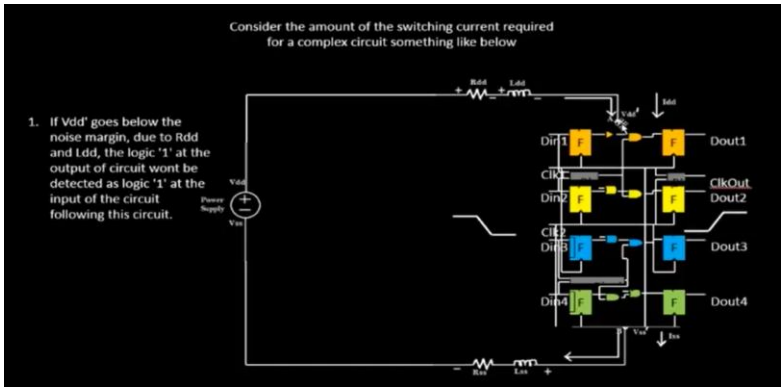
As per the above example,
Utilization factor = Area occupied by netlist / Total area of the core = 1
Aspect Ratio = Length / Width = 1

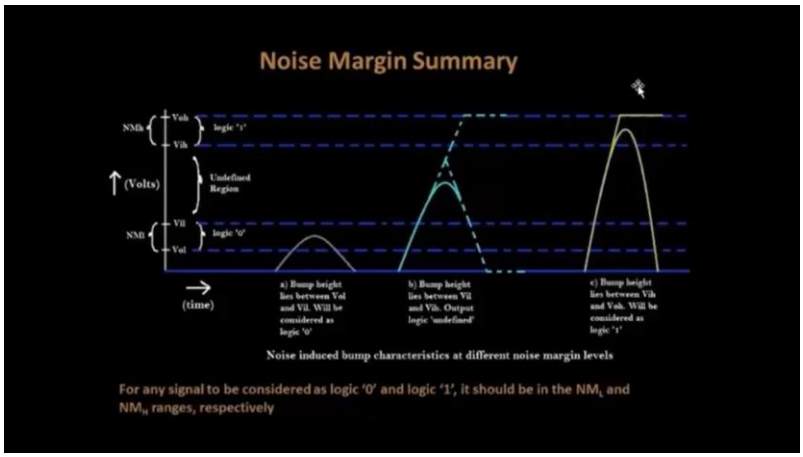
In preplaced Cells, overall combinational circuit will separated as per the gates into various blocks and also considered as black box.



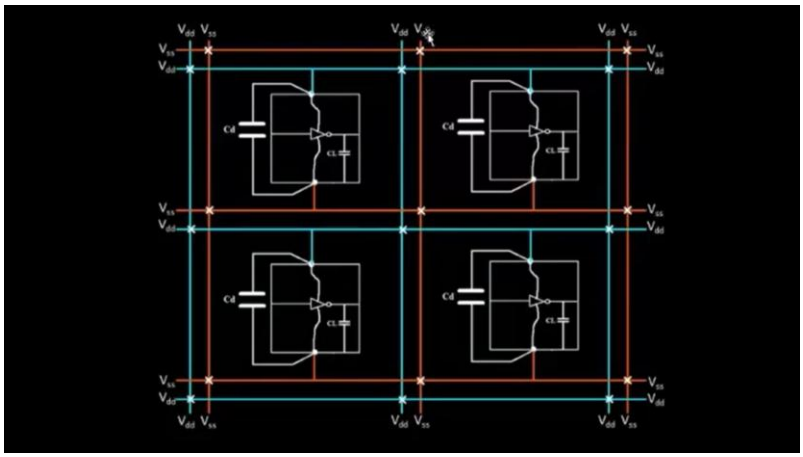
The next step is to focus on De-coupling capacitors, which was surround pre-placed cells. The main purpose of this de-coupling capacitor is used to isolate the design from unwanted noise and power variance from other designs.

Noise margin also plays a vital role in this flow. This is considered as the amount of tolerance of CMOS noise without compromising its normal operation. It is calculated by signal and noise values, and usually measured as decibels. The following image shows various bump characteristics at different noise margin levels.

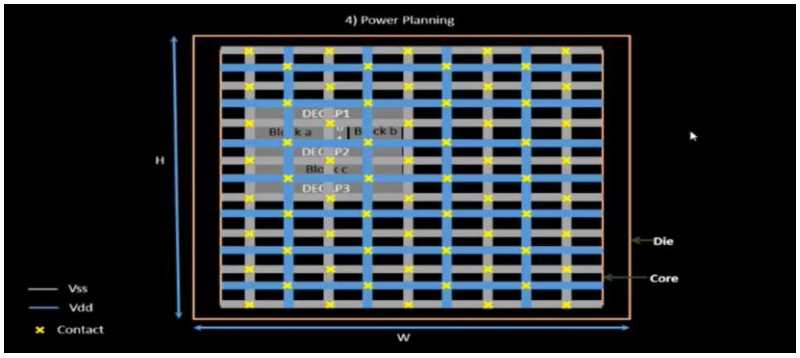




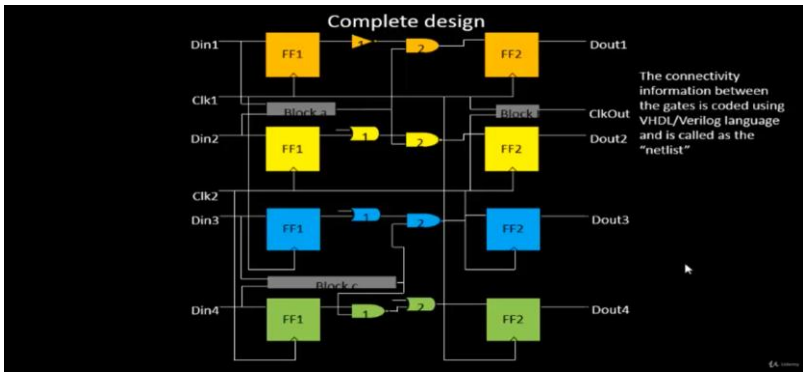
In the next process, power planning is considered for proper power lines to every IP cores and macro cells. It contains power and ground lines and connected with each and every core cell in terms of matrix type of arrangements.

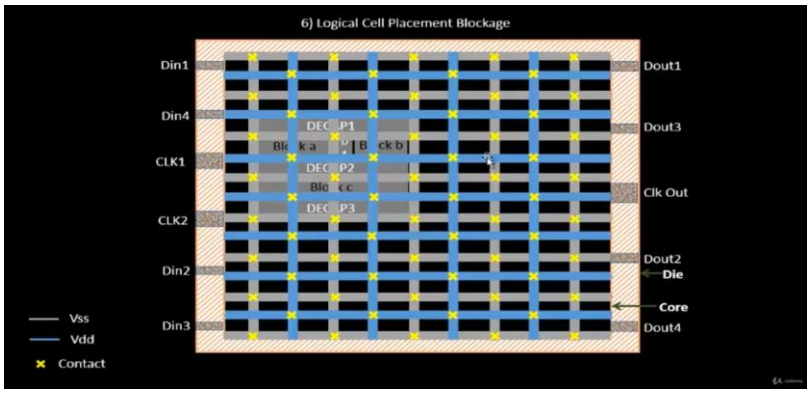


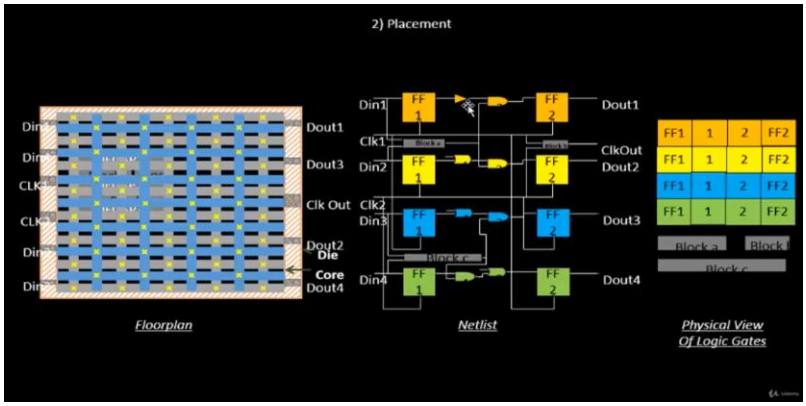
For example, if the path line contains 16-bit bus, then it uses an inverter for the purpose of logic 1 (capacitor charging to Vdd) and logic 0 (capacitor discharge to ground). This two functions contains Ground bounce and volt droop.



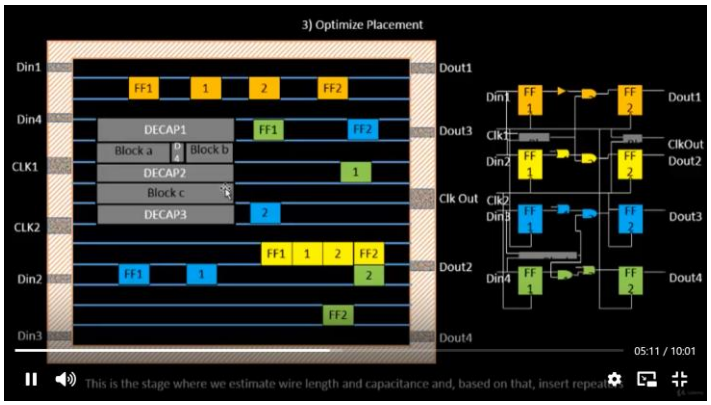
The placement of pin and logical cells follow after the power planning. The following example shows inputs, clock and output pins. They are Din1, Din2, Din3, Din4, Clk1, Clk2,Dout1, Dout2, Dout3, Dout4 and Clkout.



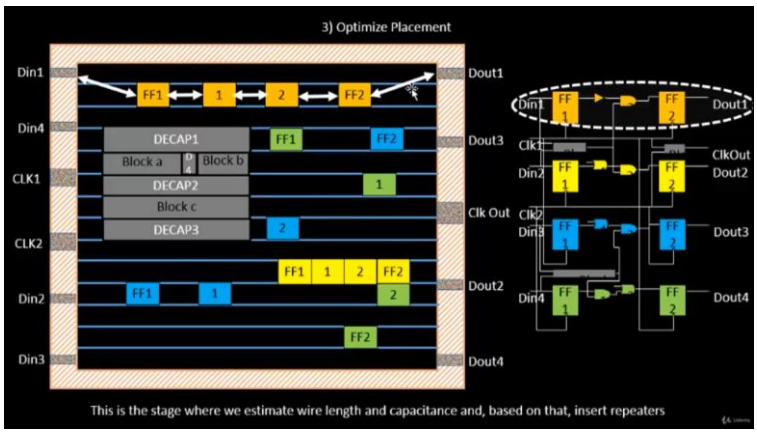




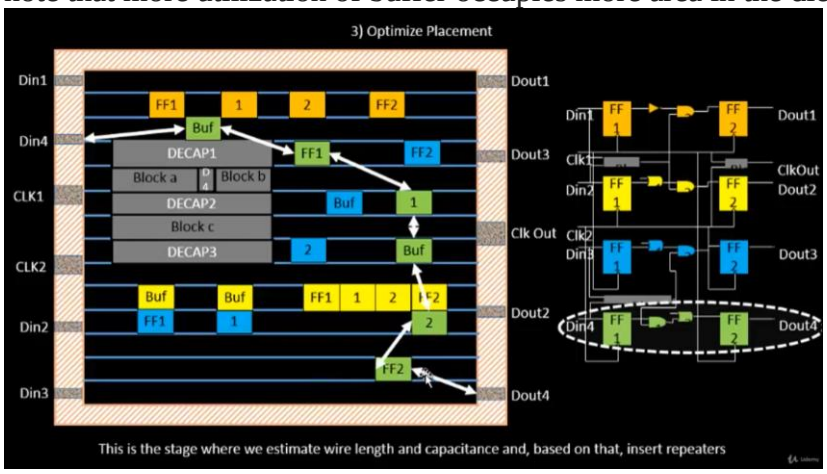
The next step helps to bind netlist with physical cells by removing the connect wires and making separate design of all the gates, and blocks. This process shows like a shelf and called as library design.



The above arrangement are randomly placed all the FF and gates. It is necessary to optimize the placement using estimated wire length and capacitance arrangements.

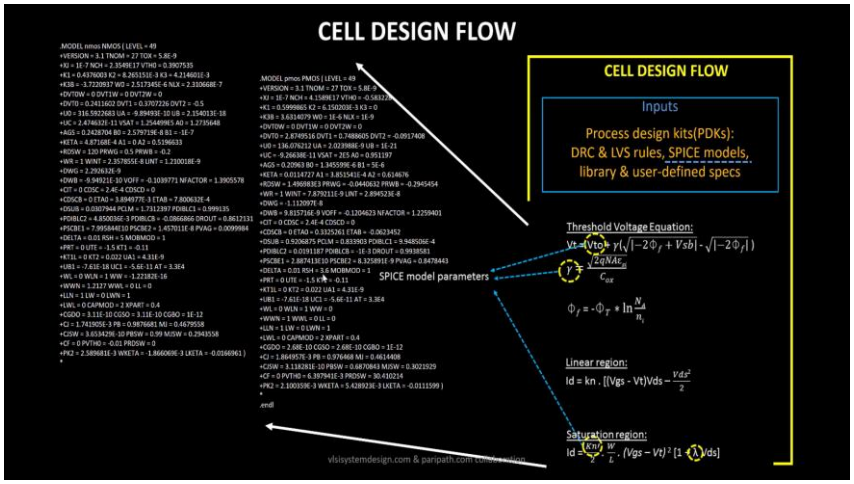


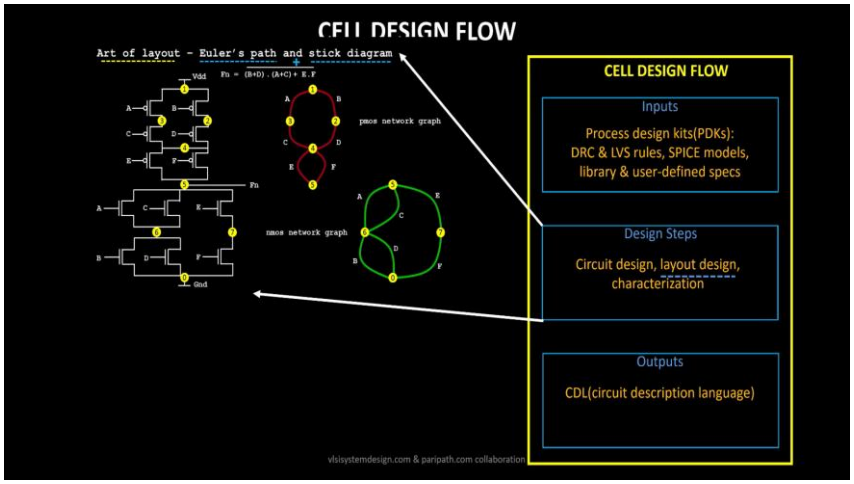
For better optimization placement, it is necessary to include some intermediate steps to maintain the integrity of the signal and also known as Repeaters (buffers). It is important ot note that more utilization of buffer occupies more area in the die.

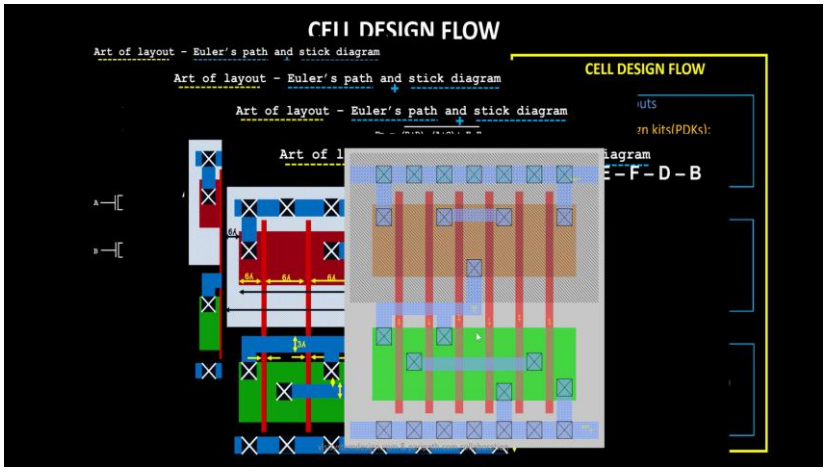


Library and its characterization is considered in terms of Logic synthesis, Floor plan, Placement, CTS and Routing. The overall characterization is focused on gates or cells.

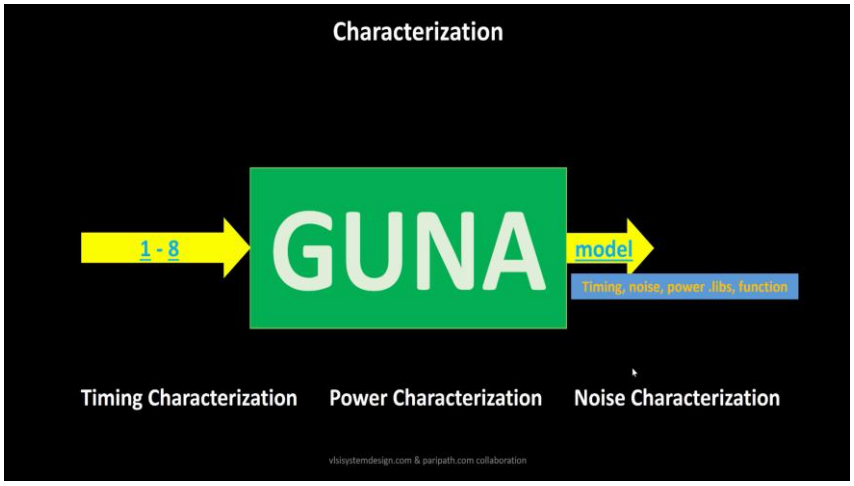
Inputs for cell design flow contains 3 main parts, named as input, design steps and outputs. In the input part, PDKs, DRC, SPICE models and libraries are considered. In the design steps part, circuit design, characterization and layout design are observed. In the output part, GDSII, LEF and extracted Spice netlist are received.



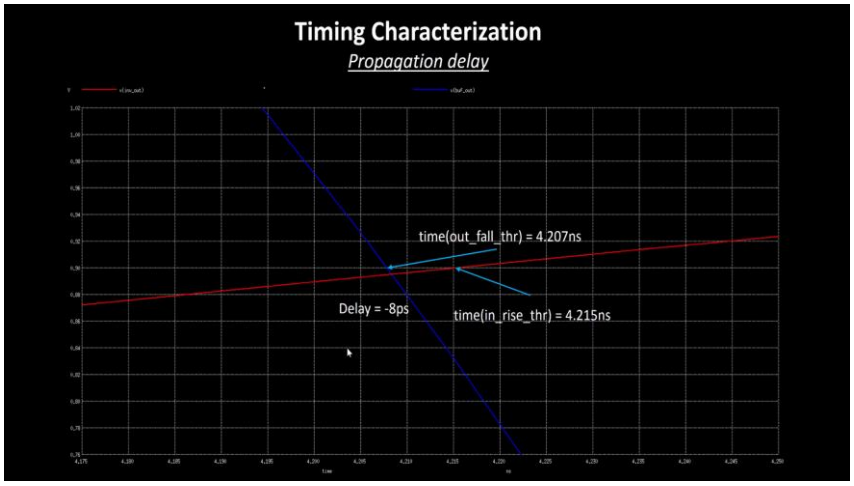


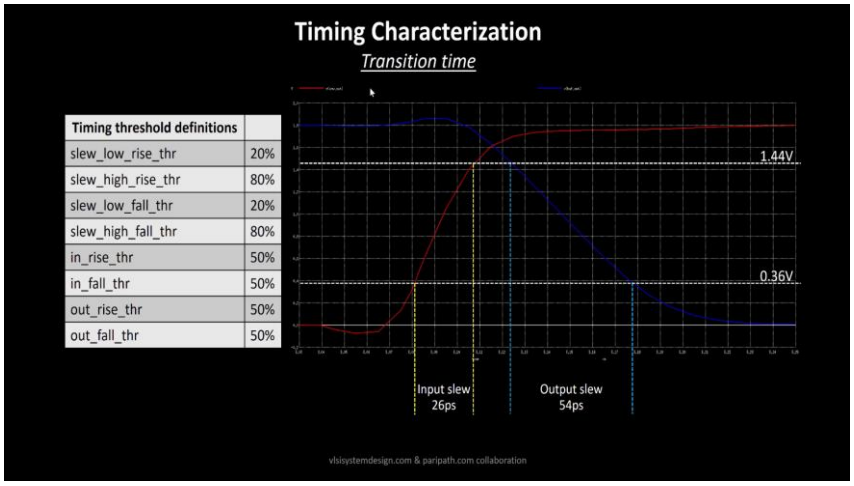


Typical characterization flow contains, model, extracted spice netlist, buffer, subcircuit, power supplies, stimulus and output capacitance. The final results where taken for transent simulation using .tran command. The overall characterization can be done using GUNA tool flow and possible to get timing, power and noise characterization.



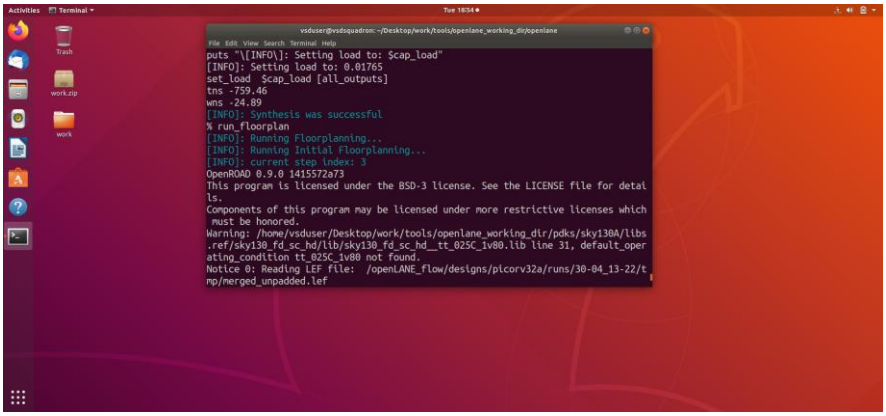
Timing threshold helps to identify Propagation delay and transition time.





The following commends are used to access OpenLANE environment.

- run_floorplan



According to floorplan def

$$1000\ Unit\ Distance = 1\ Micron$$

$$Die\ width\ in\ unit\ distance = 660685 - 0 = 660685$$

$$Die\ height\ in\ unit\ distance = 671405 - 0 = 671405$$

$$Distance\ in\ microns = \frac{Value\ in\ Unit\ Distance}{1000}$$

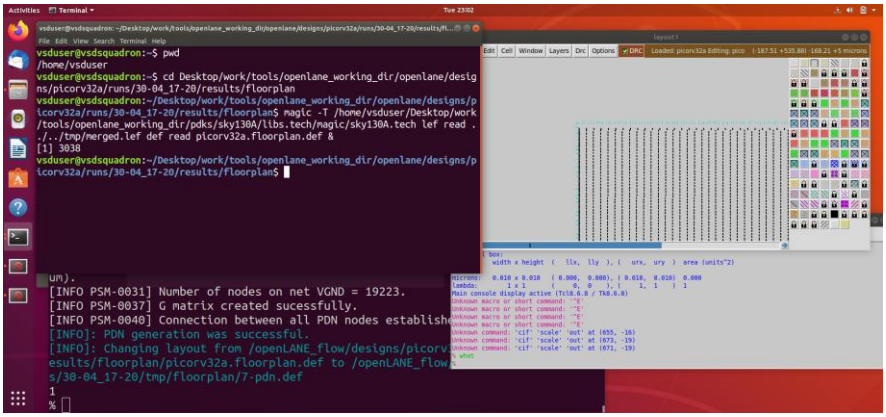
$$Die\ width\ in\ microns = \frac{660685}{1000} = 660.685\ Microns$$

$$Die\ height\ in\ microns = \frac{671405}{1000} = 671.405\ Microns$$

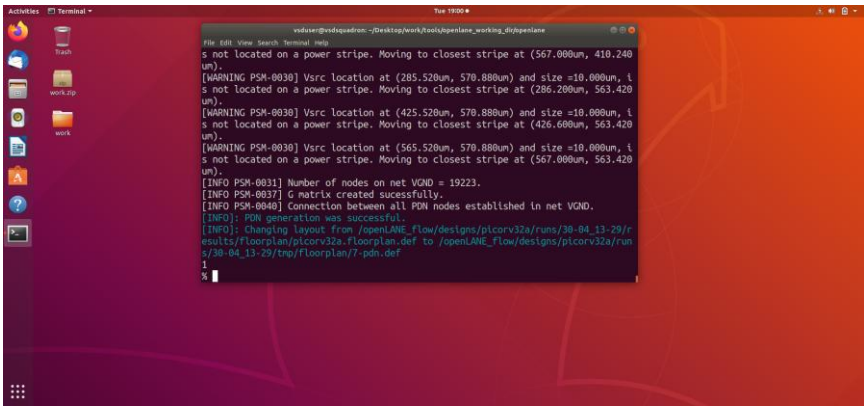
$$Area\ of\ die\ in\ microns = 660.685 * 671.405 = 443587.212425\ Square\ Microns$$

- cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/30-04_13-29/results/floorplan/

- magic -T /home/vsduse/Desktop/work/tools/openlane_working_dir/ pdks/sky130A/libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.floorplan.def &

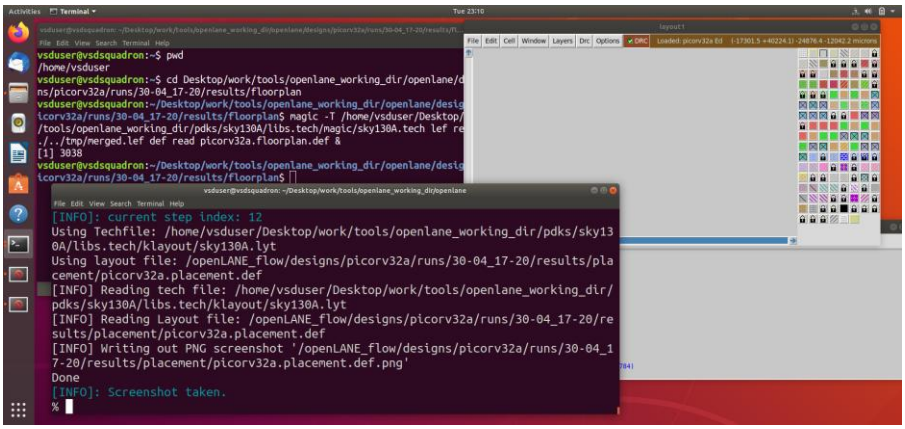


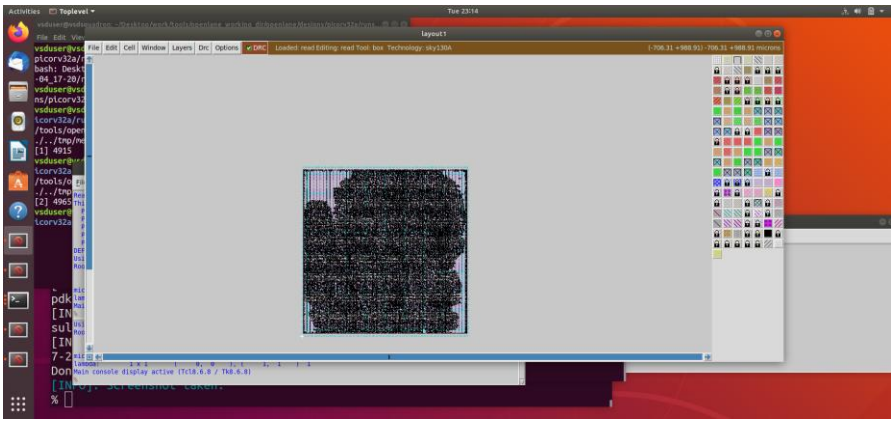
- run_placement



- cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/30-04_13-29/results/placement/

- magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.placement.def &





- exit (exit from openLANE flow)

- exit (exit from docker sub-system)