Section 4 - Pre-layout timing analysis and importance of good clock tree
[24 April – 7 May, 2024]

After the 3rd session, this 4th session contains pre-layout timing analysis with the following steps.

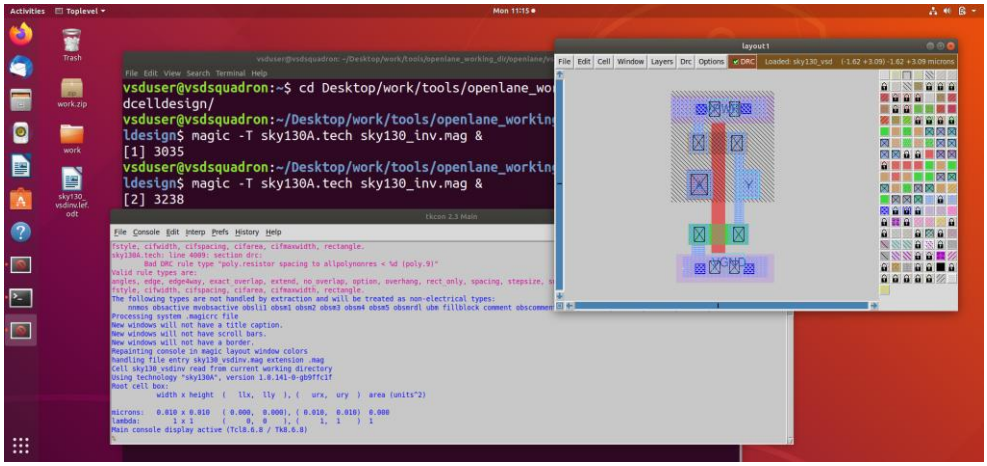
- Including error in the DRC file and verifying it in the present flow
- Save the final layout
- Generate the required lef file from above layout
- Copy lef file and lib file to picorv32a's src directory
- Modify the config.tcl file and add the additional lef information
- Do synthesis in the openlane flow for custom inverter design cell
- If warning /error comes, modify the parameter
- Run floorplan and placement to verify the cell
- Use OpenSTA tool for post synthesis and replace old netlist
- Do Post-CTS based timing analysis and remove few parameters for final design flow

Initial flow contains with custom design cell, which should support its output ports lies on vertical (width-odd multiples) and horizontal (height-even multiples) tracks

❖ **Including error in the DRC file and verifying** - Use vsdstdcelldesign folder

➢ cd Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign

➢ magic -T sky130A.tech sky130_inv.mag &



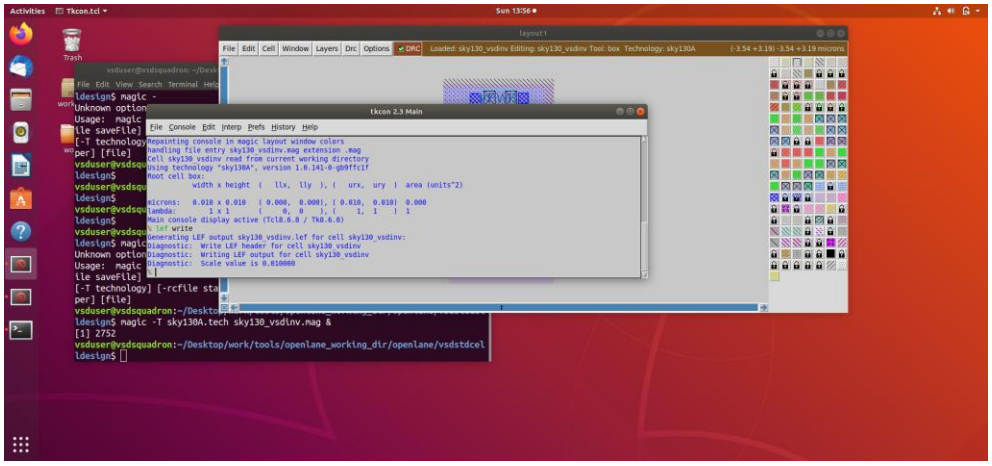
➢ help grid

➢ grid 0.46um 0.34um 0.23um 0.17um

❖ **Save the final layout**

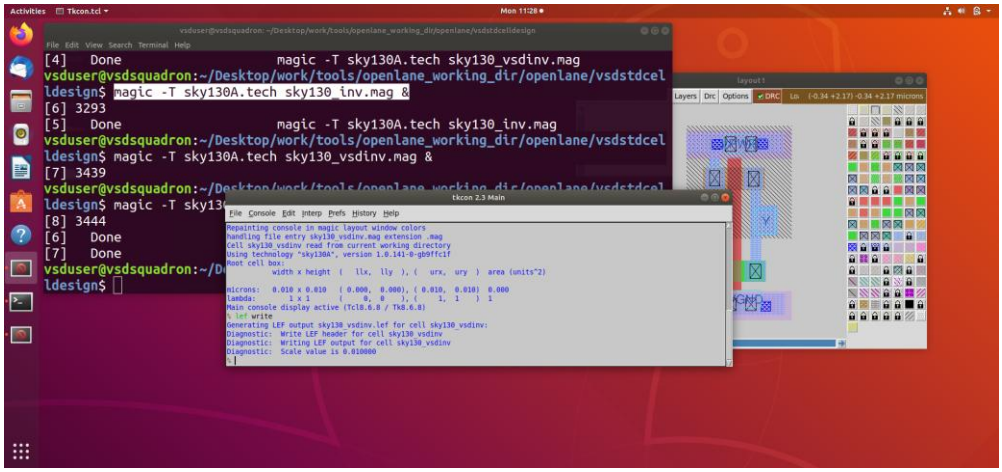
➢ save sky130_vsdinv.mag

➢ magic -T sky130A.tech sky130_vsdinv.mag &



- ❖ **Generate the required lef file**

- ➢ lef write



- ❖ **Copy lef file and lib file to picorv32a's src directory**

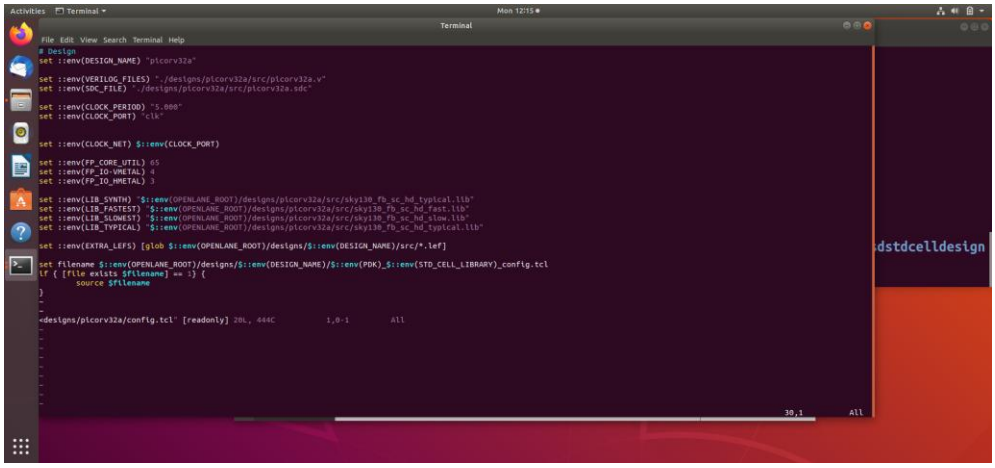
- ➢ cp sky130_vsdinv.lef ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/

- ➢ cp libs/sky130_fd_sc_hd__* ~ /Desktop/work/tools/openlane_working_dir/ openlane/ designs/ picorv32a/src/

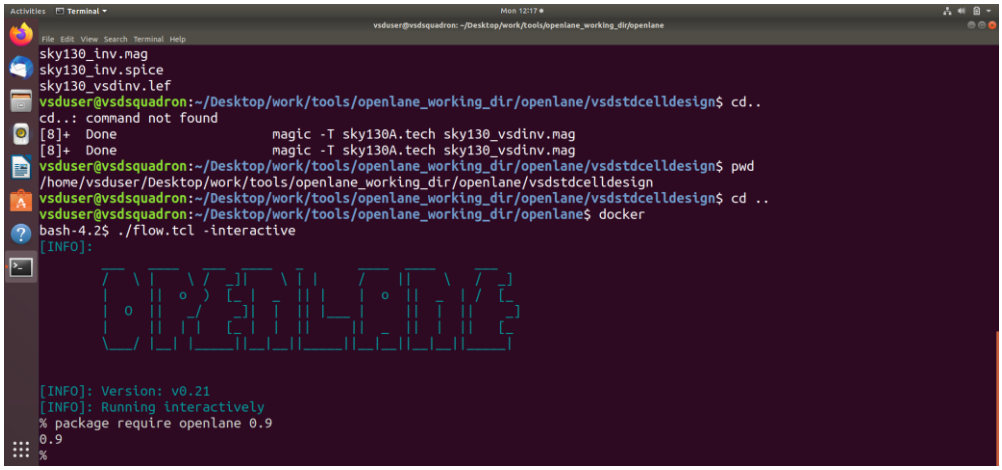
- ❖ **Modify the config.tcl file and add the additional lef information**

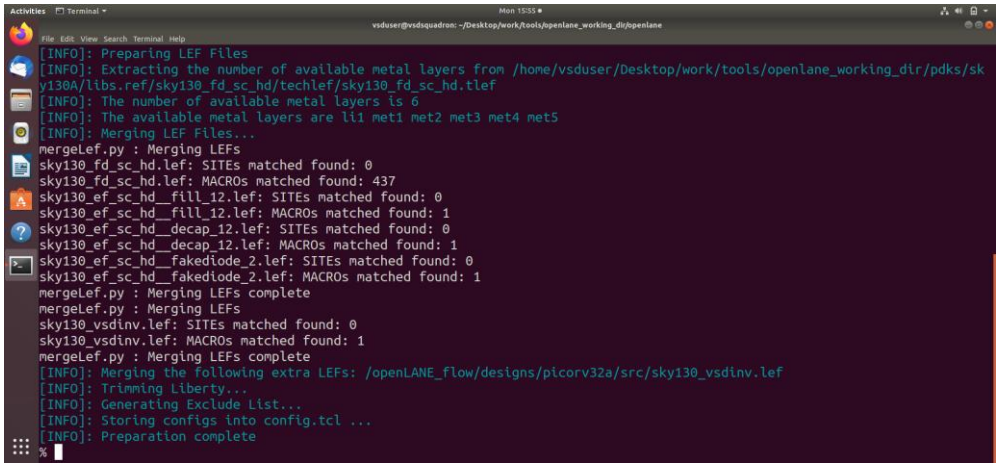
It is necessary to modify confit.tcl file with the following parameters

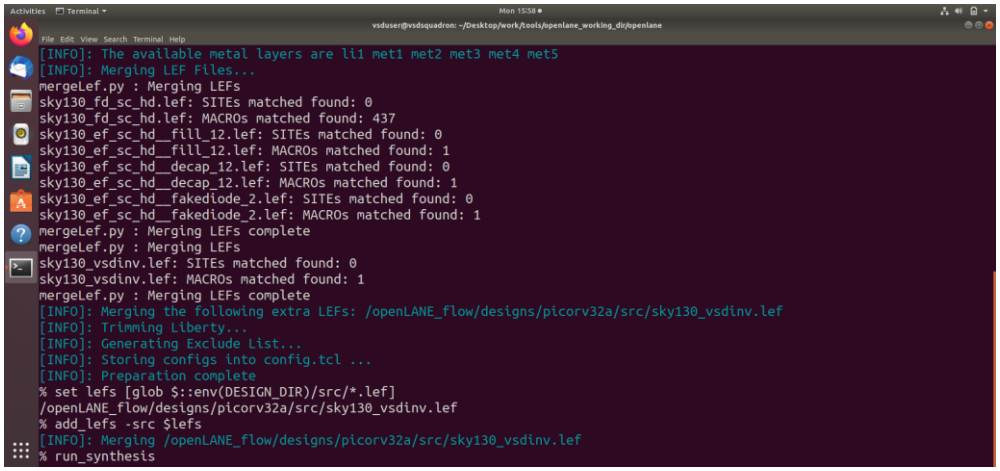
```
set ::env(LIB_SYNTH) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd__typical.lib"
set ::env(LIB_FASTEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd__fast.lib"
set ::env(LIB_SLOWEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd__slow.lib"
set ::env(LIB_TYPICAL) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd__typical.lib"

set ::env(EXTRA_LEFS) [glob $::env(OPENLANE_ROOT)/designs/$::env(DESIGN_NAME)/src/*.lef]
```



- **Do synthesis in the openlane flow for custome inverter design cell**
- cd ~/Desktop/work/tools/openlane_working_dir/openlane
- docker
- bash-4.25 ./flow.tcl –interactive
- Package require openlane 0.9
- prep -design picorv32a
- set lefs [glob$::env(DESIGN_DIR)/src/*.lef]
- add_lefs –src $lefs
- run_synthesis

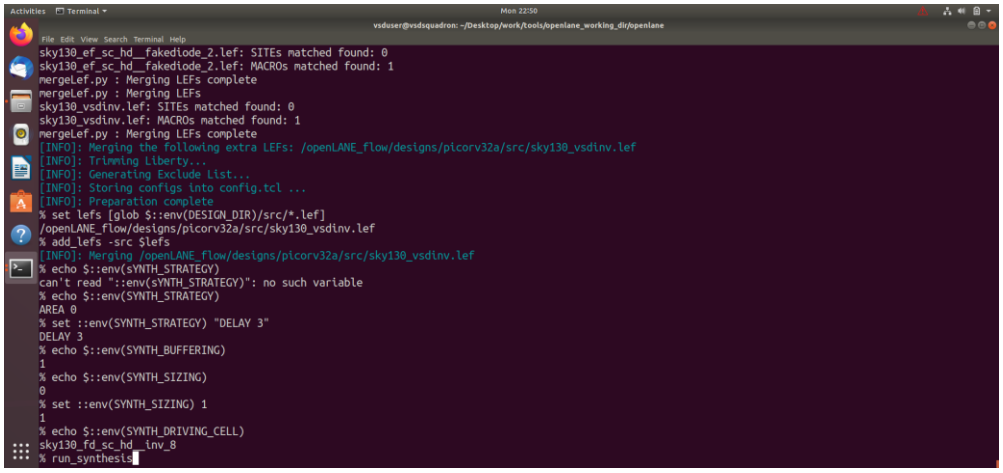


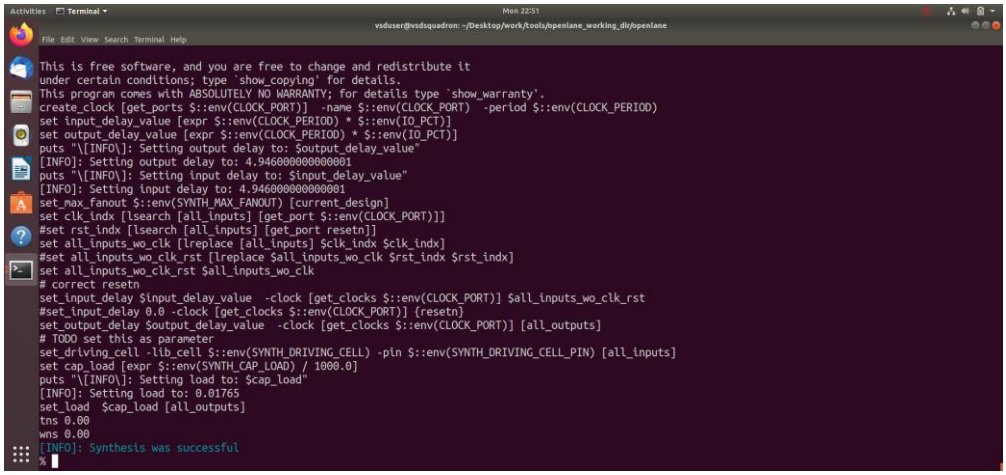




- **Modify the parameter – occurrence of warning /error**

- prep -design picorv32a -tag 24-03_10-03 -overwrite
- set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
- add_lefs –src $lefs
- echo $::env(SYNTH_STRATEGY)
- set ::env(SYNTH_STRATEGY) "DELAY 3"
- echo $::env(SYNTH_BUFFERING)
- echo $::env(SYNTH_SIZING)
- set ::env(SYNTH_SIZING) 1
- echo $::env(SYNTH_DRIVING_CELL)
- run_synthesis



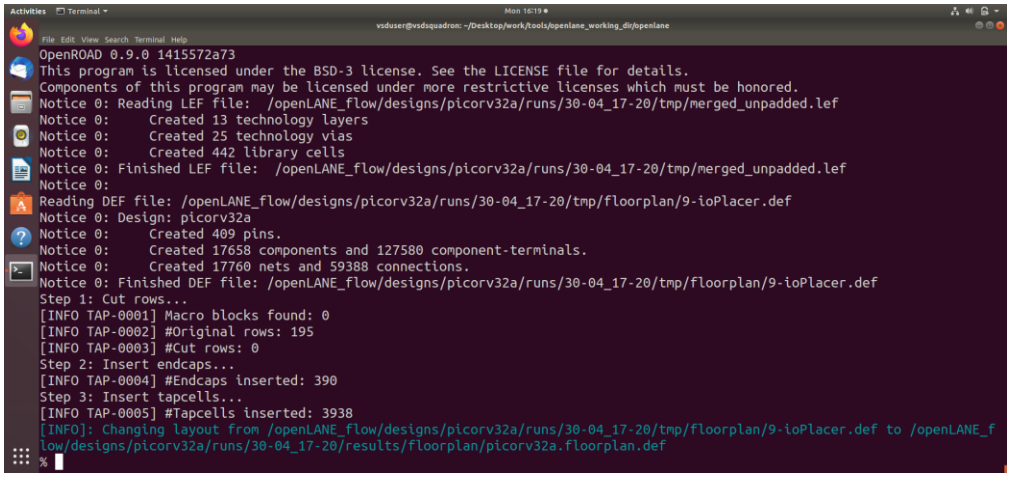


❖ Run floorplan and placement to verify the cell in the PnR

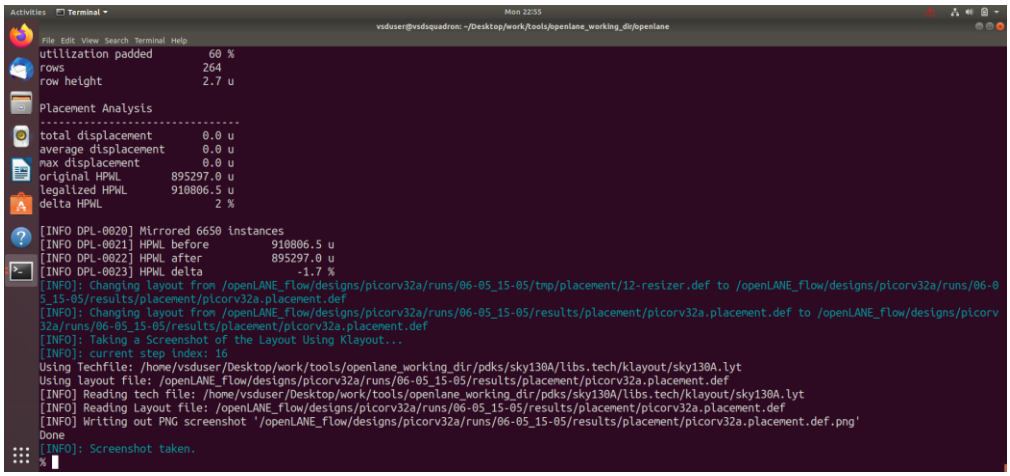
➢ run_floorplan

➢ Follwing commands are alltogather sourced in "run_floorplan" command

init_floorplan
place_io
tap_decap_or



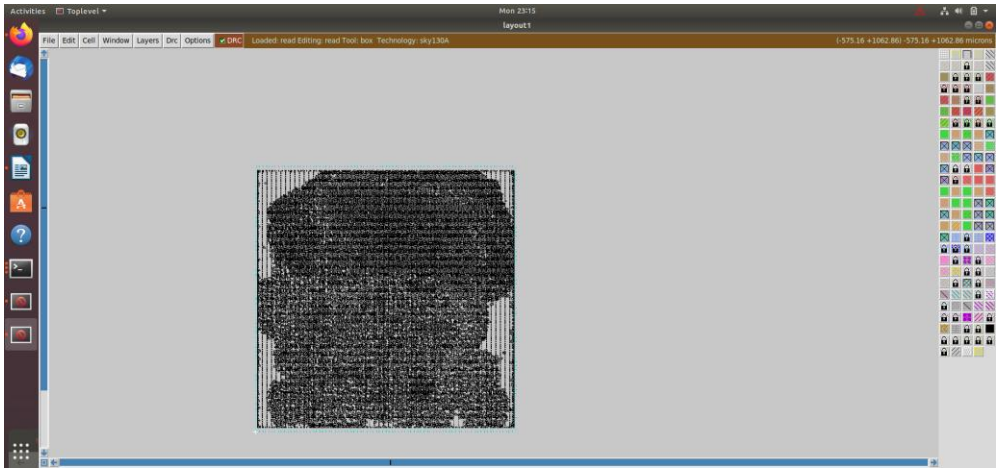
- run_placement



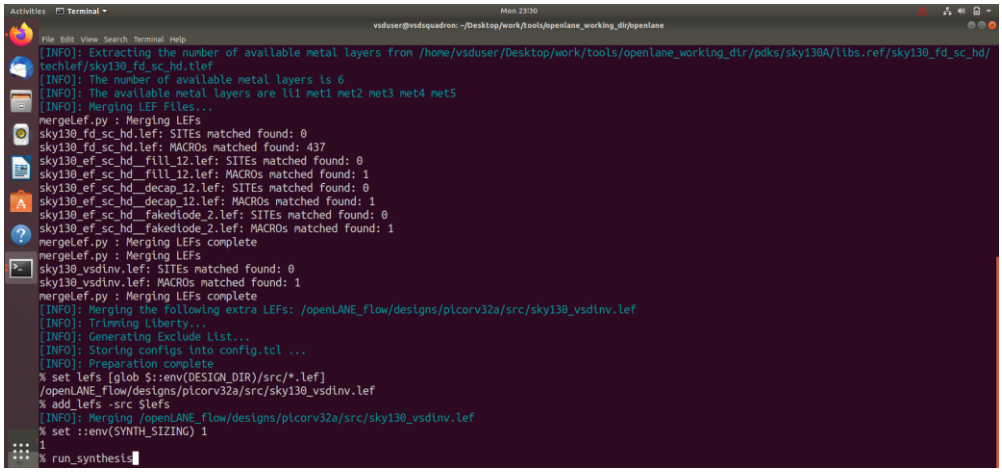
- cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/24-03_10-03/results/placement/

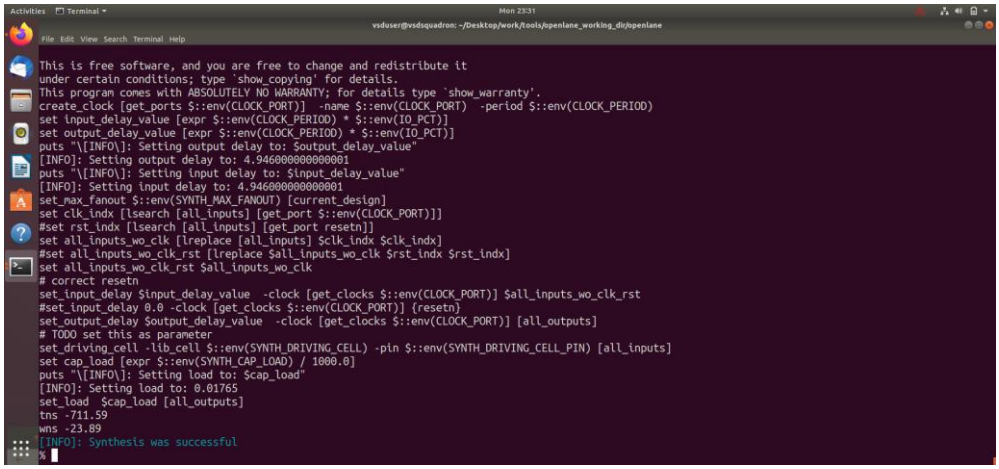
- magic -T /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.placement.def &

- expand



- **Use OpenSTA tool for post synthesis**
- cd Desktop/work/tools/openlane_working_dir/openlane
- docker
- ./flow.tcl –interactive
- package require openlane 0.9
- prep -design picorv32a
- set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
- add_lefs –src $lefs
- set ::env(SYNTH_SIZING) 1
- run_synthesis





- cd Desktop/work/tools/openlane_working_dir/openlane
- sta pre_sta.conf (To invoke OpenSTA tool with script)