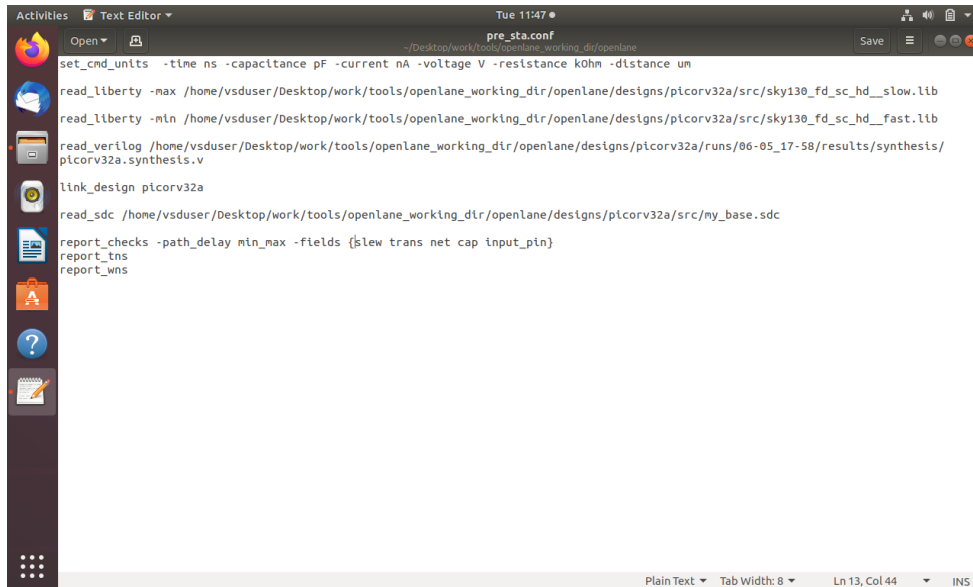


Section 4 - Pre-layout timing analysis and importance of good clock tree [24 April – 7 May, 2024]

The last process in the session 4 is given below.

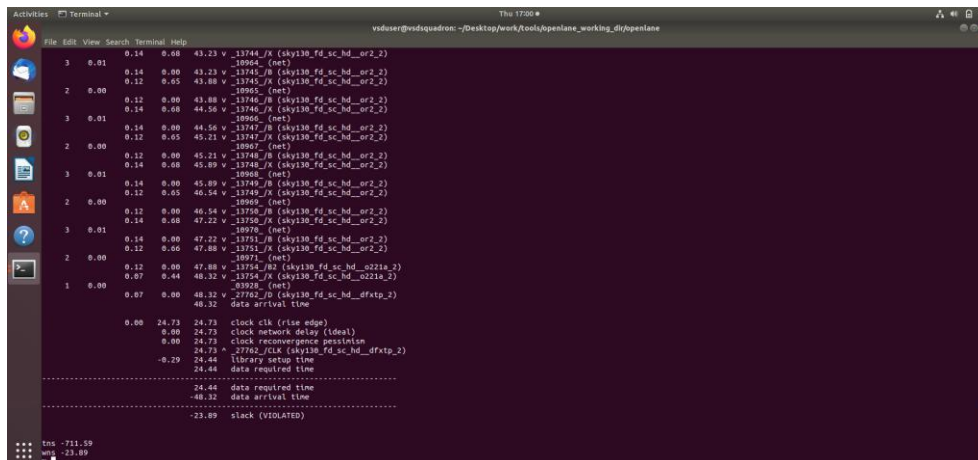
- `cd Desktop/work/tools/openlane_working_dir/openlane`
- `sta pre_sta.conf` (To invoke OpenSTA tool with script)



```
pre_sta.conf
set_cmd_units -time ns -capacitance pF -current nA -voltage V -resistance kohm -distance um
read_liberty -max /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd__slow.lib
read_liberty -min /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd__fast.lib
read_verilog /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/06-05-17-58/results/synthesis/
picorv32a.synthesis.v
link_design picorv32a
read_sdc /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/my_base.sdc
report_checks -path_delay min_max -fields {slew trans net cap input_pin}
report_tns
report_wns
```

It is necessary to create new `pre_sta.conf` for STA analysis in openlane directory. The following commands used to run STA.

- `cd Desktop/work/tools/openlane_working_dir/openlane`
- `sta pre_sta.conf`



```
vduser@vdsiquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
3 0.01 0.14 0.08 43.23 v -13744_/X (sky130_fd_sc_hd__or2_2)
0.01 0.14 0.00 43.23 v -13745_/M (sky130_fd_sc_hd__or2_2)
0.12 0.05 43.88 v -13745_/X (sky130_fd_sc_hd__or2_2)
2 0.00 0.12 0.00 43.88 v -13746_/M (sky130_fd_sc_hd__or2_2)
0.14 0.08 44.56 v -13746_/X (sky130_fd_sc_hd__or2_2)
3 0.01 0.14 0.08 44.56 v -13747_/M (sky130_fd_sc_hd__or2_2)
0.12 0.05 45.21 v -13747_/X (sky130_fd_sc_hd__or2_2)
2 0.00 0.12 0.00 45.21 v -13748_/M (sky130_fd_sc_hd__or2_2)
0.14 0.08 45.89 v -13748_/X (sky130_fd_sc_hd__or2_2)
3 0.01 0.14 0.08 45.89 v -13749_/M (sky130_fd_sc_hd__or2_2)
0.12 0.05 46.54 v -13749_/X (sky130_fd_sc_hd__or2_2)
2 0.00 0.12 0.00 46.54 v -13750_/M (sky130_fd_sc_hd__or2_2)
3 0.01 0.14 0.08 47.22 v -13750_/X (sky130_fd_sc_hd__or2_2)
0.12 0.05 47.88 v -13751_/M (sky130_fd_sc_hd__or2_2)
2 0.00 0.12 0.00 47.88 v -13751_/X (sky130_fd_sc_hd__or2_2)
0.07 0.44 48.32 v -13754_/X (sky130_fd_sc_hd__o221a_2)
1 0.00 0.07 0.00 48.32 v -27762_/M (sky130_fd_sc_hd__dffatp_2)
0.00 24.73 24.73 clock clk (rise edge)
0.00 24.73 clock network delay (ideal)
0.00 24.73 clock reconvergence pessimism
24.73 -27762_/CLK (sky130_fd_sc_hd__dffatp_2)
24.44 library setup time
24.44 data required time
24.44 data required time
-40.22 data arrival time
-23.89 slack (VIOLATED)
```

This following commands used to run the synthesis using new lef file. Use the basic commands also.

- prep -design picorv32a -tag 25-03_18-52 --overwrite
- set lefs [glob\$::env(DSIGN_DIR)/src/*.lef]
- add_lefs -src \$lefs
- set ::env(SYNTH_SIZING) 1
- set ::env(SYNTH_MAX_FANOUT) 4
- echo \$::env(SYNTH_DRIVING_CELL)
- run_synthesis

```

[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITES matched found: 0
sky130_fd_sc_hd.lef: MACROS matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITES matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROS matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITES matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROS matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITES matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROS matched found: 1
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITES matched found: 0
sky130_vsdinv.lef: MACROS matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openlane_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
% set lefs [glob $::env(DSIGN_DIR)/src/*.lef]
/openlane_flow/designs/picorv32a/src/sky130_vsdinv.lef
% add_lefs -src $lefs
[INFO]: Merging /openlane_flow/designs/picorv32a/src/sky130_vsdinv.lef
% set ::env(SYNTH_SIZING) 1
1
% set ::env(SYNTH_MAX_FANOUT) 4
4
% echo $::env(SYNTH_DRIVING_CELL)
sky130_fd_sc_hd_inv_8
% run_synthesis

```

The following commands are used to run new STA files.

- Cd Desktop/work/tools/openlane_working_dir/openlane
- sta pre_sta.conf

```

3 0.01 0.14 0.68 43.24 v _10220_/n (sky130_fd_sc_hd_or2_2)
0.14 0.00 43.24 v _10221_/n (sky130_fd_sc_hd_or2_2)
0.12 0.65 43.46 v _10221_/n (sky130_fd_sc_hd_or2_2)
2 0.00 0.12 0.00 43.89 v _10222_/n (sky130_fd_sc_hd_or2_2)
0.14 0.68 44.57 v _10222_/n (sky130_fd_sc_hd_or2_2)
3 0.01 0.14 0.90 44.57 v _10223_/n (sky130_fd_sc_hd_or2_2)
0.12 0.65 45.22 v _10223_/n (sky130_fd_sc_hd_or2_2)
2 0.00 0.12 0.00 45.22 v _10224_/n (sky130_fd_sc_hd_or2_2)
0.14 0.68 45.90 v _10224_/n (sky130_fd_sc_hd_or2_2)
3 0.01 0.14 0.00 45.90 v _10225_/n (sky130_fd_sc_hd_or2_2)
0.12 0.65 46.55 v _10225_/n (sky130_fd_sc_hd_or2_2)
2 0.00 0.12 0.00 46.55 v _10226_/n (sky130_fd_sc_hd_or2_2)
0.14 0.68 47.23 v _10226_/n (sky130_fd_sc_hd_or2_2)
3 0.01 0.14 0.00 47.23 v _10227_/n (sky130_fd_sc_hd_or2_2)
0.12 0.65 47.89 v _10227_/n (sky130_fd_sc_hd_or2_2)
2 0.00 0.12 0.00 47.89 v _10228_/n2 (sky130_fd_sc_hd_or21a_2)
0.07 0.44 48.33 v _10228_/n (sky130_fd_sc_hd_or21a_2)
1 0.00 0.07 0.00 48.33 v _00440_/n (sky130_fd_sc_hd_dftxp_2)
48.33 data arrival time
0.00 24.73 24.73 clock clk (rise edge)
0.00 24.73 clock network delay (ideal)
0.00 24.73 clock convergence position
24.73 - 38440_/clk (sky130_fd_sc_hd_dftxp_2)
-0.29 24.44 library setup time
24.44 data required time
-----
-24.44 data required time
-48.33 data arrival time
-----
-23.90 slack (V004102)

tns -719.69
wts -23.90

```

❖ Make timing ECO fixes to remove all violations

Use the following commands to optimize timing value. It will few iteration process for better fit of timing value.

- `report_net -connections _11672_`
- `help replace_cell`
- `replace_cell _14510_ sky130_fd_sc_hd__or3_4`
- `report_checks -fields {net cap slew input_pins} -digits 4`

```

vduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
0.1162 0.0000 46.1648 v _15226_/B (sky130_fd_sc_hd__or2_2)
0.1421 0.6813 46.8462 v _15226_/X (sky130_fd_sc_hd__or2_2)
3 0.0079 0.1421 0.0000 46.8462 v _15227_/B (sky130_fd_sc_hd__or2_2)
0.1228 0.6610 47.5072 v _15227_/X (sky130_fd_sc_hd__or2_2)
2 0.0044 0.1228 0.0000 47.5072 v _15227_/X (sky130_fd_sc_hd__or2_2)
0.0713 0.4381 47.9453 v _15230_/B2 (sky130_fd_sc_hd__o221a_2)
1 0.0016 0.0713 0.0000 47.9453 v _15230_/X (sky130_fd_sc_hd__o221a_2)
0.0713 0.0000 47.9453 v _03928_(net)
47.9453 v _30440_/D (sky130_fd_sc_hd__dfxtp_2)
47.9453 data arrival time

0.0000 24.7300 24.7300 clock clk (rise edge)
0.0000 24.7300 clock network delay (ideal)
0.0000 24.7300 clock reconvergence pessimism
24.7300 ^ _30440_/CLK (sky130_fd_sc_hd__dfxtp_2)
-0.2939 24.4361 library setup time
24.4361 data required time

-----
24.4361 data required time
-47.9453 data arrival time
-----
-23.5092 slack (VIOLATED)

```

- `report_net -connections _11675_`
- `replace_cell _14514_ sky130_fd_sc_hd__or3_4`
- `report_checks -fields {net cap slew input_pins} -digits 4`

```

vduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
0.0572 0.0000 0.5830 v _14460_/A (sky130_vsdinv)
0.1856 0.1667 0.7497 ^ _14460_/Y (sky130_vsdinv)
3 0.0138 0.1856 0.0000 0.7497 ^ _14461_/B2 (sky130_fd_sc_hd__o22ai_2)
0.0878 0.1436 0.8933 v _14461_/Y (sky130_fd_sc_hd__o22ai_2)
1 0.0021 0.0878 0.0000 0.8933 v _14462_/C1 (sky130_fd_sc_hd__a221o_2)
0.0784 0.5469 1.4402 v _14462_/X (sky130_fd_sc_hd__a221o_2)
1 0.0013 0.0784 0.0000 1.4402 v _14481_/A (sky130_fd_sc_hd__or4_2)
0.2106 1.5344 2.9746 v _14481_/X (sky130_fd_sc_hd__or4_2)
1 0.0024 0.2106 0.0000 2.9746 v _14509_/A1 (sky130_fd_sc_hd__o2111a_2)
0.0792 0.5466 3.5212 v _14509_/X (sky130_fd_sc_hd__o2111a_2)
2 0.0044 0.0792 0.0000 3.5212 v _14510_/C (sky130_fd_sc_hd__or3_4)
0.1349 0.6755 4.1967 v _14510_/X (sky130_fd_sc_hd__or3_4)
4 0.0089 0.1349 0.0000 4.1967 v _14513_/A (sky130_fd_sc_hd__or2_2)
0.1182 0.6880 4.8847 v _14513_/X (sky130_fd_sc_hd__or2_2)
2 0.0034 0.1182 0.0000 4.8847 v _14514_/X (sky130_fd_sc_hd__or3_4)
0.1290 0.6794 5.5641 v _14514_/X (sky130_fd_sc_hd__or3_4)
4 0.0070 0.1290 0.0000 5.5641 v _15166_/B (sky130_fd_sc_hd__or2_2)
0.1148 0.0414 6.2055 v _15166_/X (sky130_fd_sc_hd__or2_2)

```

```

vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
0.1162 0.0000 45.7962 v _15226_/B (sky130_fd_sc_hd_or2_2)
0.1421 0.6813 46.4775 v _15226_/X (sky130_fd_sc_hd_or2_2)
3 0.0079 0.1421 0.0000 46.4775 v _15227_/B (sky130_fd_sc_hd_or2_2)
0.1228 0.6610 47.1385 v _15227_/X (sky130_fd_sc_hd_or2_2)
2 0.0044 0.1228 0.0000 47.1385 v _15227_/X (sky130_fd_sc_hd_or2_2)
0.0713 0.4381 47.5766 v _15230_/B2 (sky130_fd_sc_hd_o221a_2)
0.0016 0.0713 0.0000 47.5766 v _15230_/X (sky130_fd_sc_hd_o221a_2)
0.0713 0.0000 47.5766 v _30440_/D (sky130_fd_sc_hd_dfxtpt_2)
47.5766 data arrival time
0.0000 24.7300 24.7300 clock clk (rise edge)
0.0000 24.7300 clock network delay (ideal)
0.0000 24.7300 clock reconvergence pessimism
24.7300 ^ _30440_/CLK (sky130_fd_sc_hd_dfxtpt_2)
-0.2939 24.4361 library setup time
24.4361 data required time
-----
24.4361 data required time
-47.5766 data arrival time
-----
-23.1405 slack (VIOLATED)

```

- report_net -connections _11643_
- replace_cell _14481_ sky130_fd_sc_hd__or4_4
- report_checks -fields {net cap slew input_pins} -digits 4

```

vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
0.1162 0.0000 45.7918 v _15226_/B (sky130_fd_sc_hd_or2_2)
0.1421 0.6813 46.4731 v _15226_/X (sky130_fd_sc_hd_or2_2)
3 0.0079 0.1421 0.0000 46.4731 v _15227_/B (sky130_fd_sc_hd_or2_2)
0.1228 0.6610 47.1341 v _15227_/X (sky130_fd_sc_hd_or2_2)
2 0.0044 0.1228 0.0000 47.1341 v _15227_/X (sky130_fd_sc_hd_or2_2)
0.0713 0.4381 47.5723 v _15230_/B2 (sky130_fd_sc_hd_o221a_2)
0.0016 0.0713 0.0000 47.5723 v _15230_/X (sky130_fd_sc_hd_o221a_2)
0.0713 0.0000 47.5723 v _30440_/D (sky130_fd_sc_hd_dfxtpt_2)
47.5723 data arrival time
0.0000 24.7300 24.7300 clock clk (rise edge)
0.0000 24.7300 clock network delay (ideal)
0.0000 24.7300 clock reconvergence pessimism
24.7300 ^ _30440_/CLK (sky130_fd_sc_hd_dfxtpt_2)
-0.2939 24.4361 library setup time
24.4361 data required time
-----
24.4361 data required time
-47.5723 data arrival time
-----
-23.1362 slack (VIOLATED)

```

- report_net -connections _11668_
- replace_cell _14506_ sky130_fd_sc_hd__or4_4
- report_checks -fields {net cap slew input_pins} -digits 4

```

vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
0.1162 0.0000 45.2729 v _15226_/B (sky130_fd_sc_hd_or2_2)
0.1421 0.6813 45.9542 v _15226_/X (sky130_fd_sc_hd_or2_2)
3 0.0079 0.1421 0.0000 45.9542 v _15227_/B (sky130_fd_sc_hd_or2_2)
0.1228 0.6610 46.6153 v _15227_/X (sky130_fd_sc_hd_or2_2)
2 0.0044 0.1228 0.0000 46.6153 v _15230_/B2 (sky130_fd_sc_hd_o221a_2)
0.0713 0.4381 47.0534 v _15230_/X (sky130_fd_sc_hd_o221a_2)
1 0.0016 0.0713 0.0000 47.0534 v _03928_(net)
0.0713 0.0000 47.0534 v _30440_/D (sky130_fd_sc_hd_dfxt_2)
47.0534 data arrival time
-----
0.0000 24.7300 24.7300 clock clk (rise edge)
0.0000 24.7300 clock network delay (ideal)
0.0000 24.7300 clock reconvergence pessimism
-0.2939 24.7300 ^ _30440_/CLK (sky130_fd_sc_hd_dfxt_2)
24.4361 library setup time
24.4361 data required time
-----
24.4361 data required time
-47.0534 data arrival time
-----
-22.6173 slack (VIOLATED)

```

➤ report_checks -from _29043_ -to _30440_ -through _14506_

```

vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
0.1162 0.0000 45.2729 v _15226_/B (sky130_fd_sc_hd_or2_2)
0.1421 0.6813 45.9542 v _15226_/X (sky130_fd_sc_hd_or2_2)
3 0.0079 0.1421 0.0000 45.9542 v _15227_/B (sky130_fd_sc_hd_or2_2)
0.1228 0.6610 46.6153 v _15227_/X (sky130_fd_sc_hd_or2_2)
2 0.0044 0.1228 0.0000 46.6153 v _15230_/B2 (sky130_fd_sc_hd_o221a_2)
0.0713 0.4381 47.0534 v _15230_/X (sky130_fd_sc_hd_o221a_2)
1 0.0016 0.0713 0.0000 47.0534 v _03928_(net)
0.0713 0.0000 47.0534 v _30440_/D (sky130_fd_sc_hd_dfxt_2)
47.0534 data arrival time
-----
0.0000 24.7300 24.7300 clock clk (rise edge)
0.0000 24.7300 clock network delay (ideal)
0.0000 24.7300 clock reconvergence pessimism
-0.2939 24.7300 ^ _30440_/CLK (sky130_fd_sc_hd_dfxt_2)
24.4361 library setup time
24.4361 data required time
-----
24.4361 data required time
-47.0534 data arrival time
-----
-22.6173 slack (VIOLATED)
% report_checks -from _29043_ -to _30440_ -through _14506_

```

```

vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
-47.0534 data arrival time
-----
-22.6173 slack (VIOLATED)
% report_checks -from _29043_ -to _30440_ -through _14506_
Startpoint: _29043_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: _30440_ (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max
Delay Time Description
-----
0.00 0.00 clock clk (rise edge)
0.00 0.00 clock network delay (ideal)
0.00 0.00 ^ _29043_/CLK (sky130_fd_sc_hd_dfxt_2)
0.58 0.58 v _29043_/Q (sky130_fd_sc_hd_dfxt_2)
0.17 0.75 ^ _14484_/Y (sky130_vsdinv)
0.17 0.92 v _14486_/Y (sky130_fd_sc_hd_o221a_2)
0.56 1.48 v _14487_/X (sky130_fd_sc_hd_a221o_2)
1.02 2.50 v _14506_/X (sky130_fd_sc_hd_or4_4)
0.49 2.99 v _14509_/X (sky130_fd_sc_hd_o2111a_2)
0.68 3.67 v _14510_/X (sky130_fd_sc_hd_or3_4)
0.69 4.36 v _14513_/X (sky130_fd_sc_hd_or2_2)
0.68 5.04 v _14514_/X (sky130_fd_sc_hd_or3_4)
0.64 5.68 v _15166_/X (sky130_fd_sc_hd_or2_2)

```

❖ New netlist generated after timing ECO

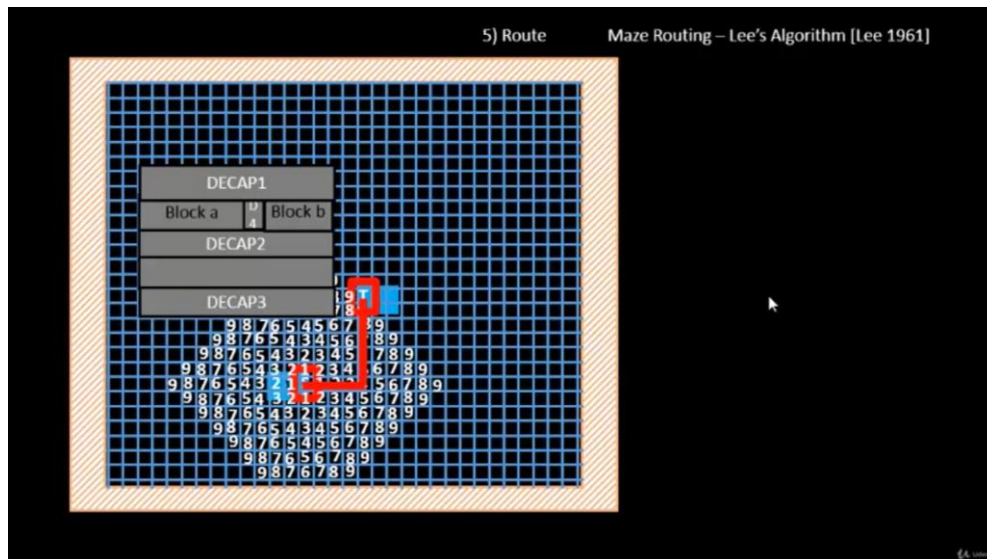
➤ Cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/09-05_16_40/results/synthesis/

➤ cp picorv32a.synthesis.v picorv32a.synthesis_old.v

Session 5 - Final steps for RTL2GDS using TritonRoute and openSTA [24 April – 7 May, 2024]

This last session is mainly focusing on RTL to GDSII file with proper triton route and OpenSTA approach. This session starts with Routing and Design Rule Check (DRC) by using Maze routing – Lee's algorithm.

The following image shows the concept of Lee algorithm, which is used in the maze routing and follow by the DRC approach.



The following commands help for CTS using TritonRoute and openSTA

Replace the new file with old .v file using write_verilog

- run_floorplan
- run_placement
- run_cts
- read_lef /openLANE_flow/designs/picorv32a/runs/04-05_21-50/tmp/merged.lef
- read_def /openLANE_flow/designs/picorv32a/runs/04-05_21-50/results/cts/picorv32a.cts.def
- write_db pico_cts.db
- read_db pico_cts.db
- read_verilog /openLANE_flow/designs/picorv32a/runs/04-05_21-50/results/synthesis/picorv32a.synthesis_cts.v
- read_liberty \$::env(LIB_SYNTH_COMPLETE)

- `read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc`
- `set_propagated_clock [all_clocks]`
- `report_checks -path_delay min_max -format full_clock_expanded -digits 4`
- `set ::env(CTS_CLK_BUFFER_LIST) [lreplace $::env(CTS_CLK_BUFFER_LIST) 0 0]`
- `echo $::env(CTS_CLK_BUFFER_LIST)`
- `echo $::env(CURRENT_DEF)`
- `run_cts`

After the above stages, it is necessary to generate power distributed network using `gen_pdn` and also use routing with `run_routing`. The final results will be notified in magic tool – layout design.