

## Section 4 - Pre-layout timing analysis and importance of good clock tree

### Session 5 - Final steps for RTL2GDS using tritonRoute and openSTA

[24 April – 7 May, 2024]

After the 3<sup>rd</sup> session, this 4<sup>th</sup> session contains pre-layout timing analysis with the following steps.

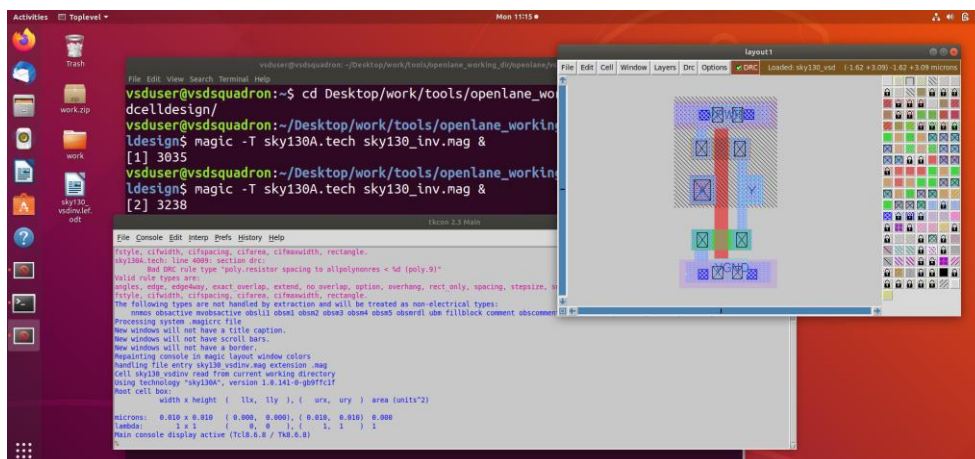
- Including error in the DRC file and verifying it in the present flow
- Save the final layout
- Generate the required lef file from above layout
- Copy lef file and lib file to picorv32a's src directory
- Modify the config.tcl file and add the additional lef information
- Do synthesis in the openlane flow for custom inverter design cell
- If warning /error comes, modify the parameter
- Run floorplan and placement to verify the cell
- Use OpenSTA tool for post synthesis and replace old netlist
- Do Post-CTS based timing analysis and remove few parameters for final design flow

Initial flow contains with custom design cell, which should support its output ports lies on vertical (width-odd multiples) and horizontal (height-even multiples) tracks

❖ **Including error in the DRC file and verifying** - Use vsdstdcelldesign folder

➤ `cd Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign`

➤ `magic -T sky130A.tech sky130_inv.mag &`



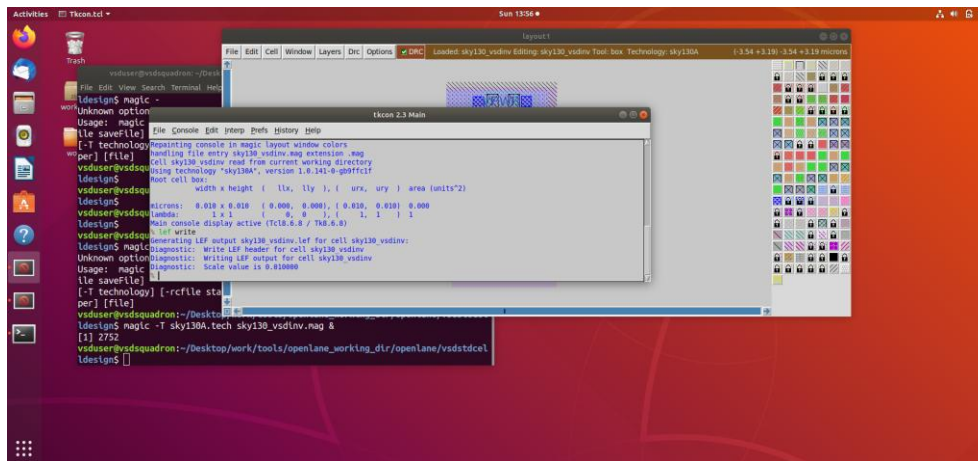
➤ `help grid`

➤ `grid 0.46um 0.34um 0.23um 0.17um`

❖ **Save the final layout**

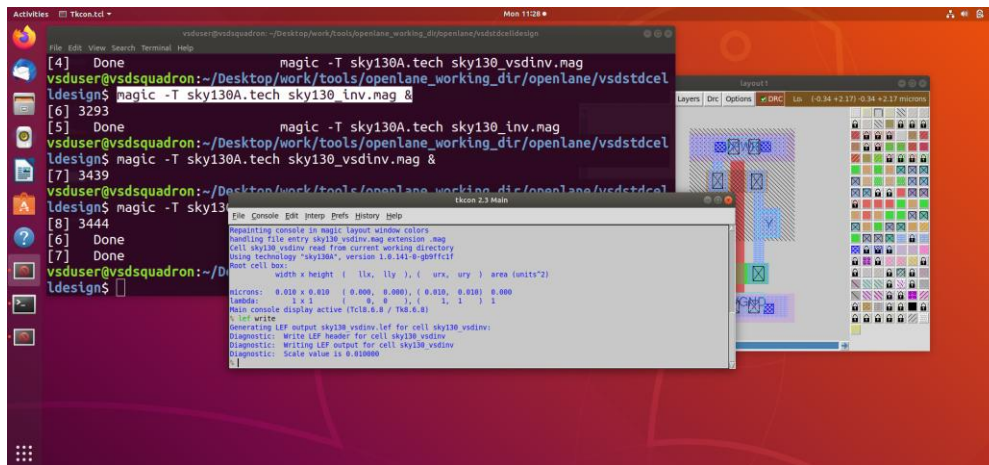
➤ `save sky130_vsdinv.mag`

➤ `magic -T sky130A.tech sky130_vsdinv.mag &`



## ❖ Generate the required lef file

### ➤ lef write



## ❖ Copy lef file and lib file to picorv32a's src directory

### ➤ cp sky130\_vsdinv.lef ~/Desktop/work/tools/openlane\_working\_dir/openlane/designs/picorv32a/src/

### ➤ cp libs/sky130\_fd\_sc\_hd\_\* ~/Desktop/work/tools/openlane\_working\_dir/openlane/designs/picorv32a/src/

## ❖ Modify the config.tcl file and add the additional lef information

It is necessary to modify config.tcl file with the following parameters

```
set ::env(LIB_SYNTH) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib"
set ::env(LIB_FASTEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib"
set ::env(LIB_SLOWEST) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib"
set ::env(LIB_TYPICAL) "$::env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fd_sc_hd_typical.lib"
```

```
set ::env(EXTRA_LEFS) [glob $::env(OPENLANE_ROOT)/designs/$::env(DESIGN_NAME)/src/*.lef]
```

```

# design
set :env(DSIGN_NAME) "picorv32a"
set :env(VERILOG_FILES) ".designs/picorv32a/src/picorv32a.v"
set :env(SDC_FILE) ".designs/picorv32a/src/picorv32a.sdc"
set :env(CLOCK_PERIOD) "5.000"
set :env(CLOCK_PORT) clk

set :env(CLOCK_NET) $:env(CLOCK_PORT)

set :env(FP_CORE_UTIL) 65
set :env(FP_ID_UTIL) 4
set :env(FP_ID_UTIL) 3

set :env(LIB_SWITCH) $:env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fb_sc_hd_typical.lib
set :env(LIB_FASTEST) $:env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fb_sc_hd_fast.lib
set :env(LIB_SLOWEST) $:env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fb_sc_hd_slow.lib
set :env(LIB_TYPICAL) $:env(OPENLANE_ROOT)/designs/picorv32a/src/sky130_fb_sc_hd_typical.lib

set :env(EXTRA_LEFS) [glob $:env(OPENLANE_ROOT)/designs/$:env(DSIGN_NAME)/src/*.lef]

set filename $:env(OPENLANE_ROOT)/designs/$:env(DSIGN_NAME)/$:env(PDK)/$:env(STD_CELL_LIBRARY)/config.tcl
if { [file exists $filename] == 1 } {
    source $filename
}

~designs/picorv32a/config.tcl [readonly] 20k, 64kC 1,0-1 All

```

## ❖ Do synthesis in the openlane flow for custome inverter design cell

- cd ~/Desktop/work/tools/openlane\_working\_dir/openlane
- docker
- bash-4.25 ./flow.tcl -interactive
- Package require openlane 0.9
- prep -design picorv32a
- set lefs [glob\$::env(DSIGN\_DIR)/src/\*.lef]
- add\_lefs -src \$lefs
- run\_synthesis

```

sky130_inv.mag
sky130_inv.spice
sky130_vsdinv.lef
vdsuser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cd..
cd..: command not found
[8]+ Done magic -T sky130A.tech sky130_vsdinv.mag
[8]+ Done magic -T sky130A.tech sky130_vsdinv.mag
vdsuser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ pwd
/home/vdsuser/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
vdsuser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cd ..
vdsuser@vdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ docker
bash-4.25 ./flow.tcl -interactive
[INFO]:
[INFO]: Version: v0.21
[INFO]: Running interactively
% package require openlane 0.9
0.9
%

```

```

Activities Terminal
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[INFO]: Preparing LEF Files
[INFO]: Extracting the number of available metal layers from /home/vdsuser/Desktop/work/tools/openlane_working_dir/pdks/sk
y130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.tlef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are li1 met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITES matched found: 0
sky130_fd_sc_hd.lef: MACROS matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITES matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROS matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITES matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROS matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITES matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROS matched found: 1
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITES matched found: 0
sky130_vsdinv.lef: MACROS matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
%

```

```

Activities Terminal
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[INFO]: The available metal layers are li1 met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITES matched found: 0
sky130_fd_sc_hd.lef: MACROS matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITES matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROS matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITES matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROS matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITES matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROS matched found: 1
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITES matched found: 0
sky130_vsdinv.lef: MACROS matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
% set lefs [glob $::env(DSIGN_DIR)/src/*.lef]
/openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% add_lefs -src $lefs
[INFO]: Merging /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
% run_synthesis

```

## ❖ Modify the parameter – occurrence of warning /error

- prep -design picorv32a -tag 24-03\_10-03 -overwrite
- set lefs [glob \$::env(DSIGN\_DIR)/src/\*.lef]
- add\_lefs -src \$lefs
- echo \$::env(SYNTH\_STRATEGY)
- set ::env(SYNTH\_STRATEGY) "DELAY 3"
- echo \$::env(SYNTH\_BUFFERING)
- echo \$::env(SYNTH\_SIZING)
- set ::env(SYNTH\_SIZING) 1
- echo \$::env(SYNTH\_DRIVING\_CELL)
- run\_synthesis

```

RECT 0.145000 2.635000 0.315000 2.805000 ;
RECT 0.605000 -0.005000 0.775000 1.005000 ;
RECT 0.605000 2.635000 0.775000 2.805000 ;
END
END sky130_ef_sc_hd_fakediode_2
CLASS CORE ;
FOREIGN sky130_vsdinv ;
ORIGIN 0.800 0.800 ;
SIZE 1.300 BY 2.720 ;
SITE unithd ;
PIN A
DIRECTION INPUT ;
USE SIGNAL ;
ANTENNA_GATEAREA 0.105600 ;
PORT
LAYER l11 ;
RECT 0.000 1.100 0.510 1.090 ;
END A
PIN V
DIRECTION OUTPUT ;
USE SIGNAL ;
ANTENNA_GATEAREA 0.207000 ;
PORT
LAYER l11 ;
RECT 0.700 1.900 1.100 2.330 ;
RECT 0.800 1.600 1.050 1.900 ;
RECT 0.800 1.100 1.330 1.090 ;
RECT 0.800 0.700 1.050 1.100 ;
RECT 0.700 0.410 1.330 0.700 ;
END
END V
DIRECTION INPUT ;
USE POWER ;
PORT
LAYER mwll ;
RECT -0.200 1.140 1.570 3.040 ;
LAYER l11 ;
RECT -0.200 2.580 1.430 2.900 ;
RECT 0.100 2.330 0.350 2.580 ;
RECT 0.100 1.970 0.440 2.330 ;
LAYER mcon ;

```

```

sky130_ef_sc_hd_fakediode_2.lef: SITES matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITES matched found: 0
sky130_vsdinv.lef: MACROs matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openlane_flow/designs/picorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming Liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
% set lefs [glob $::env(DESIGN_DIR)/src/* lef]
/openlane_flow/designs/picorv32a/src/sky130_vsdinv.lef
% add_lefs -src $lefs
[INFO]: Merging /openlane_flow/designs/picorv32a/src/sky130_vsdinv.lef
% echo $::env(SYNTH_STRATEGY)
can't read "env(SYNTH_STRATEGY)": no such variable
% echo $::env(SYNTH_STRATEGY)
AREA 0
% set ::env(SYNTH_STRATEGY) "DELAY 3"
DELAY 3
% echo $::env(SYNTH_BUFFERING)
1
% echo $::env(SYNTH_SIZING)
0
% set ::env(SYNTH_SIZING) 1
1
% echo $::env(SYNTH_DRIVING_CELL)
sky130_fd_sc_hd_inv_8
% run_synthesis

```

```

This is free software, and you are free to change and redistribute it
under certain conditions; type 'show copying' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type 'show warranty'.
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "[INFO]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "[INFO]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_idx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_idx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [replace [all_inputs] $clk_idx $clk_idx]
#set all_inputs_wo_clk_rst [replace [all_inputs_wo_clk] $rst_idx $rst_idx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "[INFO]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns 0.00
wns 0.00
[INFO]: Synthesis was successful
%

```

## ❖ Run floorplan and placement to verify the cell in the PnR

### ➤ run\_floorplan

➤ Following commands are alltogether sourced in "run\_floorplan" command

init\_floorplan

place\_io

tap\_decap\_or



```

OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/30-04_17-20/tmp/merged_unpadded.lef
Notice 0: Created 13 technology layers
Notice 0: Created 25 technology vias
Notice 0: Created 442 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/30-04_17-20/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/30-04_17-20/tmp/floorplan/9-ioPlacer.def
Notice 0: Design: picorv32a
Notice 0: Created 409 pins.
Notice 0: Created 17658 components and 127580 component-terminals.
Notice 0: Created 17760 nets and 59388 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/30-04_17-20/tmp/floorplan/9-ioPlacer.def
Step 1: Cut rows...
[INFO TAP-0001] Macro blocks found: 0
[INFO TAP-0002] #Original rows: 195
[INFO TAP-0003] #Cut rows: 0
Step 2: Insert endcaps...
[INFO TAP-0004] #Endcaps inserted: 390
Step 3: Insert tapcells...
[INFO TAP-0005] #Tapcells inserted: 3938
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/30-04_17-20/tmp/floorplan/9-ioPlacer.def to /openLANE_flow/designs/picorv32a/runs/30-04_17-20/results/floorplan/picorv32a.floorplan.def
%

```

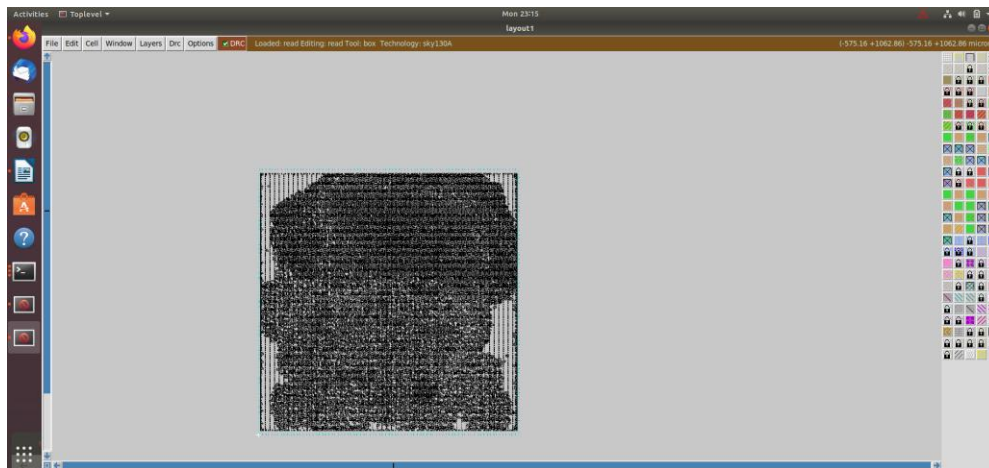
➤ run\_placement

```

utilization padded 60 %
rows 264
row height 2.7 u
Placement Analysis
-----
total displacement 0.0 u
average displacement 0.0 u
max displacement 0.0 u
original HPWL 895297.0 u
legalized HPWL 910806.5 u
delta HPWL 2 %
[INFO DPL-0020] Mirrored 6650 instances
[INFO DPL-0021] HPWL before 910806.5 u
[INFO DPL-0022] HPWL after 895297.0 u
[INFO DPL-0023] HPWL delta -1.7 %
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/06-05_15-05/tmp/placement/12-resizer.def to /openLANE_flow/designs/picorv32a/runs/06-05_15-05/results/placement/picorv32a.placement.def
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/06-05_15-05/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/06-05_15-05/results/placement/picorv32a.placement.def
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 16
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/06-05_15-05/results/placement/picorv32a.placement.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/06-05_15-05/results/placement/picorv32a.placement.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/06-05_15-05/results/placement/picorv32a.placement.def.png'
Done
[INFO]: Screenshot taken.
%

```

- cd Desktop/work/tools/openlane\_working\_dir/openlane/designs/picorv32a/runs/24-03\_10-03/results/placement/
- magic -T /home/vsduser/Desktop/work/tools/openlane\_working\_dir/pdks/sky130A/libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.placement.def &
- expand



## ❖ Use OpenSTA tool for post synthesis

- `cd Desktop/work/tools/openlane_working_dir/openlane`
- `docker`
- `./flow.tcl -interactive`
- package require openlane 0.9
- `prep -design picorv32a`
- `set lefs [glob $::env(DESIGN_DIR)/src/*.lef]`
- `add_lefs -src $lefs`
- `set ::env(SYNTH_SIZING) 1`
- `run_synthesis`

```

Activities Terminal v
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
[INFO]: Extracting the number of available metal layers from /home/vdsuser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.tlef
[INFO]: The number of available metal layers is 6
[INFO]: The available metal layers are li1 met1 met2 met3 met4 met5
[INFO]: Merging LEF Files...
mergeLef.py : Merging LEFs
sky130_fd_sc_hd.lef: SITES matched found: 0
sky130_fd_sc_hd.lef: MACROS matched found: 437
sky130_ef_sc_hd_fill_12.lef: SITES matched found: 0
sky130_ef_sc_hd_fill_12.lef: MACROS matched found: 1
sky130_ef_sc_hd_decap_12.lef: SITES matched found: 0
sky130_ef_sc_hd_decap_12.lef: MACROS matched found: 1
sky130_ef_sc_hd_fakediode_2.lef: SITES matched found: 0
sky130_ef_sc_hd_fakediode_2.lef: MACROS matched found: 1
mergeLef.py : Merging LEFs complete
mergeLef.py : Merging LEFs
sky130_vsdinv.lef: SITES matched found: 0
sky130_vsdinv.lef: MACROS matched found: 1
mergeLef.py : Merging LEFs complete
[INFO]: Merging the following extra LEFs: /openlane_flow/designs/plcorv32a/src/sky130_vsdinv.lef
[INFO]: Trimming liberty...
[INFO]: Generating Exclude List...
[INFO]: Storing configs into config.tcl ...
[INFO]: Preparation complete
% set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
/openlane_flow/designs/plcorv32a/src/sky130_vsdinv.lef
% add_lefs -src $lefs
[INFO]: Merging /openlane_flow/designs/plcorv32a/src/sky130_vsdinv.lef
% set ::env(SYNTH_SIZING) 1
1
% run_synthesis
  
```

```
Mon 23:31
vdsuser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane

This is free software, and you are free to change and redistribute it
under certain conditions; type 'show_copyright' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type 'show_warranty'.
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "[INFO]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.9460000000000001
puts "[INFO]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.9460000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_idx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_idx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_idx $clk_idx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_idx $rst_idx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "[INFO]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -711.59
wns -23.89
[INFO]: Synthesis was successful
%
```

- cd Desktop/work/tools/openlane\_working\_dir/openlane
- sta pre\_sta.conf (To invoke OpenSTA tool with script)

```
Tue 11:47 ●
pre_sta.conf
~/Desktop/work/tools/openlane_working_dir/openlane

set_cmd_units -time ns -capacitance pF -current nA -voltage V -resistance kOhm -distance um

read_liberty -max /home/vdsuser/Desktop/work/tools/openlane_working_dir/openlane/designs/plcorv32a/src/sky130_fd_sc_hd__slow.lib
read_liberty -min /home/vdsuser/Desktop/work/tools/openlane_working_dir/openlane/designs/plcorv32a/src/sky130_fd_sc_hd__fast.lib
read_verilog /home/vdsuser/Desktop/work/tools/openlane_working_dir/openlane/designs/plcorv32a/runs/06-05-17-58/results/synthesis/plcorv32a.synthesis.v
link_design plcorv32a

read_sdc /home/vdsuser/Desktop/work/tools/openlane_working_dir/openlane/designs/plcorv32a/src/my_base.sdc

report_checks -path_delay min_max -fields {slew trans net cap input_pin}
report_tns
report_wns

Plain Text Tab Width: 8 Ln 13, Col 44 INS
```