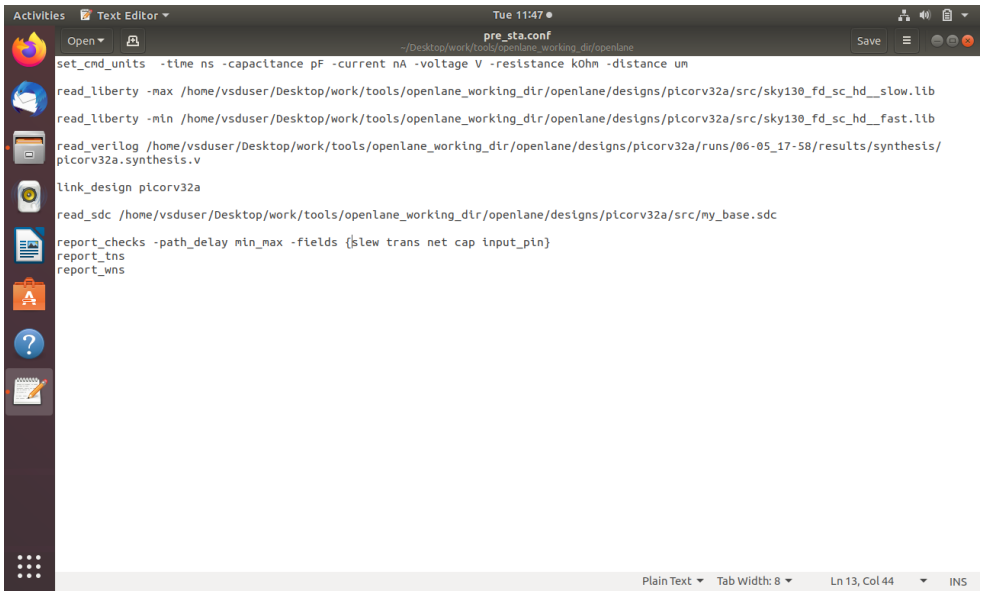
Section 4 - Pre-layout timing analysis and importance of good clock tree [24 April – 7 May, 2024]

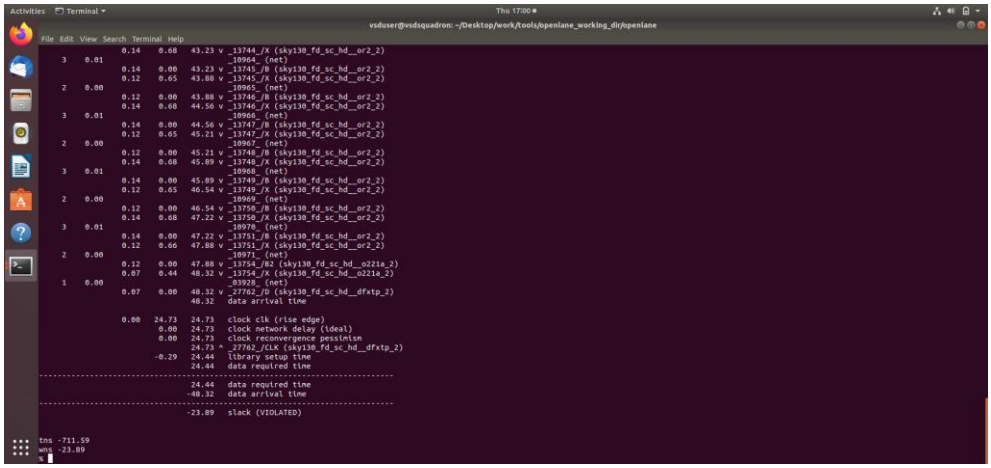
The last process in the session 4 is given below.

- cd Desktop/work/tools/openlane_working_dir/openlane
- sta pre_sta.conf (To invoke OpenSTA tool with script)



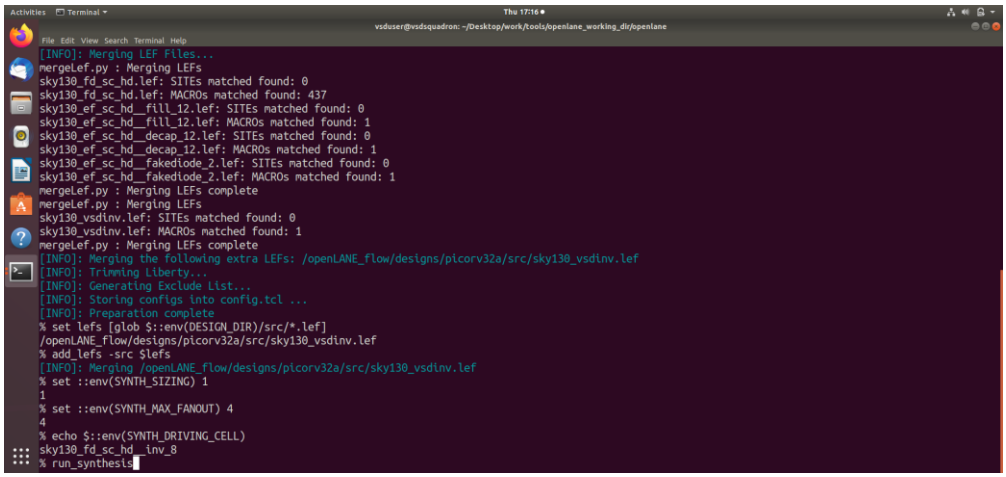
It is necessary to create new pre_sta.conf for STA analysis in openlane directory. The following commends used to run STA.

- cd Desktop/work/tools/openlane_working_dir/openlane
- sta pre_sta.conf



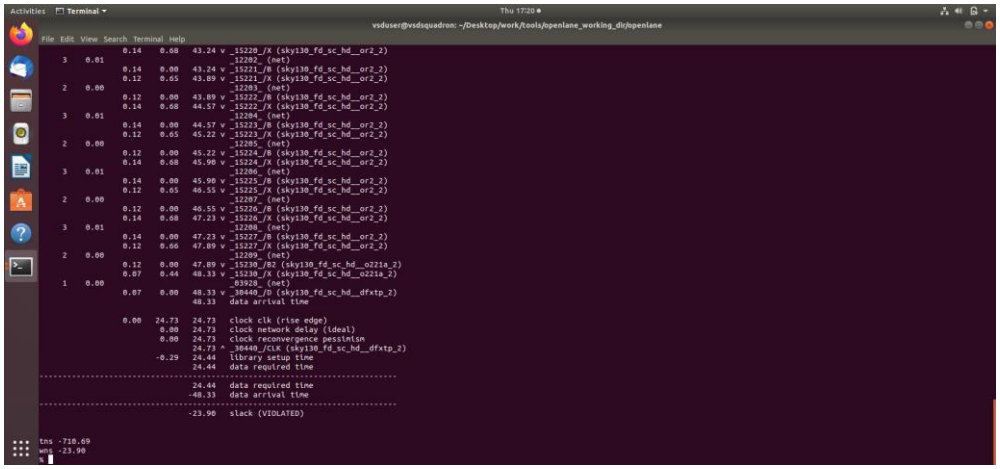
This following commends used to run the synthesis using new lef file. Use the basic commends also.

- prep -design picorv32a -tag 25-03_18-52 –overwrite
- set lefs [glob$::env(DESIGN_DIR)/src/*.lef]
- add_lefs –src $lefs
- set ::env(SYNTH_SIZING) 1
- set ::env(SYNTH_MAX_FANOUT) 4
- echo $::env(SYNTH_DRIVING_CELL)
- run_synthesis



The following commends are used to run new STA files.

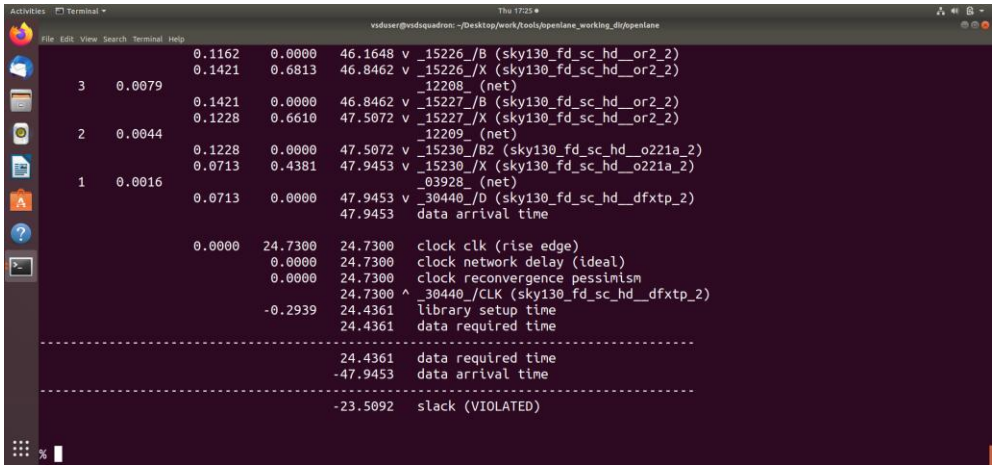
- Cd Desktop/work/tools/openlane_working_dir/openlane
- sta pre_sta.conf



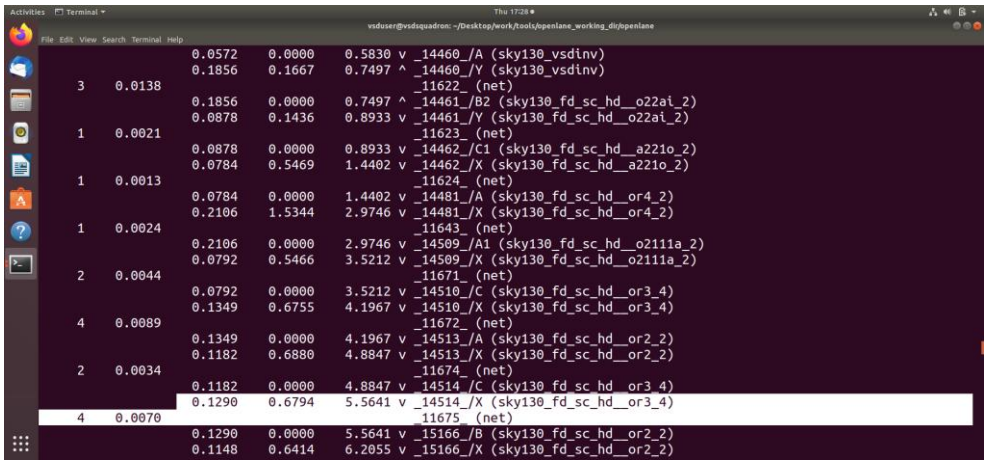
- ❖ Make timing ECO fixes to remove all violations

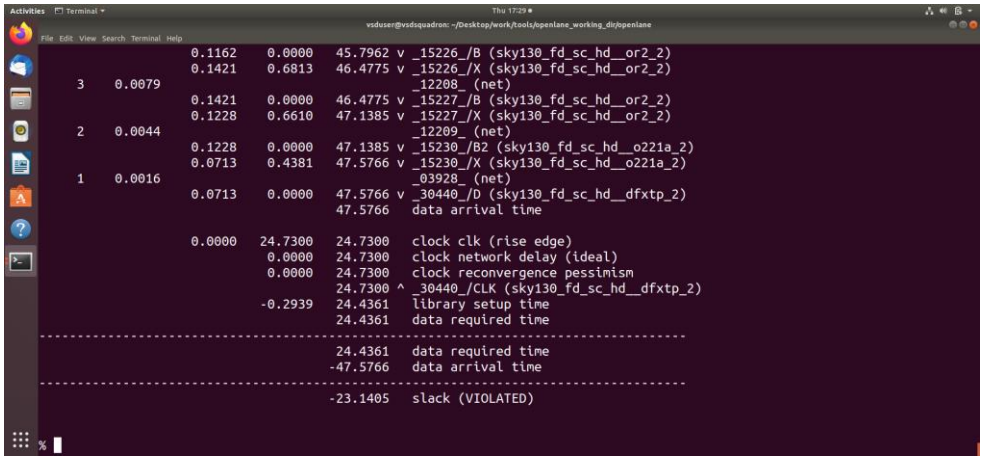
Use the following commends to optimize timing value. It will few iteration process for better fit of timing value.

- ➢ report_net -connections _11672_
- ➢ help replace_cell
- ➢ replace_cell _14510_ sky130_fd_sc_hd__or3_4
- ➢ report_checks -fields {net cap slew input_pins} -digits 4

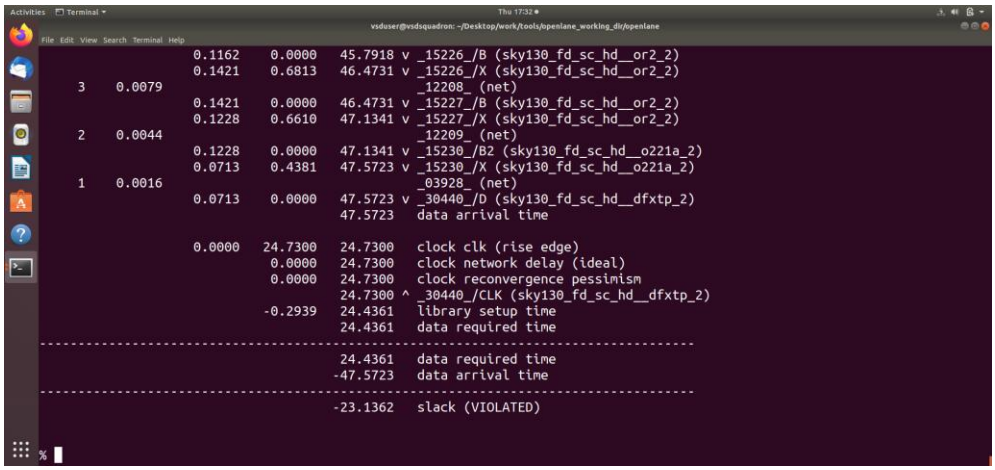


- ➢ report_net -connections _11675_
- ➢ replace_cell _14514_ sky130_fd_sc_hd__or3_4
- ➢ report_checks -fields {net cap slew input_pins} -digits 4

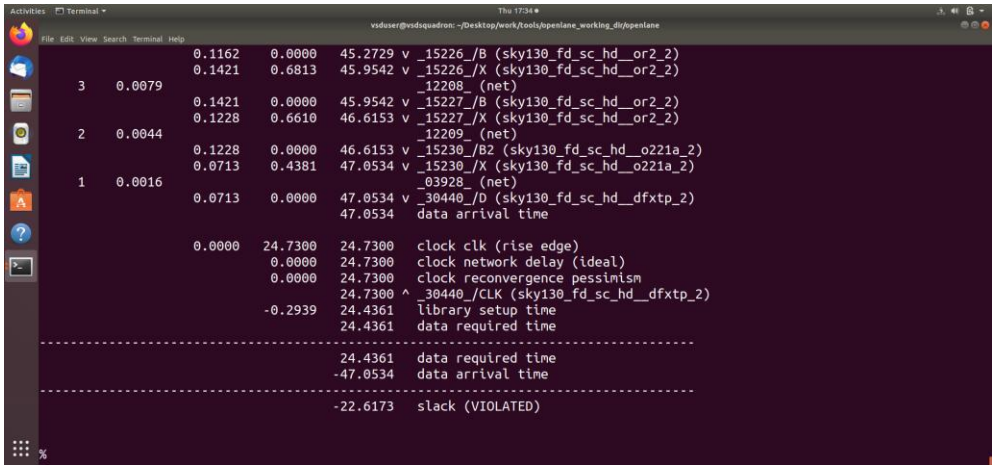




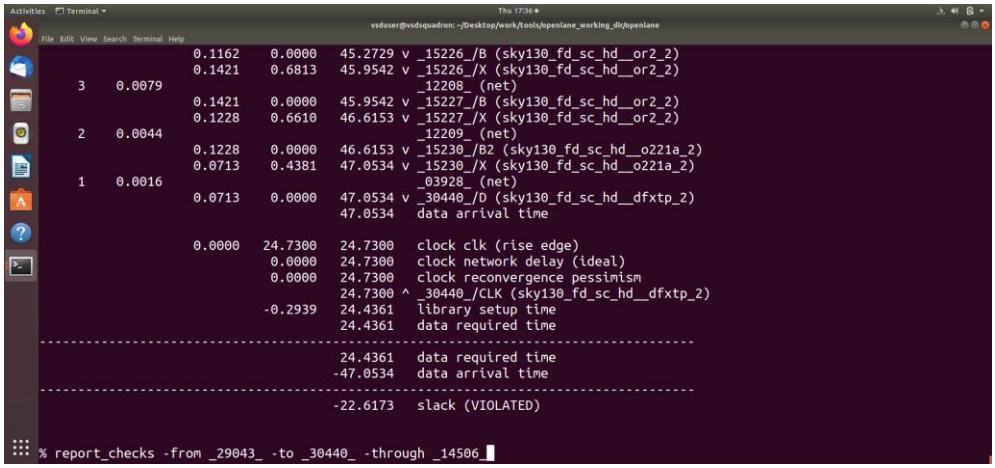
- report_net -connections _11643_
- replace_cell _14481_ sky130_fd_sc_hd__or4_4
- report_checks -fields {net cap slew input_pins} -digits 4

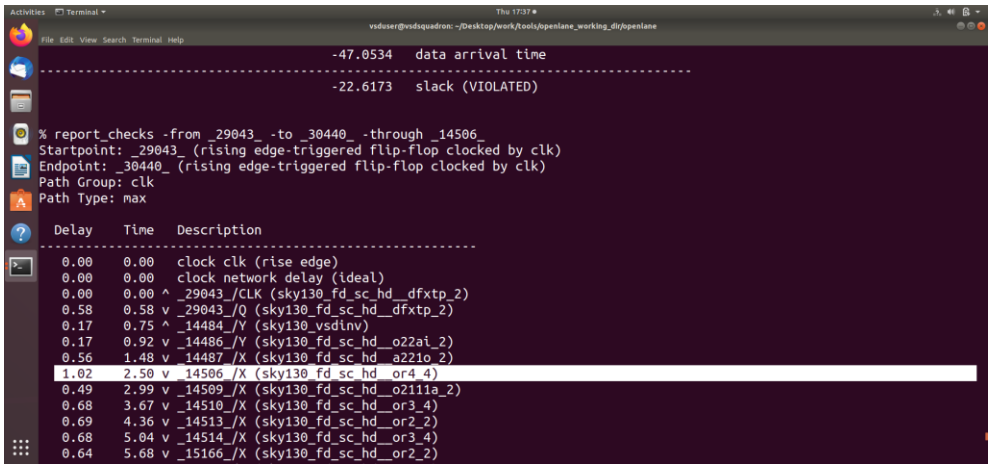


- report_net -connections _11668_
- replace_cell _14506_ sky130_fd_sc_hd__or4_4
- report_checks -fields {net cap slew input_pins} -digits 4



- report_checks -from _29043_ -to _30440_ -through _14506_





- New netlist generated after timing ECO

- Cd Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/09-05_16_40/results/synthesis/

- cp picorv32a.synthesis.v picorv32a.synthesis_old.v

Session 5 - Final steps for RTL2GDS using TritonRoute and openSTA
[24 April – 7 May, 2024]

This last session is mainly focusing on RTL to GDSII file with proper triton route and OpenSTA approach. This session starts with Routing and Design Rule Check (DRC) by using Maze routing – Lee's algorithm.

The following image shows the concept of Lee algorithm, which is used in the maze routing and follow by the DRC approach.

The following commends helps for CTS using TritonRoute and openSTA

Replace the new file with old .v file using write_verilog

- run_floorplan
- run_placement
- run_cts
- read_lef /openLANE_flow/designs/picorv32a/runs/04-05_21-50/tmp/merged.lef
- read_def /openLANE_flow/designs/picorv32a/runs/04-05_21-50/results/cts/picorv32a.cts.def
- write_db pico_cts.db
- read_db pico_cts.db
- read_verilog /openLANE_flow/designs/picorv32a/runs/04-05_21-50/results/synthesis/picorv32a.synthesis_cts.v
- read_liberty $::env(LIB_SYNTH_COMPLETE)

- read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc
- set_propagated_clock [all_clocks]
- report_checks -path_delay min_max -format full_clock_expanded -digits 4
- set ::env(CTS_CLK_BUFFER_LIST) [lreplace $::env(CTS_CLK_BUFFER_LIST) 0 0]
- echo $::env(CTS_CLK_BUFFER_LIST)
- echo $::env(CURRENT_DEF)
- run_cts

After the above stages, it is necessary to generate power distributed network using gen_pdn and also use routing with run_routing. The final results will be notified in magic tool – layout design.