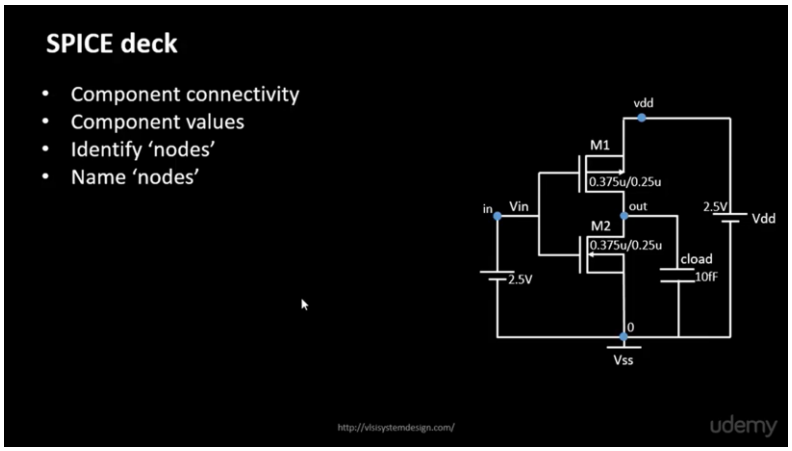
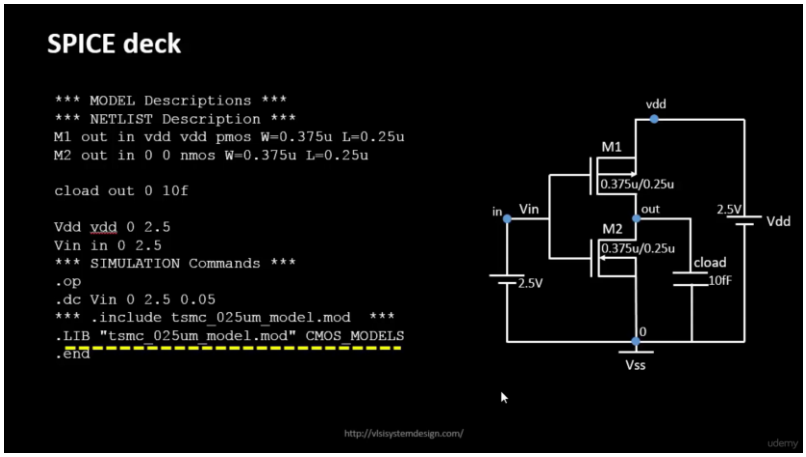
Day 3 - Sky130 Day 3 - Design library cell using Magic Layout and ngspice characterization [24 April – 7 May, 2024]

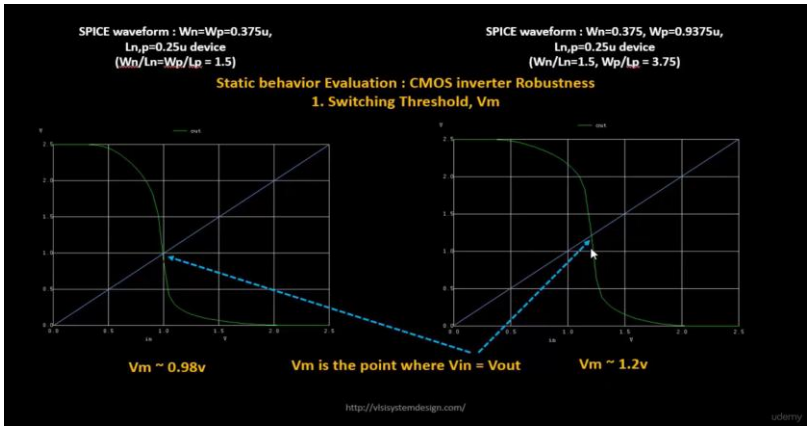
This session gives the fundamental concept of CMOS inverter in ngspice simulations. SPICE based CMOS inverter is proposed with the details of component connectivity, values, Identifying nodes and naming the nodes.



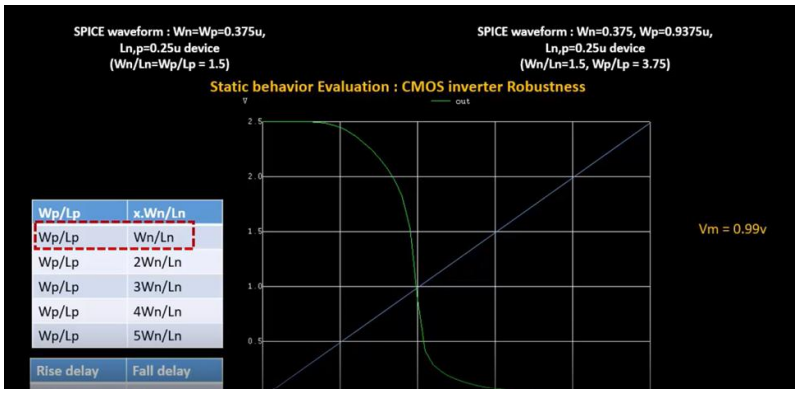
A typical spice model for CMOS inventor is given below with W=0.375 micron and L=0.25 micron and tragets to TSMC lib file.



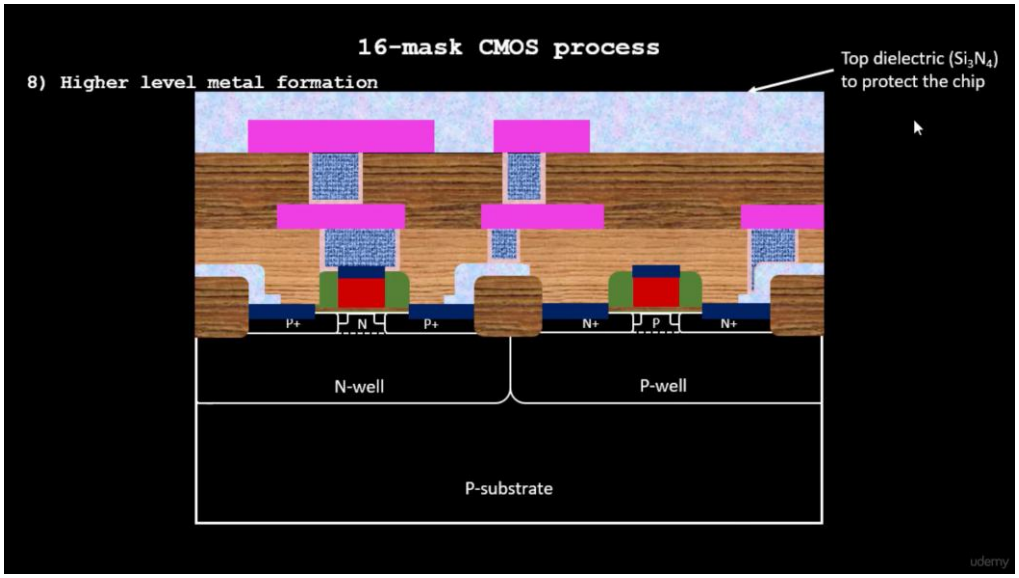
The below diagram show two differen Width and Length dimesions and its corresponding Vm values.



Static behaviour of CMOS inverter is shown with its various Wp/Lp and Wn/Ln



A 16-mask CMOS Process have the following stages. They are selecting a substrate, creating active region, N-well and P-well formulation, gate formulation, Lightly doped drain (LDD), Source and drain formulation, Interconnets, and metal formulation.



LAB:

This session contains 6 steps known as,

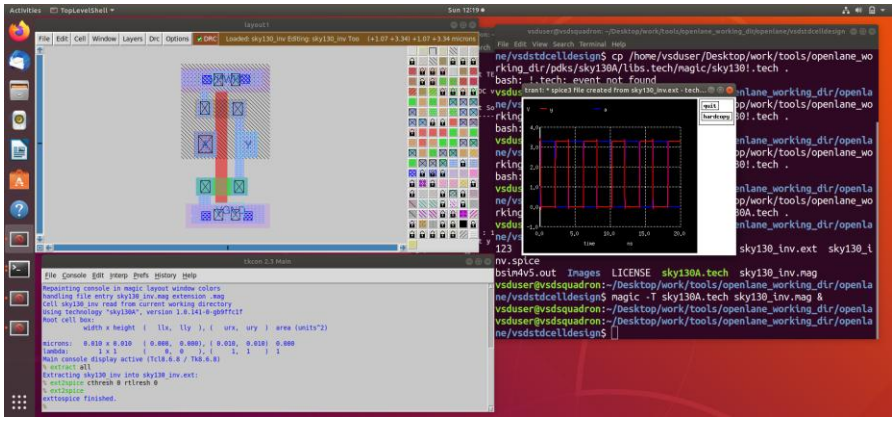
- From github (vsdstdcelldesign), clone the custom inverter standard cell
- Using magic tool, custom the inverter layout
- Extract inverter – spice model
- Edit the spice model for simulation purpose
- Using ngspice simulation – post layout module
- Fix the problem occurred in old magic DRC files

- cd Desktop/work/tools/openlane_working_dir/openlane
- git clone https://github.com/nickson-jose/vsdstdcelldesign
- cd vsdstdcelldesign

- cp /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic/sky130A.tech

.

- magic -T sky130A.tech sky130_inv.mag &
- In the magic tool – tkcon, check pwd, then
- extract all
- ext2spice cthresh 0 rthresh 0
- ext2spice
- Edit the available spice file for ngspice simulation
- Use Command line - ngspice sky130_inv.spice
- plot y vs time a



- Rise transition time:

Time taken for output to rise to 80% - Time taken for output to rise to 20%
20% of output = 660mV
80% of output = 2.64V

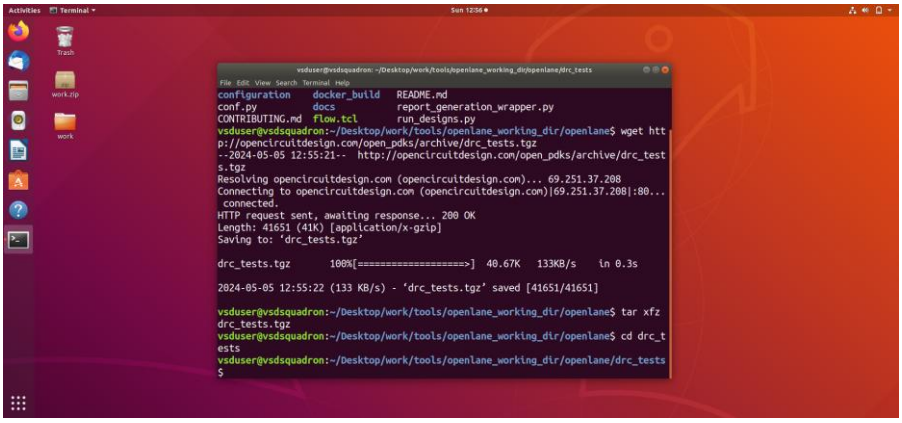
- Fall transition time:

Time taken for output to fall to 20% - Time taken for output to fall to 80%
20% of output = 660mV
80% of output = 2.64V

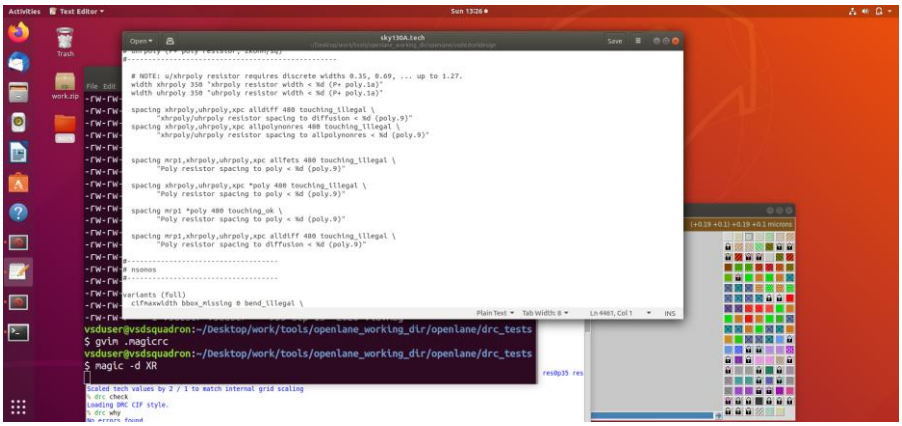
- Rise cell delay and Fall cell delay

Time taken for output to rise / fall to 50% -
Time taken for input to fall/rise to 50%
50% of 3.3V = 1.65 V

- Command to download lab files
  Wget http://opencircuitdesign.com/open_pdks_archive/drc_tests.tgz
- Tar xfz drc_tests.tgz



- cd drc_tests
- ls –al
- gvim –magicrc
- magic –d XR &
- Due to incorrect poly.9 rule – update sky130A.tech file



- In magic tkcon window,
  tech load sky130A.tech
  drc check
  drc why
- Due to incorrect difftap.2 – update sky130A.tech file
- In magic tkcon window,
  tech load sky130A.tech
  drc check
  drc why
- Due to incorrect nwell.4 – update sky130A.tech
- In magic tkcon window,

tech load sky130A.tech
drc style drc (full)
drc check
drc why