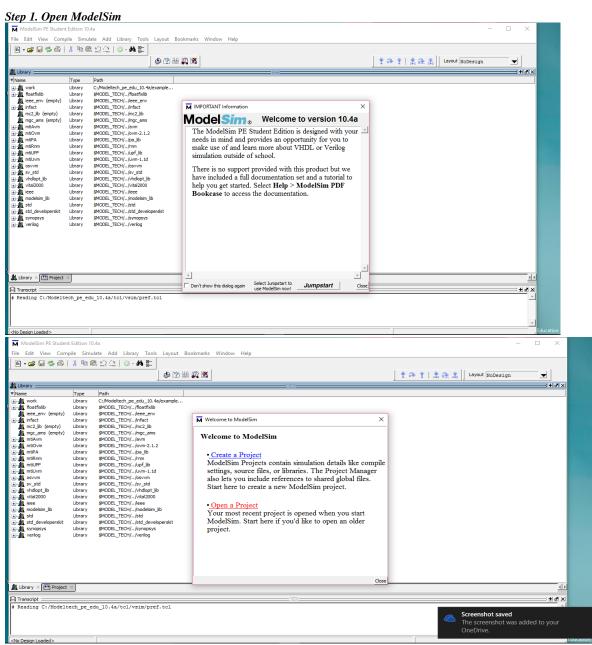
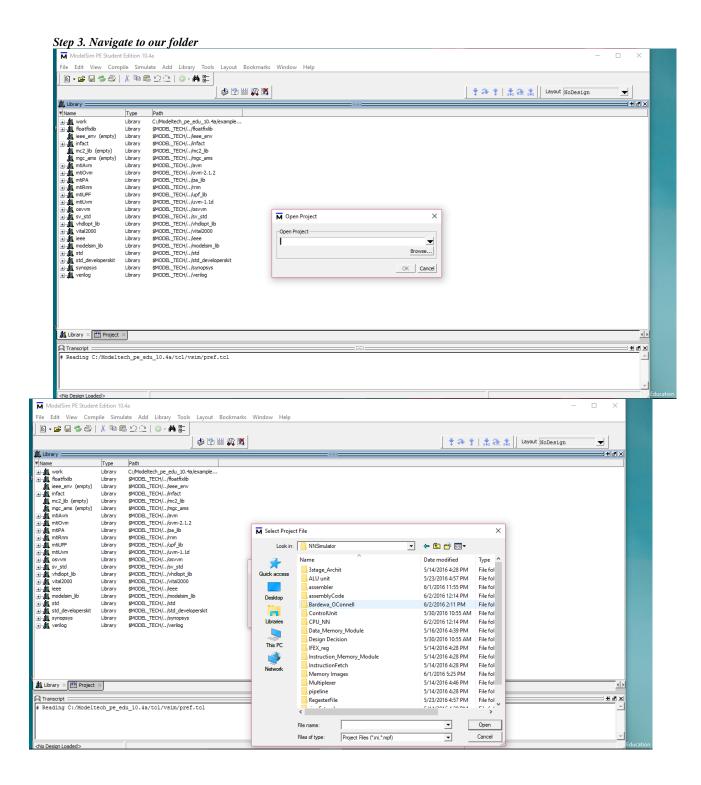
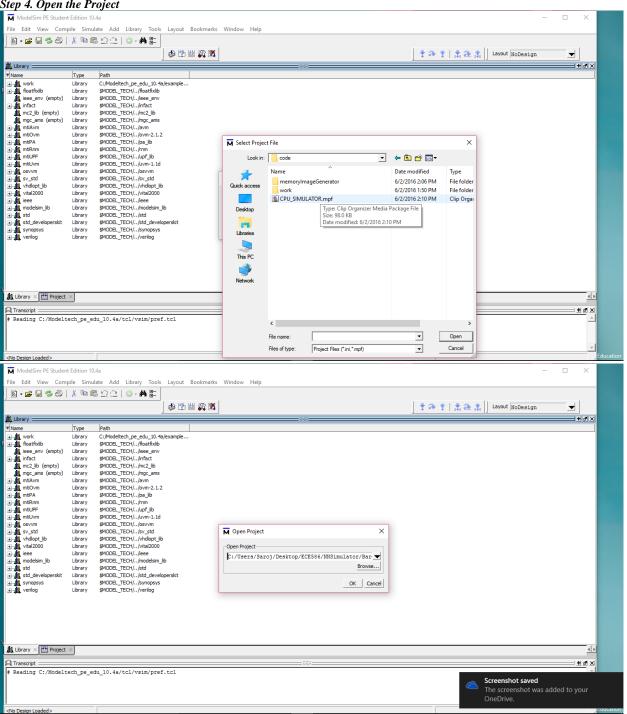
## How to run our project in ModelSim



Step 2. Click on "Open a project"



Step 4. Open the Project



Step 5. Compile the Project ModelSim PE Student Edition 10.4a File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help Compile...
Compile Options... | O - M == **⋄≇⊞**Д**≅** tayout NoDesign mulator/Bardewa\_OConnell/code/CPU\_SIMULATOR Project - C:/User: Compile All | Name | Compile All | Modified | Modified | Group's General | Gro ⚠ Library × 🛗 Project × # # X Transcript = # Reading C:/Modeltech\_pe\_edu\_10.4a/tcl/vsim/pref.tcl
project open C:/Users/Saroj/Desktop/ECE586/NNSimulator/Bardewa\_OConnell/code/CFU\_SIMULATOR.mpf
# Loading project CFU\_SIMULATOR Project : CPU SIMULATOR <No Design Loaded> ModelSim PE Student Edition 10.4a X File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help Start Simulation... Runtime Options... Layout NoDesign 🦠 🕮 🕮 👰 🌋 Project - C:/Users/Saroj/Desk wa\_OConnell/code/CPU\_SIMULATOR = + # × Sten ame regfile.v
cpu.v
IDIE\_Reg.v
BitFieldExtender.v
instructMemory.v
cputest.v
controlUnit.v
multiplexer\_6bits.v
ALUI.v 6 07:25:38 ... 6 07:15:24 ... 6 07:15:24 ... 6 07:15:25 ... 05/30/2016 10:37:47 ... 06/01/2016 07:48:34 ... 06/01/2016 07:18:17 ... 06/01/2016 05:16:30 ... 06/01/2016 07:23:201 ALU1.v
dataMemory.v
multiplexer.v
ALU2.v Library × Project × Transcript = # Compile of multiplexer\_6bits.v was successful. # Compile of regfile.v was successful. # 12 compiles, 0 failed with no errors.

Step 6. Simulate the program

Step 7. Click on cpuTest to simulate it File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help **B** • **≥ G** • **4 5 4 5 1 X 9 8 2 2 2 1 0** • **M E ◆郵曲線**■ | † 💸 🛊 🕍 🚉 | Layout NoDesign Project - C:/Users/Saroj/Desktop/ECE586/NNSimulator/Bardewa\_OConnell/code/CPU\_SIMULATOR Sta △ Type Order Modified | Stao | Type | Orde| Modified | Verling | 11 | 06/01/2016 07:25:38 ... | Verling | 1 | 06/01/2016 07:25:38 ... | Verling | 7 | 06/01/2016 07:25:34 ... | Verling | 7 | 06/01/2016 07:35:54 ... | Verling | 8 | 06/01/2016 07:35:54 ... | Verling | 8 | 06/01/2016 07:35:47 ... | Verling | 8 | 06/01/2016 07:48:17 ... | Verling | 3 | 06/01/2016 07:18:17 ... | Verling | 3 | 06/01/2016 07:23:01 ... | Verling | 0 regfile.v

cpu.v

DIE\_Reg.v

BitFieldextender.v

instructMemory.v

controllnit.v

ALU1.v

dataMemory.v

dataMemory.v

multiplexer\_6bits.v multiplexer.v ALU2.v M Start Simulation Design VHDL Verilog Libraries SDF Others **∢** ≽ work Library Module Module work

ALU1

ALU2

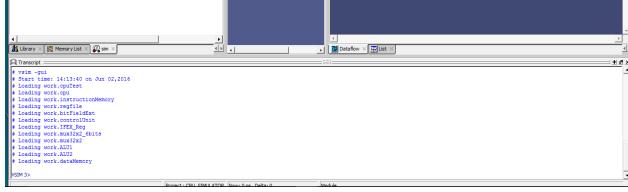
DitFieldExt

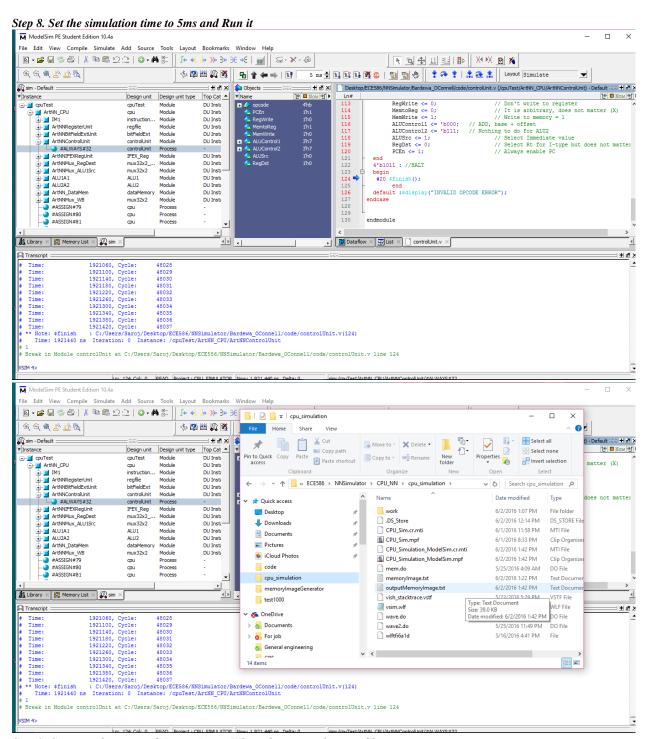
ControlUnit

Copu

DitFex Reg

MinstructionNe work
C:/Users/Saroj/Desktop/ECE586/NNSi. C:/Users/Saroj/Desktop/ECE586/NNSi... C:/Users/Saroj/Desktop/ECE586/NNSi... Module Module C:/Users/Saroi/Desktop/ECE586/NNSi... C:/Users/Saroj/Desktop/ECE586/NNSi... C:/Users/Saroj/Desktop/ECE586/NNSi... C:/Users/Saroj/Desktop/ECE586/NNSi... C:/Users/Saroj/Desktop/ECE586/NNSi... C:/Users/Saroj/Desktop/ECE586/NNSi... C:/Users/Saroj/Desktop/ECE586/NNSi... ⚠ Library × 🕮 Project × work.cpuTest default. Transcript === # # X OK Cancel # Compile of regfile.v was successia. # 12 compiles, 0 failed with no errors. Project : CPU\_SIMULATOR | <No Design Loaded > ModelSim PE Student Edition 10.4a **我只佩斯拉克** ▼ sim - Default \_\_\_\_\_ # # X Dijects # # X Run taflow - Default : | Design unit | Design unit type | Top Catego | V|Name | Unit type | Top Catego | V|Name | Unit tance | Unit Te Now → A cpu cpuTest cpuTest cpuTest Process Process Process Capacity Welcome to the Enhanced Dataflow Window NOTE: Extended dataflow mode active





Step 9. Compare the outputofMemoryImageFile to the expected output file