

1DT301 lab1

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September 8, 2016

1 Introduction

This report provides the solutions for the first laboratory of the course 1DT301.

2 Task 1

Hereby, code for the first task is presented, which to light LED 2

[illegible]

In order to light LED light, the minimum lines of code are four. First line should store 0b11111111 into register, second should load that value into data direction register of the desired port. The fourth line should load into the register the desired output value, and the last line should put the desired value into the port so that LED lights on. In such case, the flowchart would look as following:

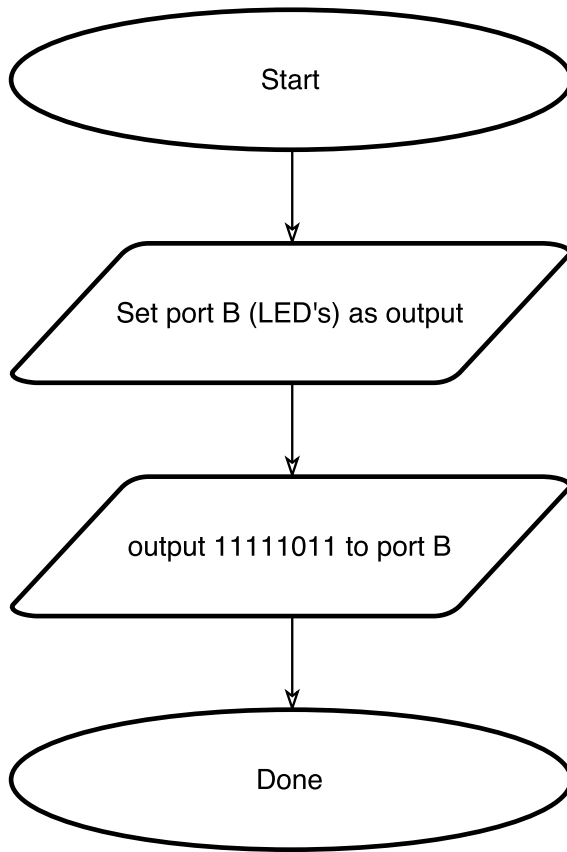


Figure 1: Flowchart of task 1

3 Task 2

Code and a flowchart for the second task is presented.

[illegible]

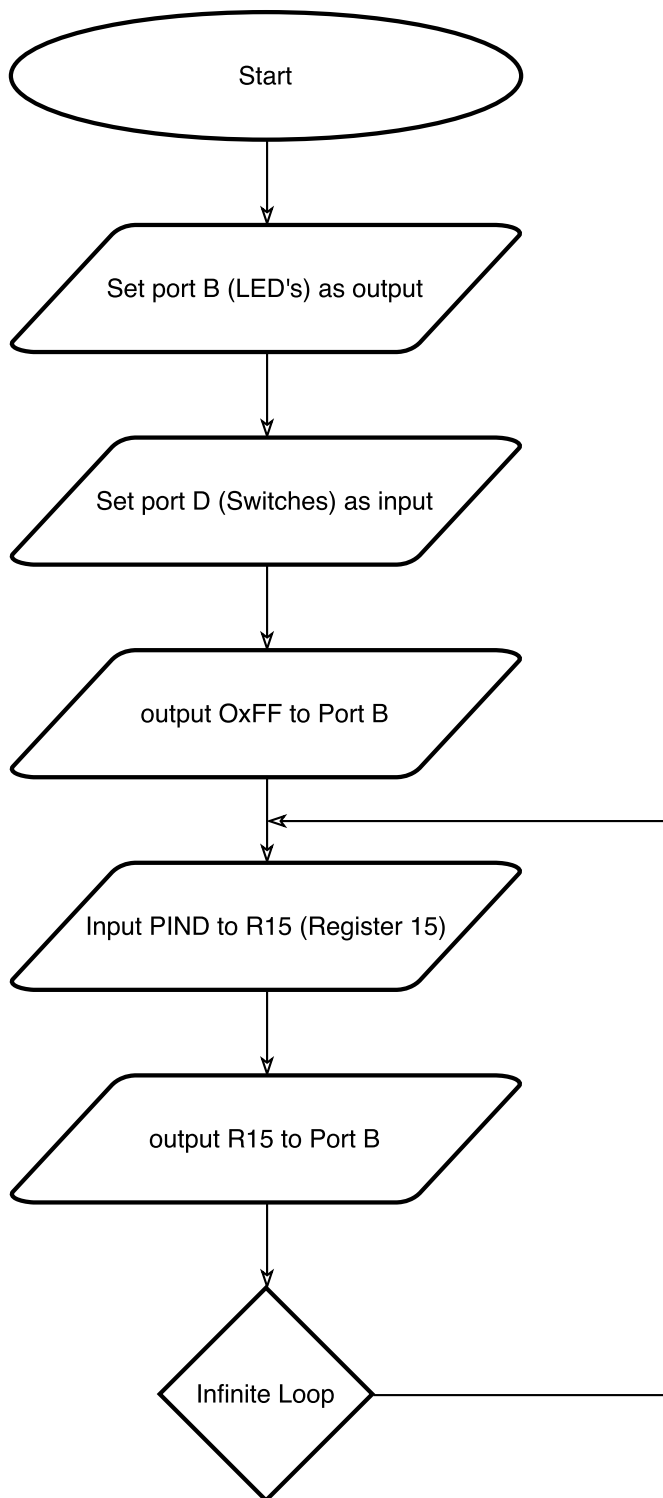


Figure 2: Flowchart of task 2

4 Task 3

Code and a flowchart for the third task is presented.

[illegible]

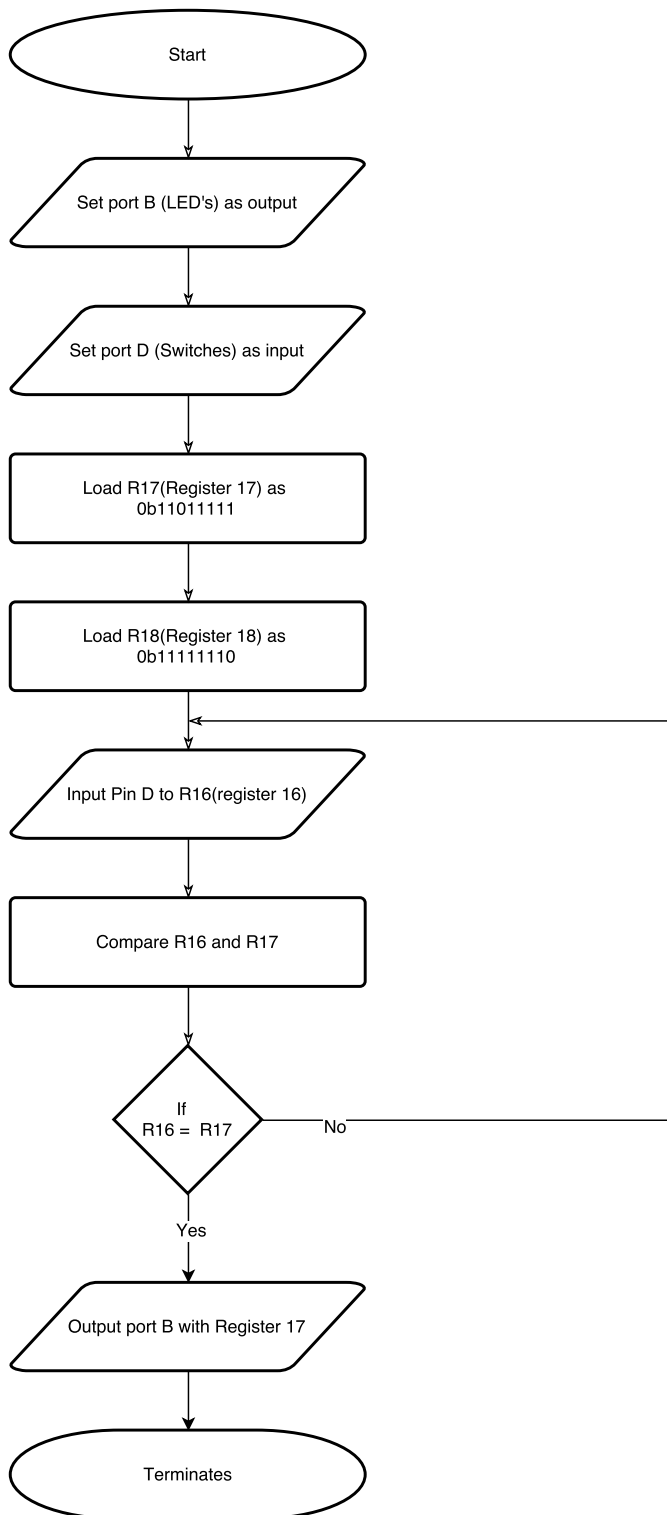


Figure 3: Flowchart of task 3

5 Task 5

Code and a flowchart for the fifth task is presented. In order for our code to have interval of 0.5 seconds, CPU clock needs to be configured with 4MHz. On the debugging simulator it returned with 538073.00 micro seconds.

[illegible]

```

        inc r24
        cp r18, r24
        brge innerdelay1

60      inc r19
        cp r18, r19
        brge outerdelay

        inc r23
65      cp r18, r23
        brge superdelay

        cp r17, r25
        breq equal
70      rjmp firstloop
equal: ldi r17, 0b00000001

```

Since delay part of the task five requires complicated control sequences, hereby we divide the chart into two parts: part before the delay, and after the delay.

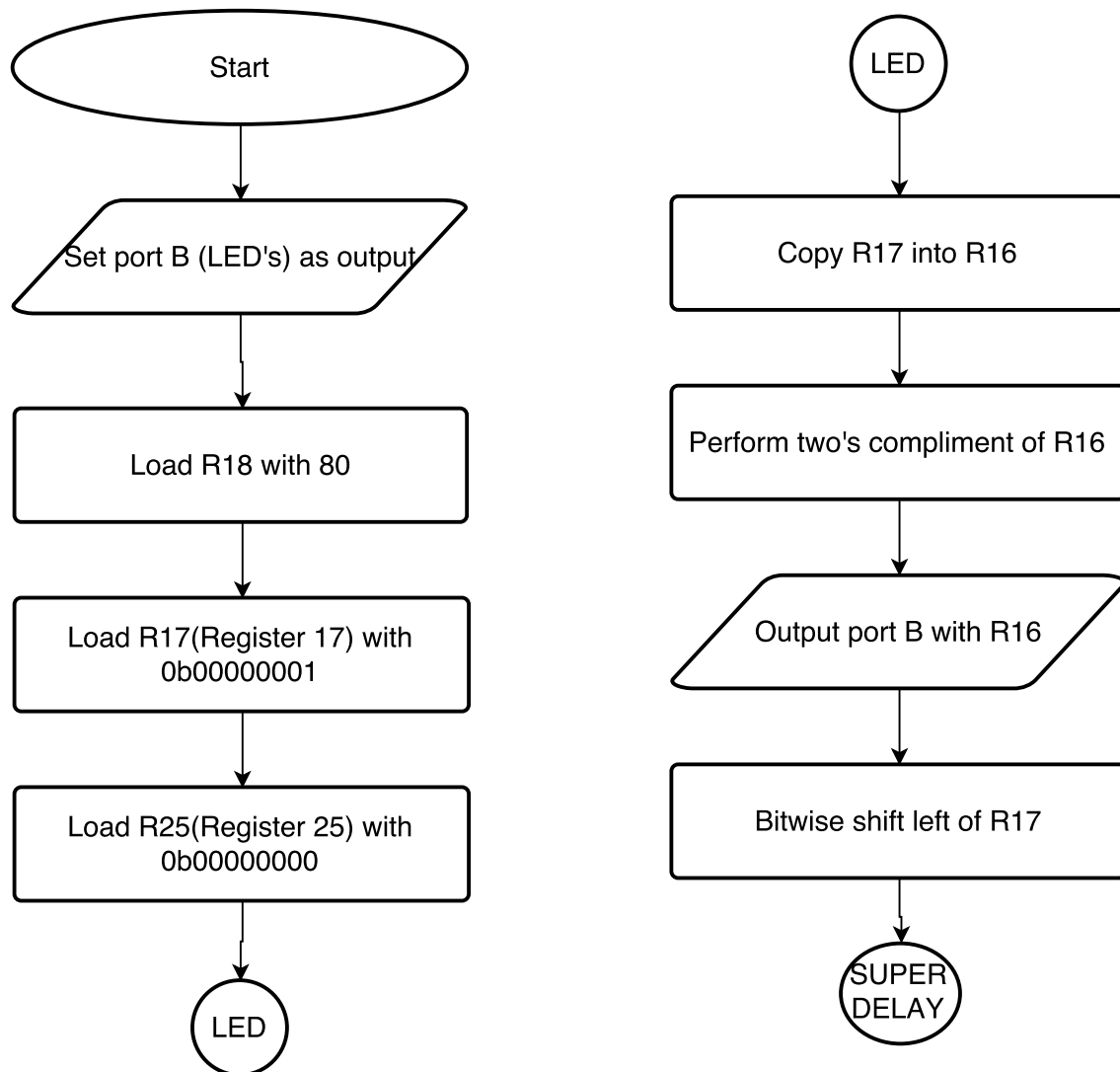


Figure 4: Flowchart of task 5 part 1

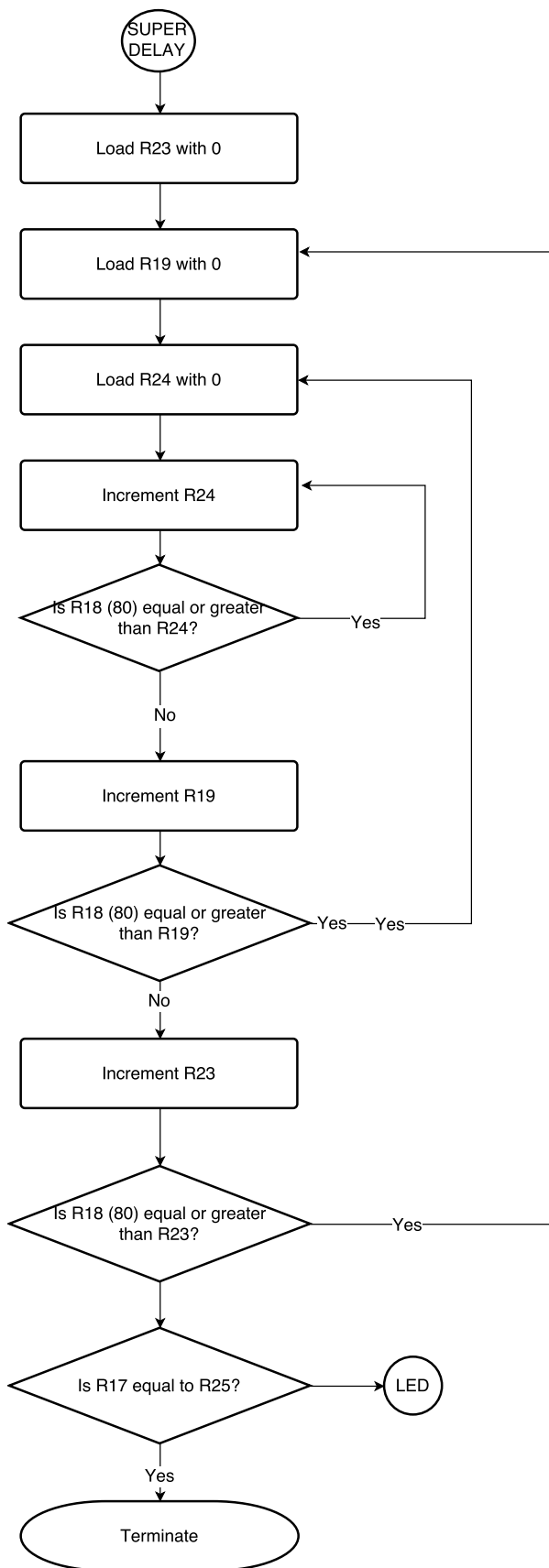


Figure 5: Flowchart of task 5 part 2

6 Task 6

Code and a flowchart for the sixth task is presented. In order for our code to have interval of 0.5 seconds, CPU clock needs to be configured with 4MHz. On the debugging simulator it returned with 538073.00 micro seconds.

[illegible]

```

ldi r18, 80;    r18 to be our N
ldi r23, 0;      r23 to be our k counter, 0
superdelay1:
    ldi r19, 0;    r19 to be our i, which is 0
60    outerdelay1:
        ldi r24, 0;    r24 to be our j, which is 0

        innerdelay1:
65        inc r24
            cp r18, r24
            brge innerdelay1

            inc r19
            cp r18, r19
70        brge outerdelay1

            inc r23
            cp r18, r23
            brge superdelay1
75
;;DELAY ENDS

;These operations for the LED
mov r16, r17
80 com r16
    out portB, r16

    cpi r22, 0xFF
    breq shiftright

85 ;COMPARISION
    shiftright:

    LSL r17
90 add r17, r21

    cpi r22, 0xFF
    brne begincompare

95 shiftright:
    LSR r17

    begincompare:
    cp r17, r25
100 breq equal

    rjmp firstloop

    equal:
105 com r25
    com r22

    rjmp mainloop

```

Since delay part of the task six requires complicated control sequences, hereby we divide the chart into three parts.

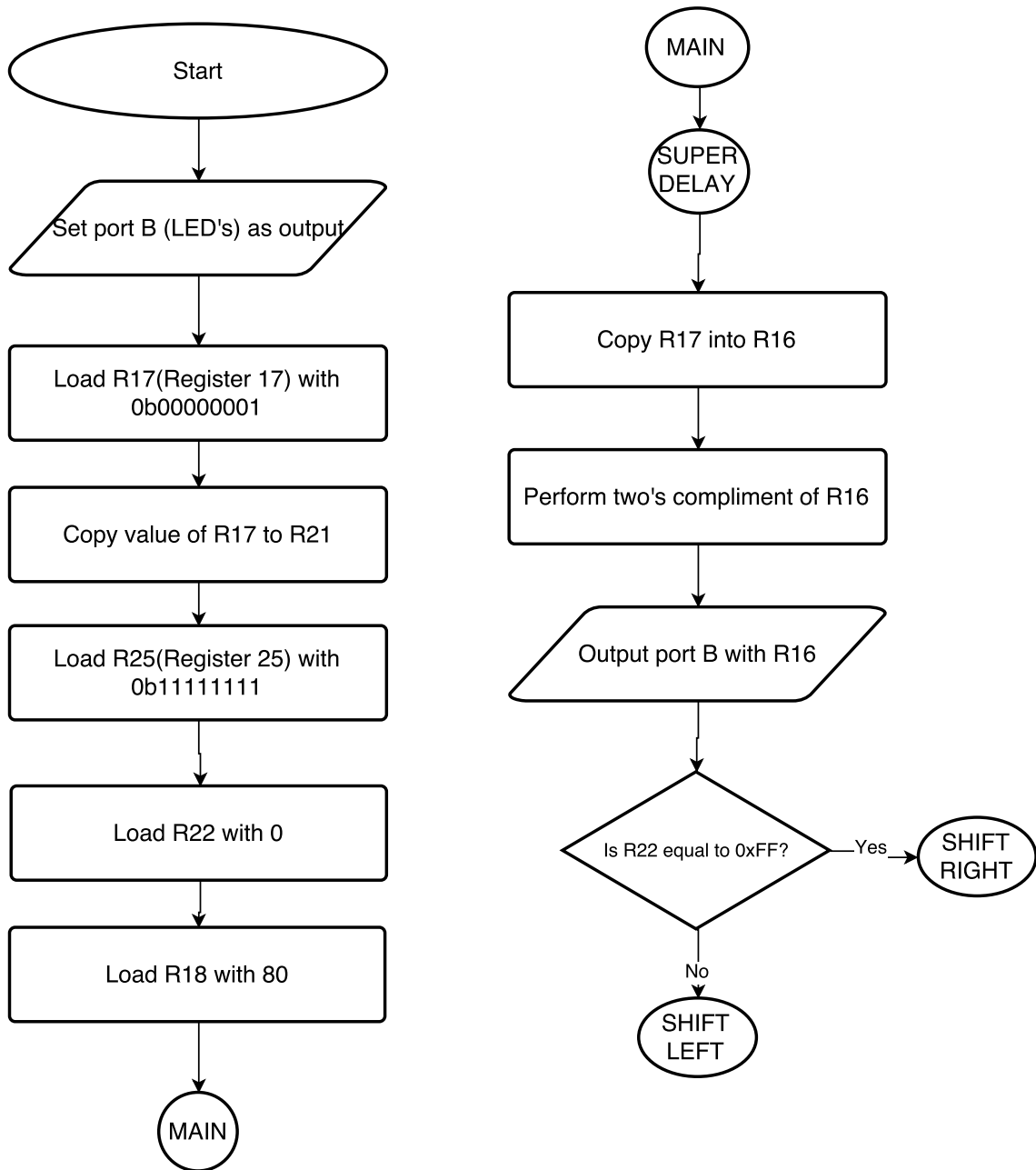


Figure 6: Flowchart of task 6 part 1

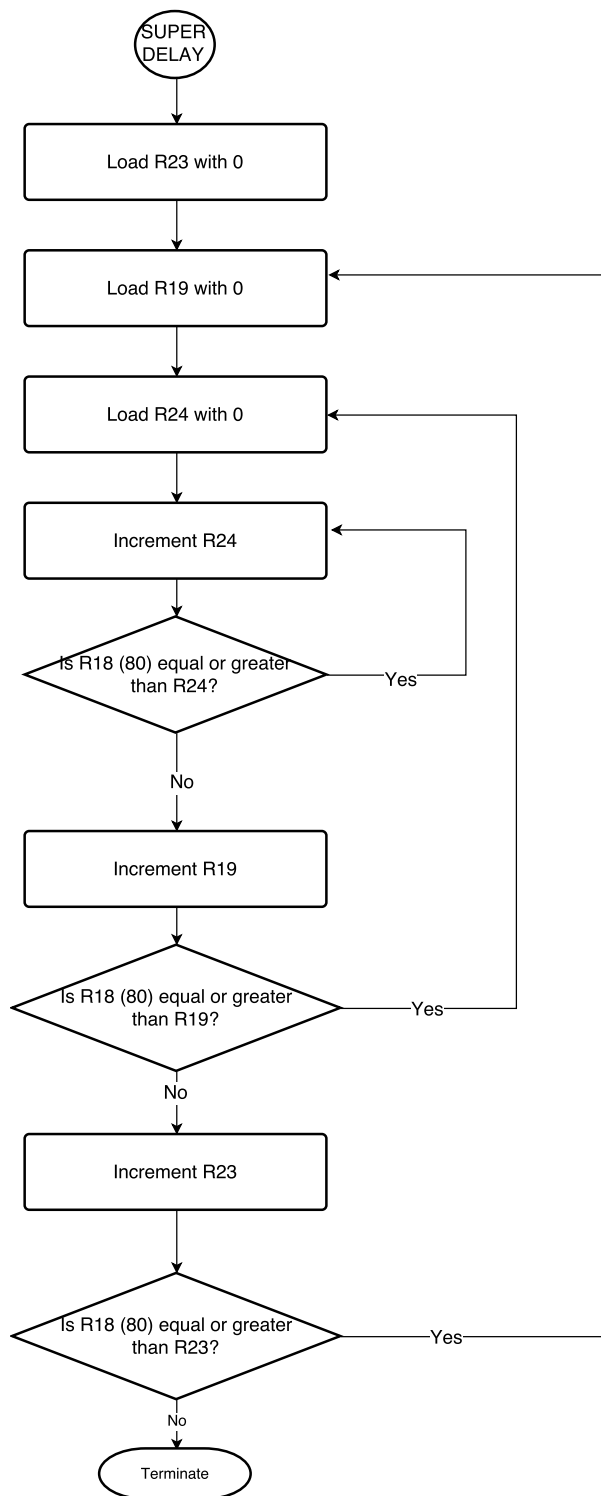


Figure 7: Flowchart of task 6 part 2

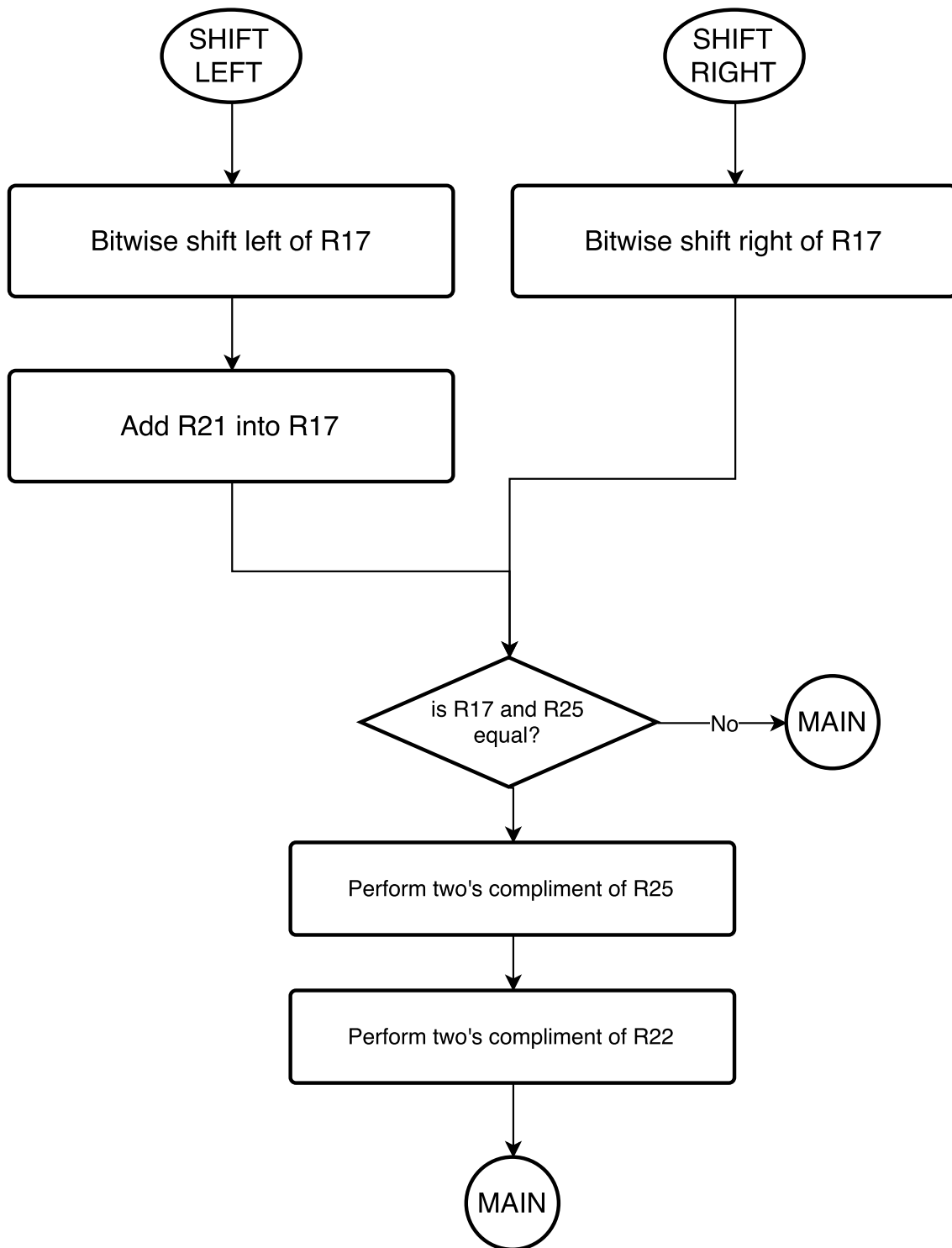


Figure 8: Flowchart of task 6 part 3