

1DT301 lab2

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1 Introduction

This report provides the solutions for the second laboratory of the course 1DT301.

2 Task 1

Task 1 asks to write a programme which switches counter when SW0 is pressed. Code for the programme and corresponding diagram is presented below, but we will not present detailed mechanism for Johnson counter and ring counter on the diagram since it has already covered in the previous report.

[illegible]

```

out DDRB, r16 ;Set B port as output ports

40 ldi r16, 0x00 ;Set data direction registers.
out DDRD, r16 ;Set D port as input ports

;LED have 0 as on, 1 as off which is opposite to normal lamps
;Hereby we command second position of the LED to be on.
45 .def N = R18
.def K = R19

50 ldi r17, 0b00000001
mov r21, r17 ;Registering 00000001 on both register 17, and 21.
ldi r25, 0b11111111
ldi r22, 0
.def DIRECTIONFLAG = R22
55 ldi r23, 0
.def COUNTERFLAG = R23

mainloop:
60 firstloop:

rcall overallldelay

65 ;Listening on the switch
in r16, PIND
ldi r26, 0b11111110
cp r26, r16

70 brne noreact
react:
com COUNTERFLAG
ldi R17, 0b00000001

75 noreact:
;Listening done

;COMPLEMMENT FOR LED
80 mov r16, r17
com r16
out portB, r16
;LED OPERATION DONE

85 cpi COUNTERFLAG, 0
brne johnson
ring:
LSL r17
cpi COUNTERFLAG, 0
90 breq johnsonend

johnson:

cpi DIRECTIONFLAG, 0xFF ;RIGHT
95 breq shiftright

;COMPARISION

```

```

shiftleft:
100 LSL r17
    add r17, r21

    cpi DIRECTIONFLAG,0xFF
    brne begincompare
105
shiftright:
    LSR r17

begincompare:
110 cp r17, r25
    breq equal

johnsonend:

115
    cpi COUNTERFLAG,0
    brne ringendconditiondone

    cpi r17, 0
120 brne ringendconditiondone
    ldi r17, 1

ringendconditiondone:

125 rjmp firstloop

equal:
    com r25
    com DIRECTIONFLAG
130
    rjmp mainloop

135 ;Now begin subroutines.

;;DELAY
overalldelay:
    push N
140 push K
    ldi N, 80;      r18 to be our N
    ldi K, 0;      r19 to be our counter for all steps
superdelay1:
    push K
145    ldi K, 0;
    outerdelay1:
    push K
    ldi K, 0;

150    innerdelay1:
    inc K
    cp N, K
    brge innerdelay1
    pop K

155    inc K
    cp N, K

```

```

    brge outerdelay1
    pop K

160
    inc K
    cp N, K
    brge superdelay1

165
    pop K
    pop N

    ret
;;DELAY ENDS

```

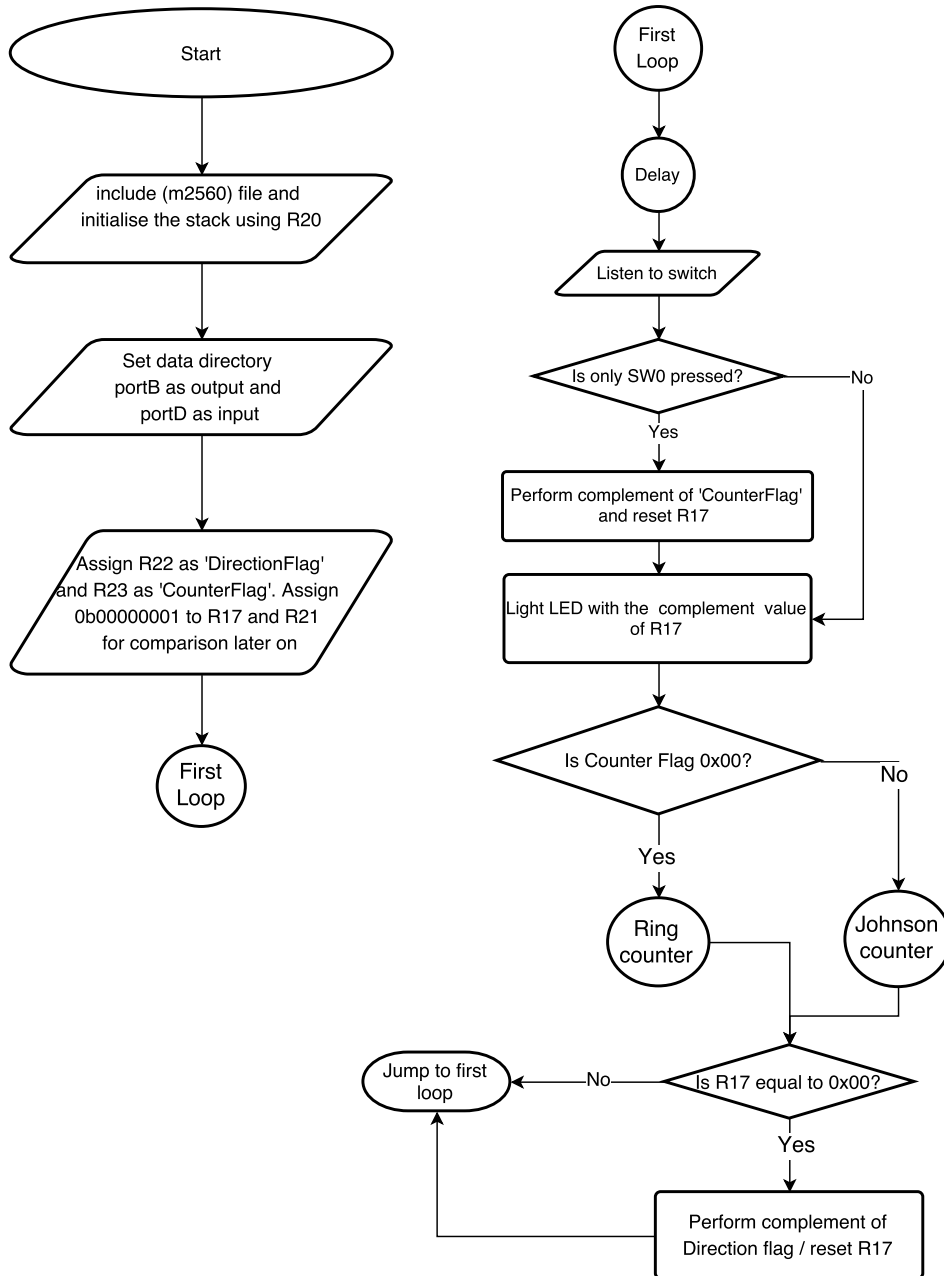


Figure 1: Flowchart of task 1

3 Task 2

Task two asks to create an electronic dice responding with random number. However, as current CPU - which is ATmega2560 - does not have a capability to create in terms of mathematics random number, hereby we listen on the length of switches that an arbitrary user presses. We assume length of listening should vary in scope of $2.5 * 10^{-7}s$ interval, which is due to our configuration of the current CPU to perform on 4MHz.

[illegible]

```

    cpi R18, 0xFF
    breq stoplistening
55 inc DICE

    cpi DICE, 7

    brne continue
60 ldi DICE, 1

    continue:

    rjmp listening
65

    stoplistening:
    cpi DICE, 1
    breq one
70 cpi DICE, 2
    breq two
    cpi DICE, 3
    breq three
    cpi DICE, 4
75 breq four
    cpi DICE, 5
    breq five
    cpi DICE, 6
    breq six
80

    one:
    ldi R16, 0b11101111
    out portB, R16
    rjmp mainloop
85

    two:
    ldi R16, 0b10111011
    out portB, R16
    rjmp mainloop
90

    three:
    ldi R16, 0b10101011
    out portB, R16
    rjmp mainloop

    four:
95 ldi R16, 0b00111001
    out portB, R16
    rjmp mainloop

    five:
    ldi R16, 0b00101001
100 out portB, R16
    rjmp mainloop

    six:
    ldi R16, 0b00010001
    out portB, R16
105 rjmp mainloop

```

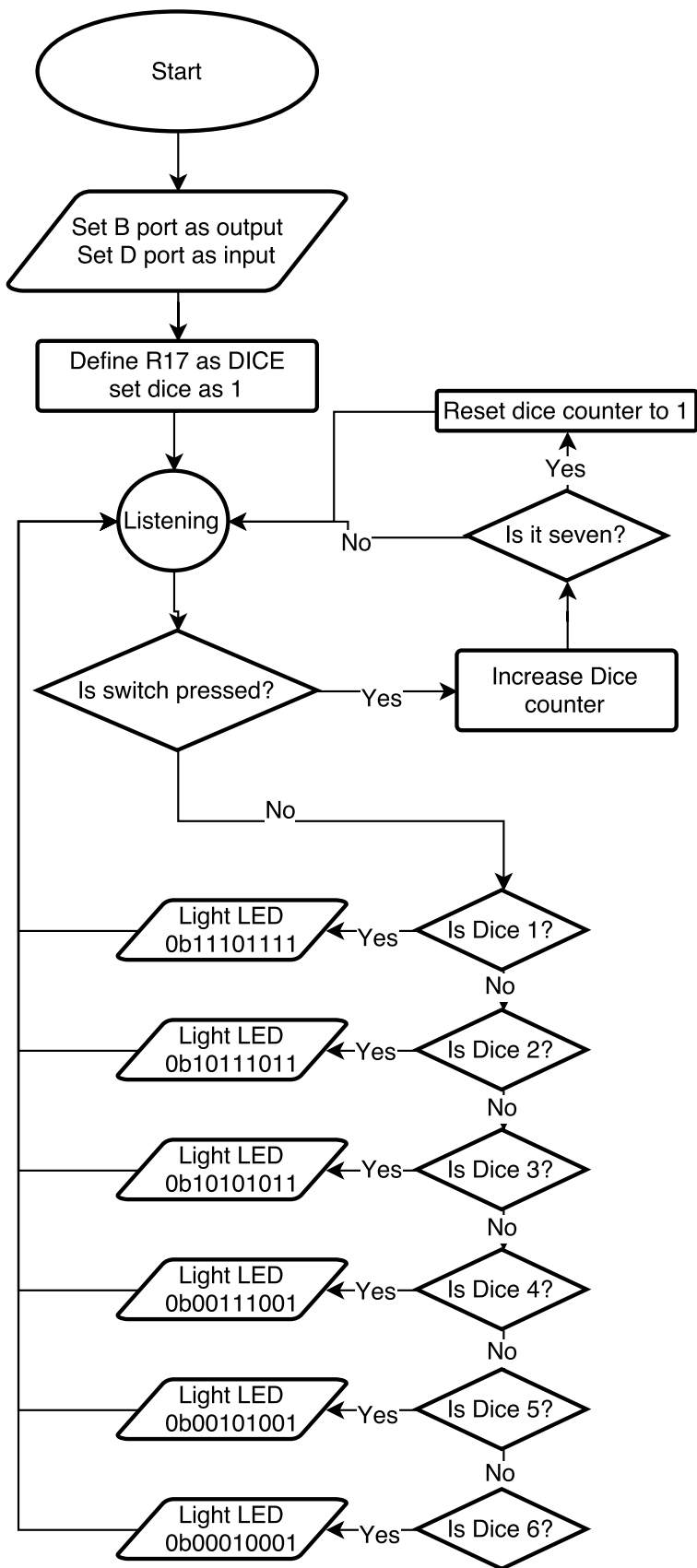


Figure 2: Flowchart of task 2

4 Task 3

The programme which listens on changes of SW0 and increases counter is presented below.

[illegible]


```

    cpi R18, 0b11111110
    brne continue

60    cpi R20,0
    brne continue

    rcall change
65    LDI R20, 0xFF

    continue:
    rjmp listening

70    stoplistening:
    cpi R20, 0xFF
    brne mainloop
    rcall change

75    rjmp mainloop

    change:
    inc COUNTER

80    MOV R19, COUNTER
    COM R19
    out portB, R19
    ret

```

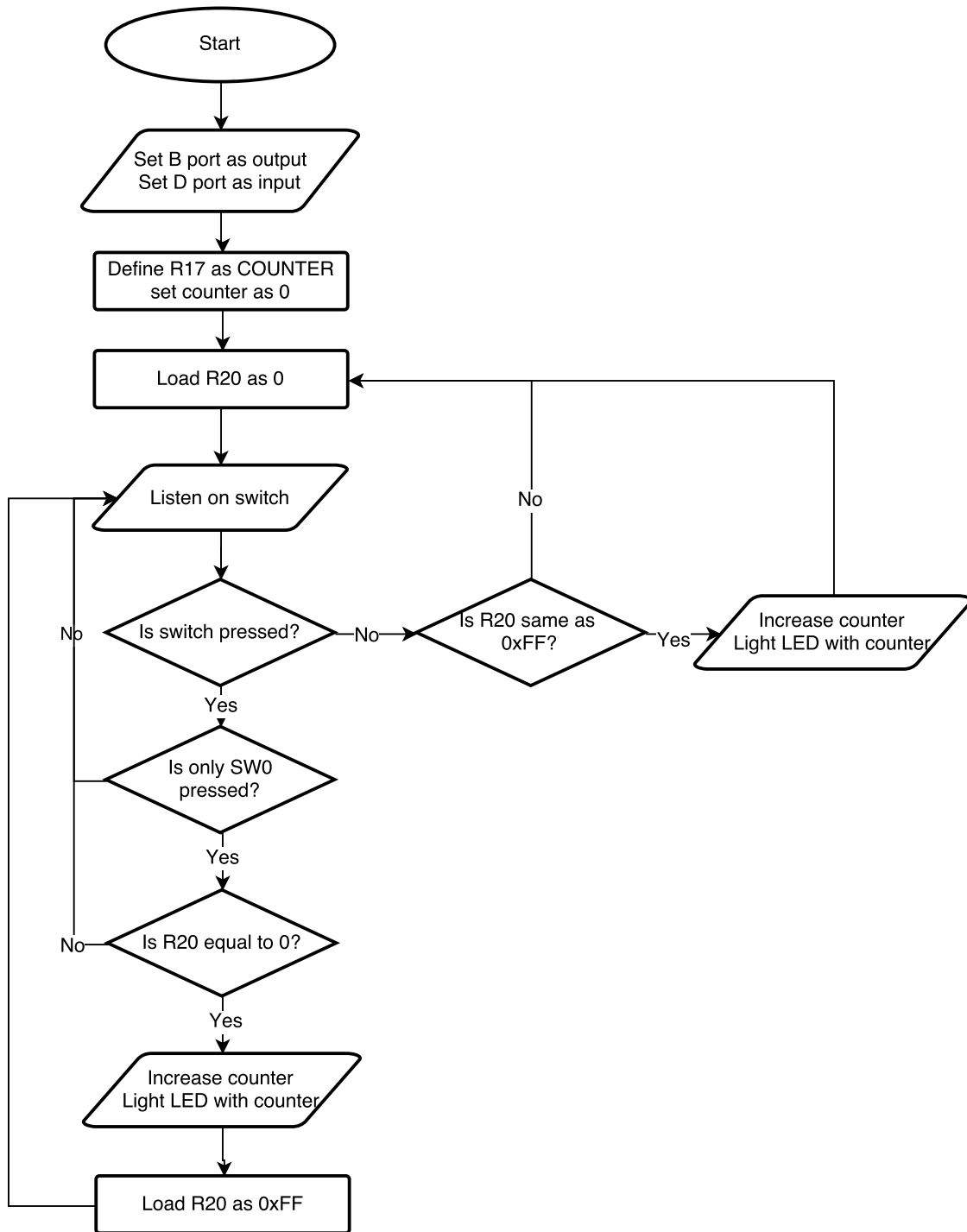


Figure 3: Flowchart of task 3

5 Task 4

Code and a flowchart for the fourth task is presented below. This programme would guarantee the timer only if it configured to run with 4MHz oscillation rate. As for diagram we have not mentioned detailed implementation of such as delay, which is already covered in the previous review about the mechanism behind the delay. The change of this task compared to the last one is that amount of repeating iteration has fine-tuned by introducing constant N, and M. Furthermore, the part in the diagram that we are comparing register pairs are done in two separate code in actually implementation, that is to compare the two later parts and two earlier parts of the register pair. However, in order to increase readability of the flow chart, hereby we decided to combine two decision making diagrams into one.

[illegible]

```

50 ;LED have 0 as on, 1 as off which is opposite to normal lamps
;Hereby we command second position of the LED to be on.

ldi r17,0b00000001
55 ldi R21,0b00000000
firstloop:

mov r16, r17
com r16
60 out portB, r16

LSL r17
rcall specificdelay

65 cp r17, R21
brne firstloop
ldi r17,0b00000001
rjmp firstloop

70 ;Now begin subroutines.

specificdelay:
ldi R26,0
75 ldi R27,0

loop:
rcall onemilliseconddelay

80 adiw R27:R26, 1

cp R24,R26
brne loop
cp R25,R27
85 brne loop
ret

rjmp loop

90 onemilliseconddelay:
push N
push K
ldi N, 8; r18 to be our N
ldi M, 9
95 ldi K, 0; r19 to be our counter for all steps
superdelay1:
push K
ldi K, 0;
outerdelay1:
100 push K
ldi K, 0;

innerdelay1:
inc K
105 cp N, K
brge innerdelay1
pop K

inc K

```

```
110      cp M, K
      brge outerdelay1
      pop K

      inc K
115      cp N, K
      brge superdelay1

      pop K
      pop N
120      ret
```

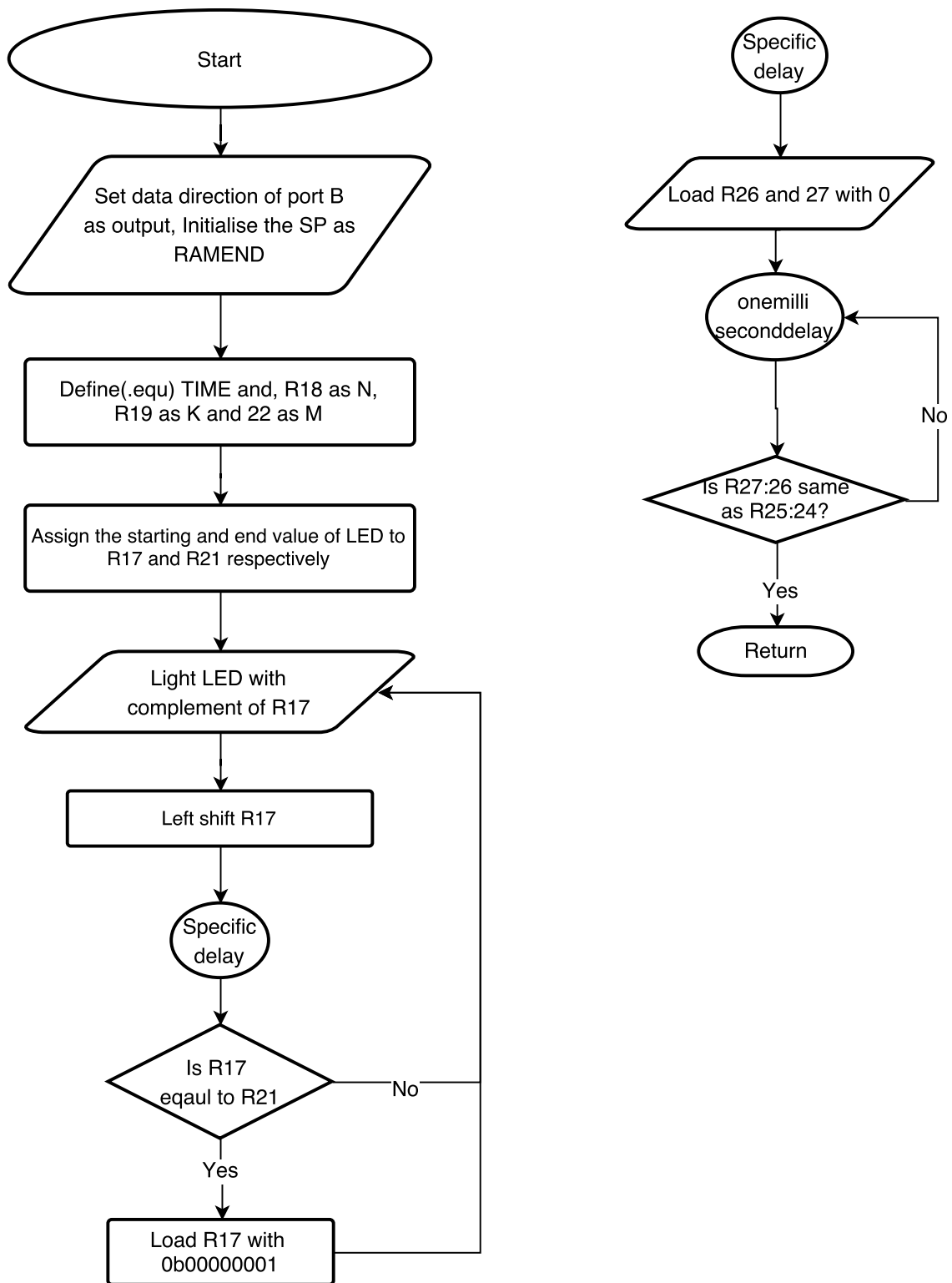


Figure 4: Flowchart of task 4