

# Single Channel Aggregation of Multiple Sensors Using Frequency Modulation and Frequency Division Multiplexing



## Team A

Alex (*Signal Processing, Team Lead*)

Hao (*Systems*)

Richard (*Software/Signals*)

Gerry (*Software/Signals*)

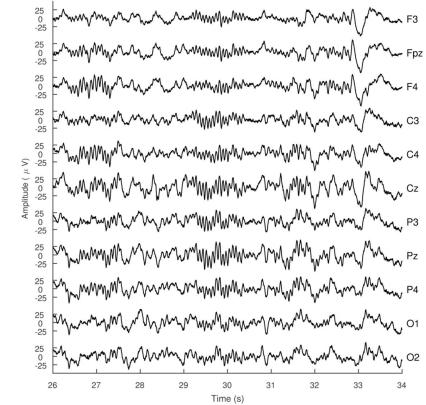
Sarp (*Hardware*)

## Advisors

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UC San Diego  
JACOBS SCHOOL OF ENGINEERING

# Problem Motivation

## Modern ExG Systems

- Lots of wires
- Physically bulky
- Motion artifacts
- Large power draw

**Takeaway:** Impractical for everything but stationary, on-site measurements

*How can we improve?*



# Proposed Solution

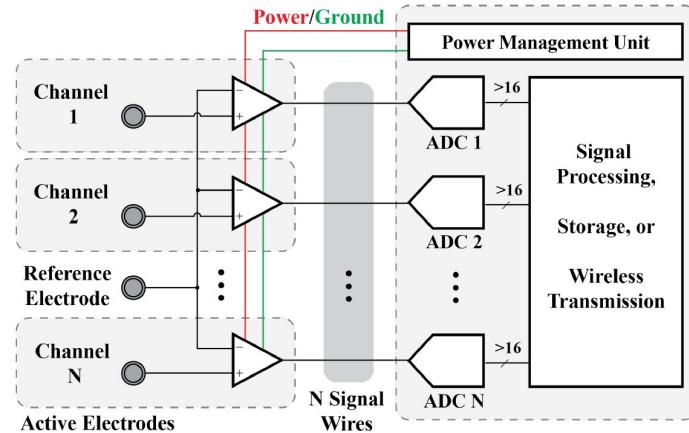
## Design Changes

- Use FM-FDM to aggregate all signals onto single wire
- Sacrifice bandwidth for signal quality
  - Directly control SNR with bandwidth

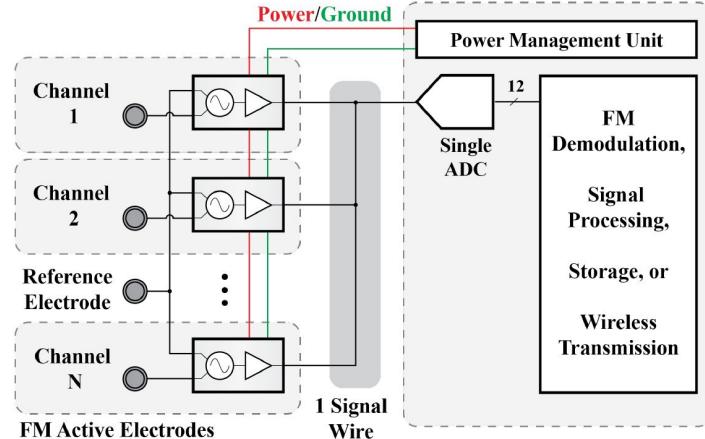
## Design Benefits

- One ADC
- Single wire
- Extendible

## Current Approach



## Proposed Approach



# Project Impact

## Direct Improvements

- 30x reduction in volume
- 30x reduction in weight
- 10x improvement in signal quality
- 2x reduction in cost

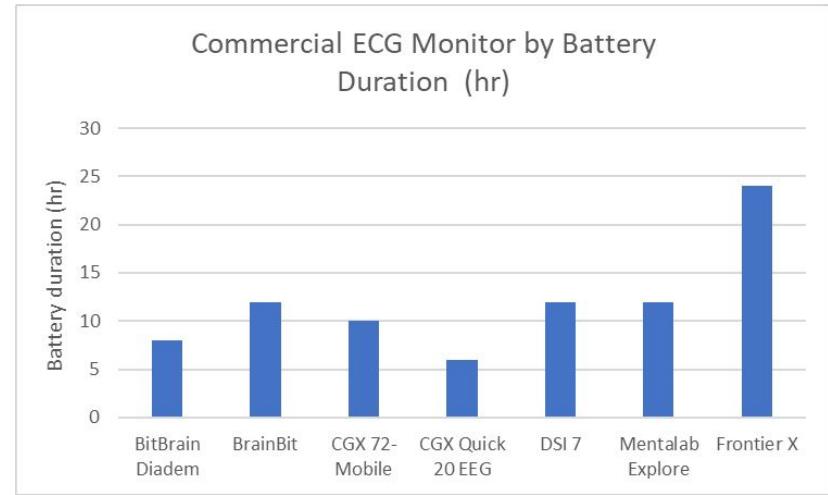


# Project Impact

- Medical research and diagnostics
- Battery powered - long-term collection of biopotential data
- Bring ExG collection outside the lab

## Example Application

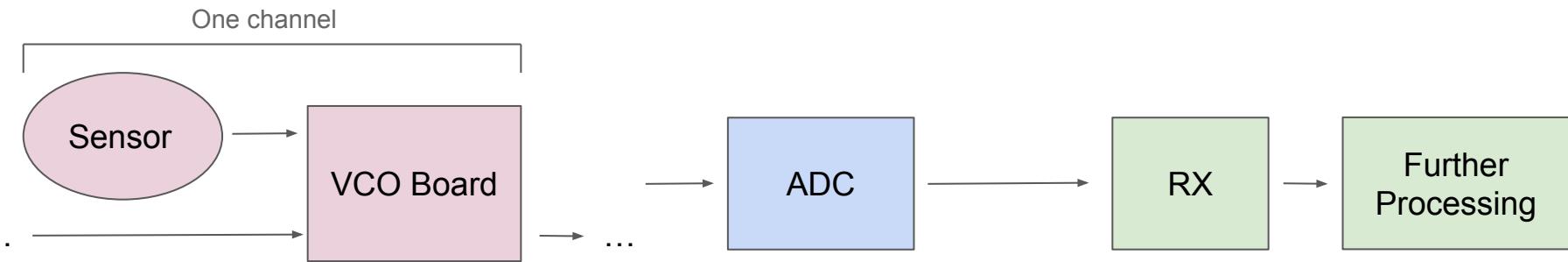
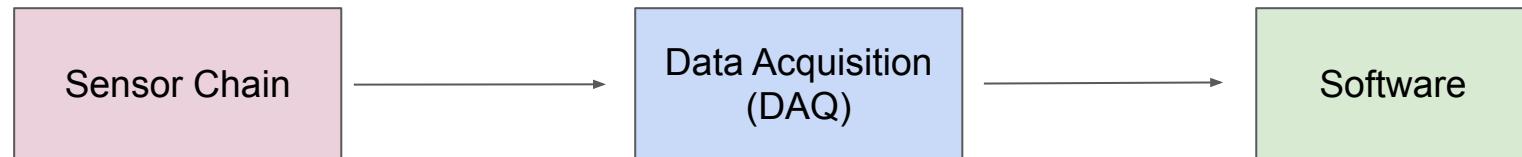
- Analyzing newborn EEG to determine hearing loss
- Small form beside monitor with multiple channel acquisition



# Project Overview

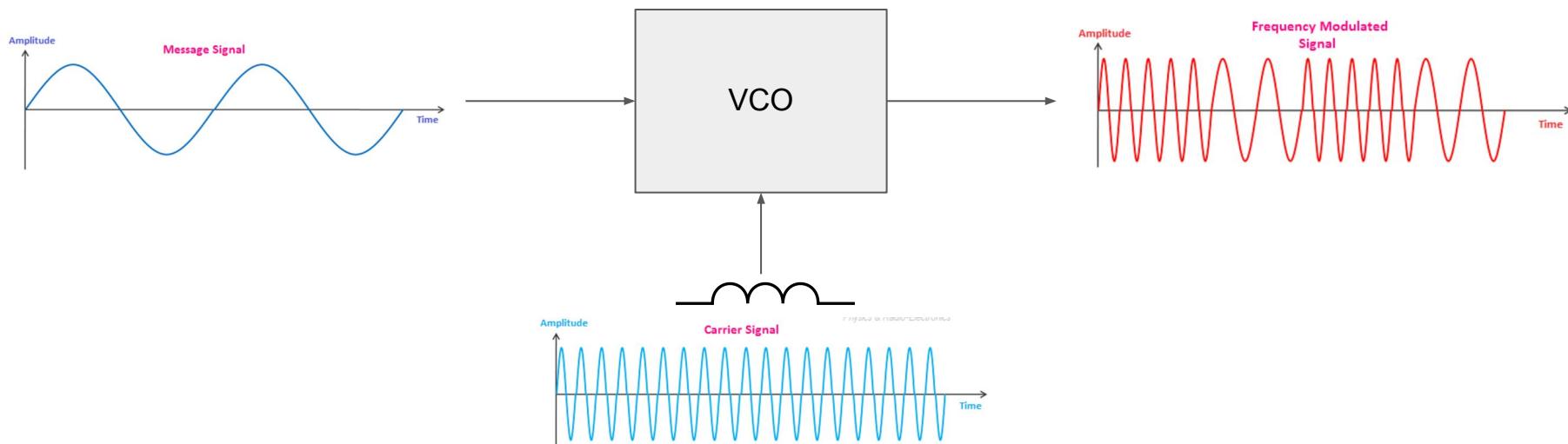
- Inherited
  - Custom board design with VCO and channel-isolating buffer
  - Software for 36 channel system at 2MHz
- Issues
  - Sensor boards not working when chained together
  - Cannot implement current software setup with off the shelf parts
- Main Accomplishments
  - Developed data collection pipeline to acquire real signals
  - Revision 2 of custom board with promising simulation results
  - Redesigned software to be compatible with hardware requirements

# System Overview

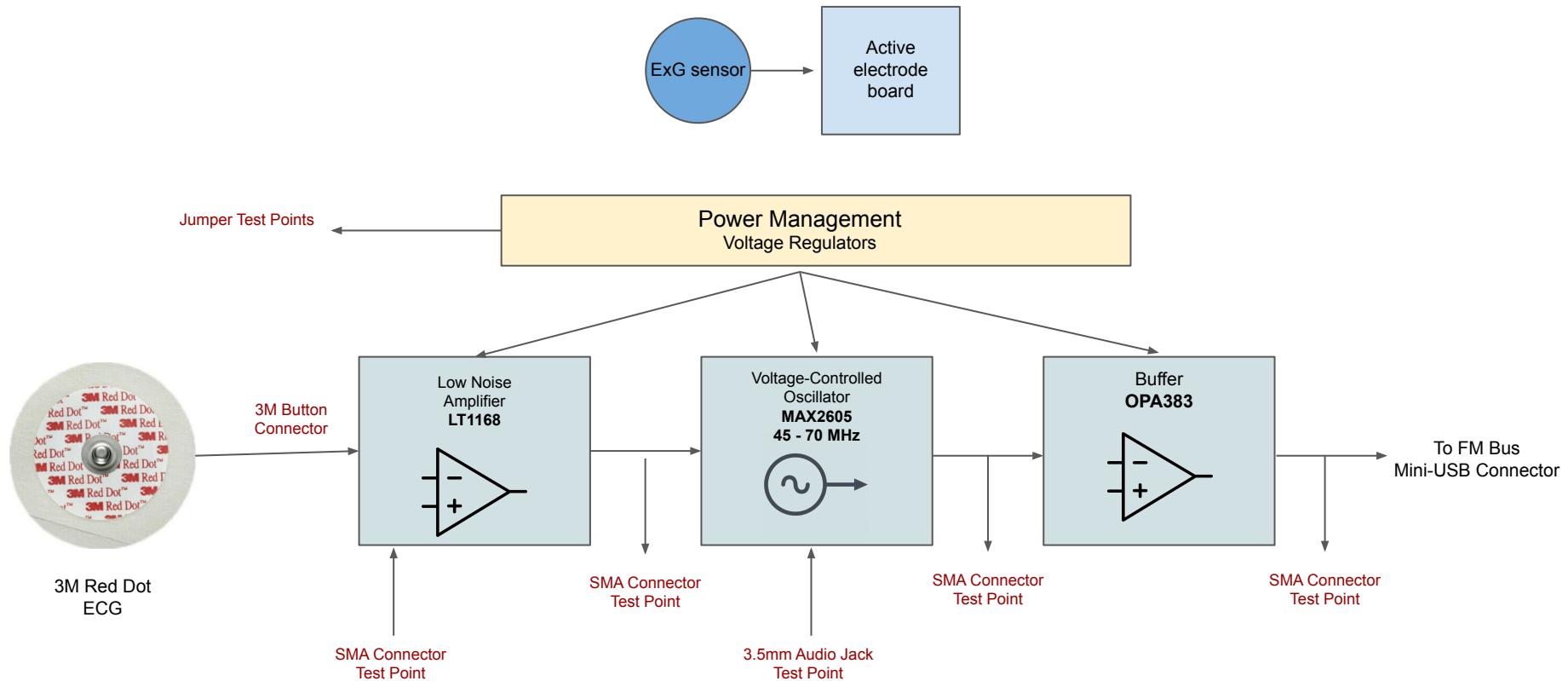


# Voltage-Controlled Oscillator (VCO)

- Fundamentally an inductor-capacitor (LC) circuit that produces a persistent sinusoidal signal
- Hard-set “center” frequency with inductors
- VCO ICs provide input to “tune” the frequency deviation
- Feed message signal into tuning input



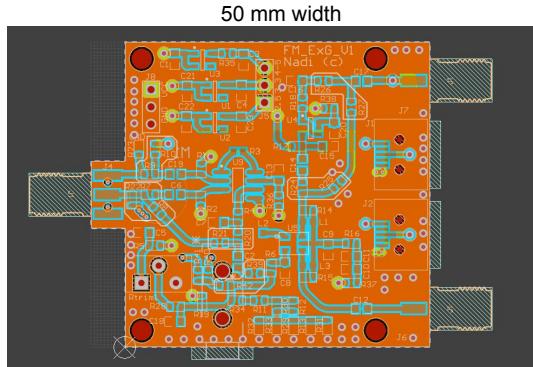
# Inherited VCO Board Design



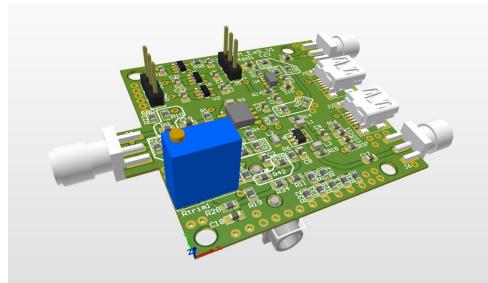
# Board Fabrication

- Altium CircuitMaker
- 4-layer board
- Imported symbols and footprints from integrated part searcher
- Sent manufacturing (silkscreen, routing, solder mask etc.,) files to PCBMinions

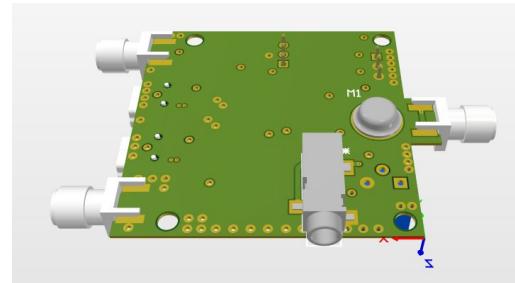
45 mm height



*Routing view*

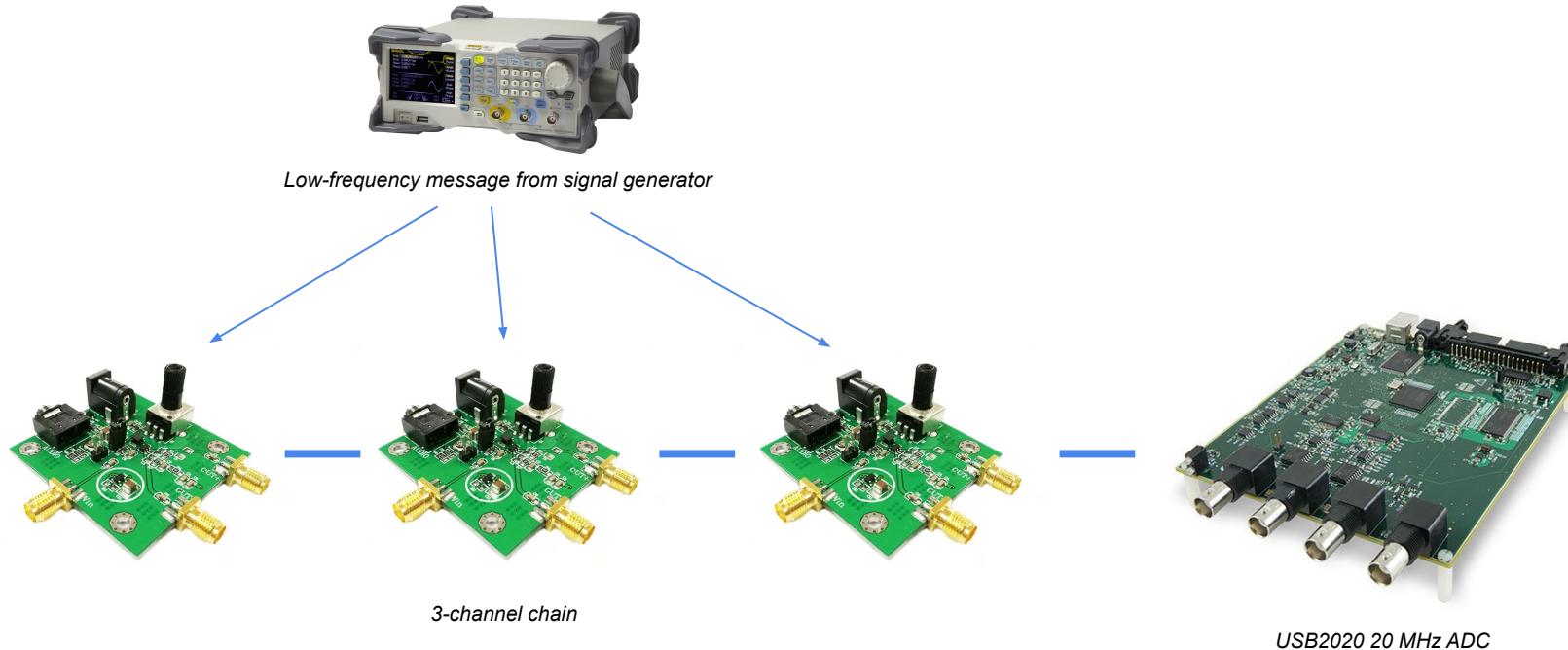


*3D render views*

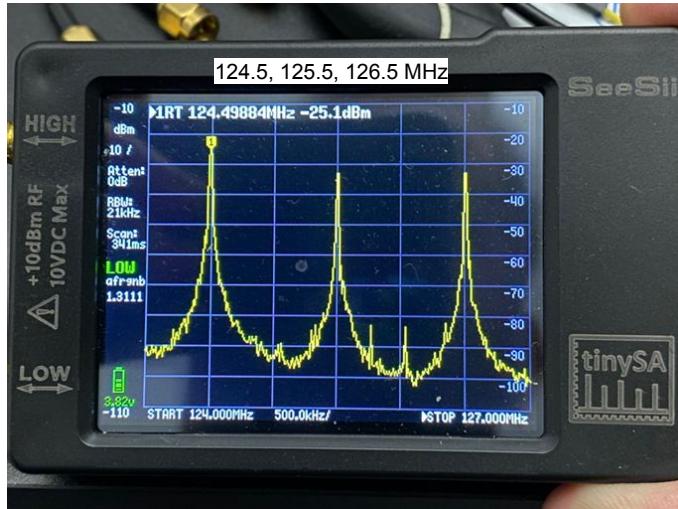


# Proof-of-concept

- Off-the-shelf MAX2606 evaluation board with similar design exists
- If boards are chained, will summation work?



# Results

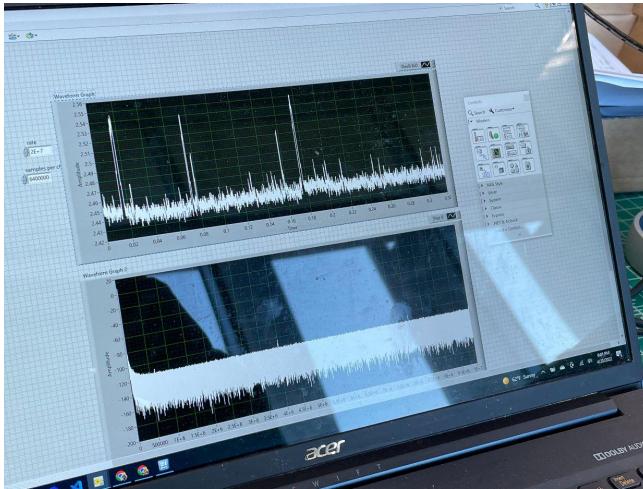


Spectrum analysis of three center frequencies



Wider bands after low-frequency 40 mVpp message is fed

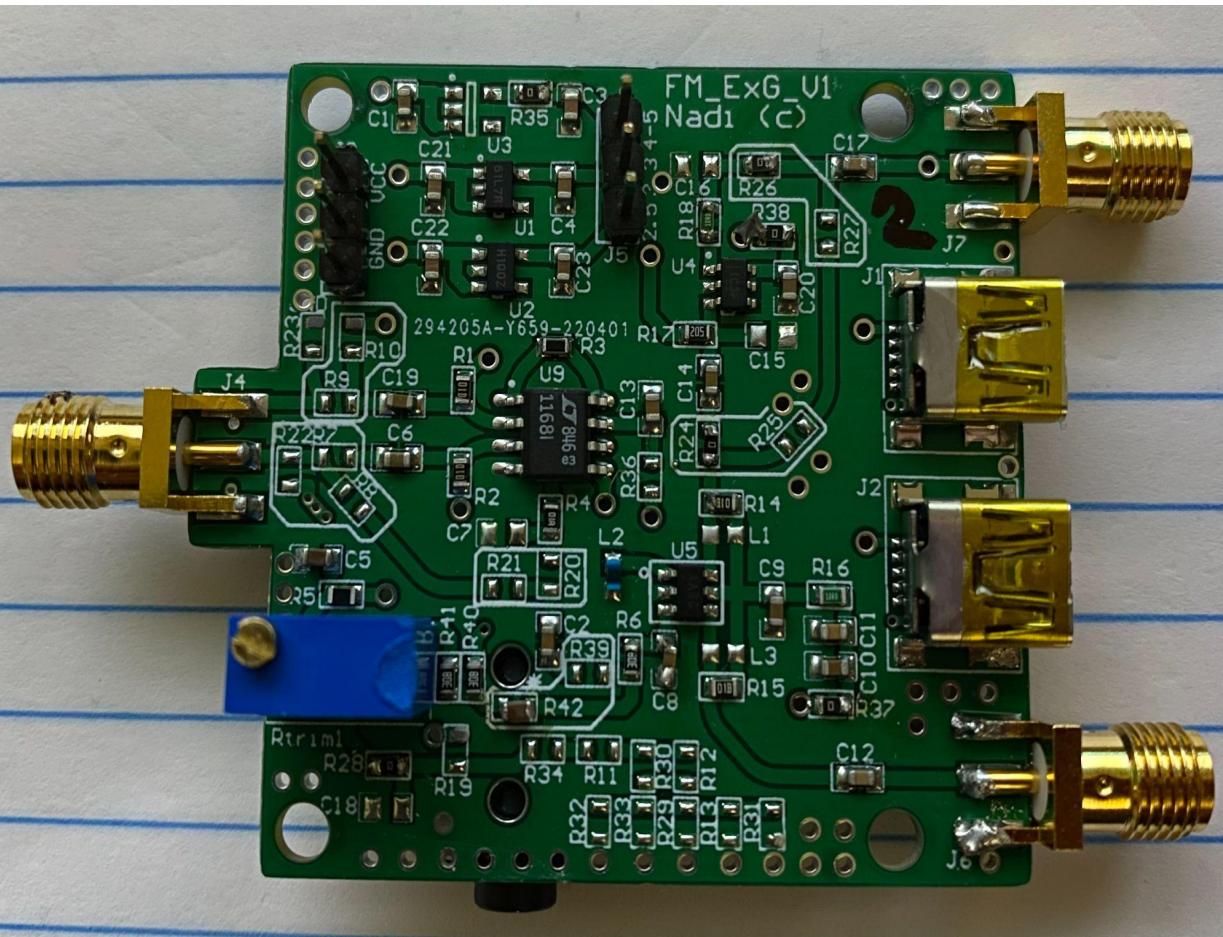
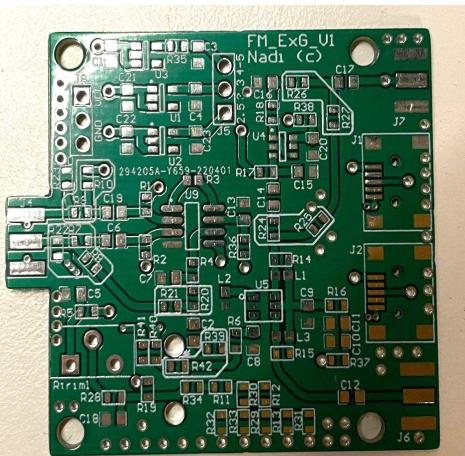
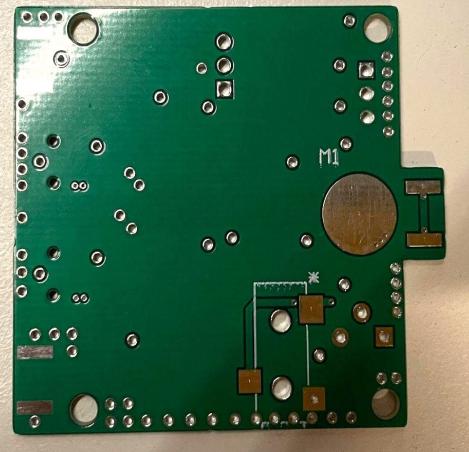
# Results



Pure garbage readings

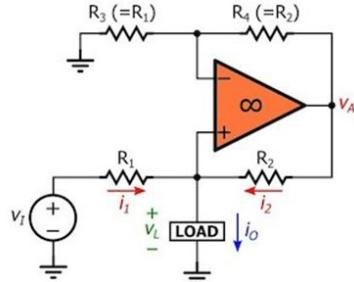
- No intelligible signal acquired
- Side experiments showed DAQ **attenuates signals above ~15 MHz**; this was confirmed in the datasheet
- Two solutions: find DAQ with higher bandwidth, or **increase V<sub>pp</sub> of aggregate signal**

C

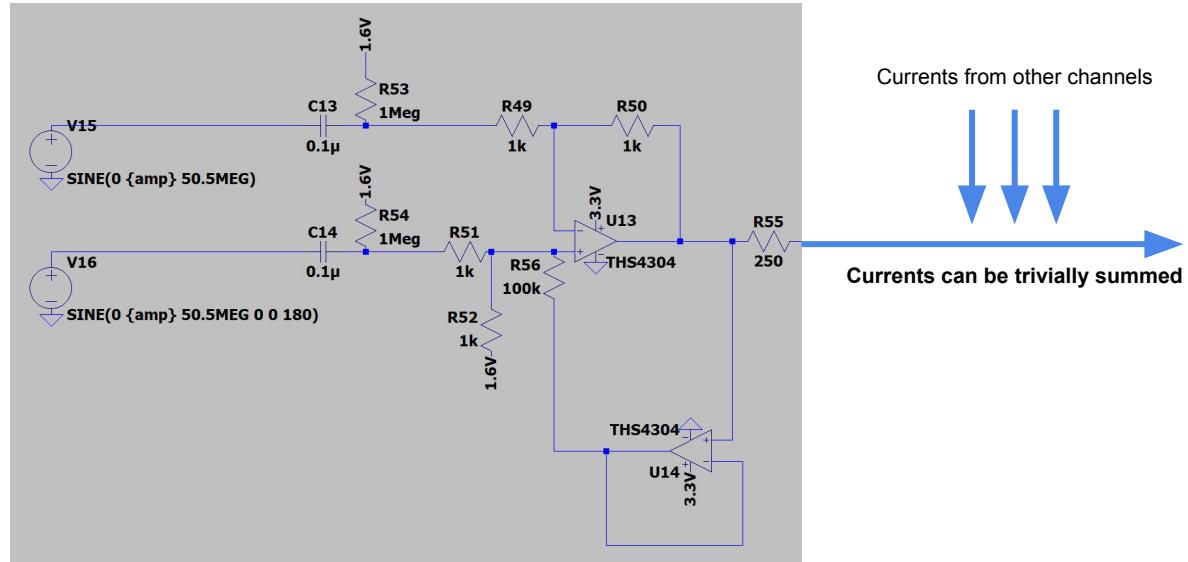


# Voltage-to-Current Buffer

- Modified Howland current pump to take in VCO's differential voltage
- Switched to **higher-speed THS4304 op amp** with flatter response curve
- Addition of unity-gain buffer **lowers resistor tolerance sensitivity and output errors caused by feedback current**
- Stabler attenuation in 8-channel chain according to simulation



Traditional Howland current pump

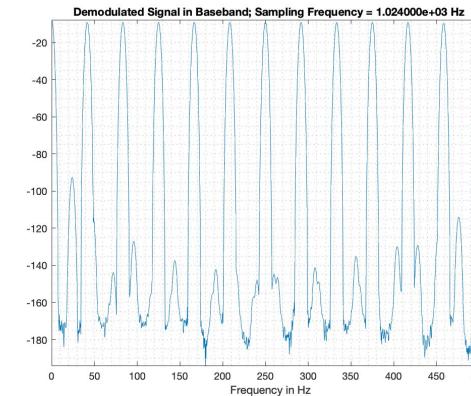
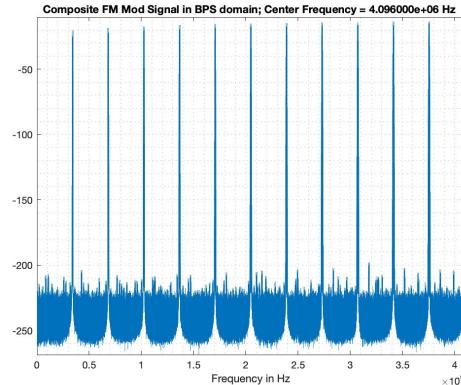


Modified differential current pump

# Software Overview

- Two main modules (Matlab scripts)
  - TX: used for testing, generating/modulating ideal signals
  - RX: used for demodulating signal and separating channels
- Improved simulation capabilities of TX
- Convert system to 12 channels at 8MHz to solve hardware bandwidth issues
- Implemented RX and plotting in Python

TX  
Ideal Test Signal



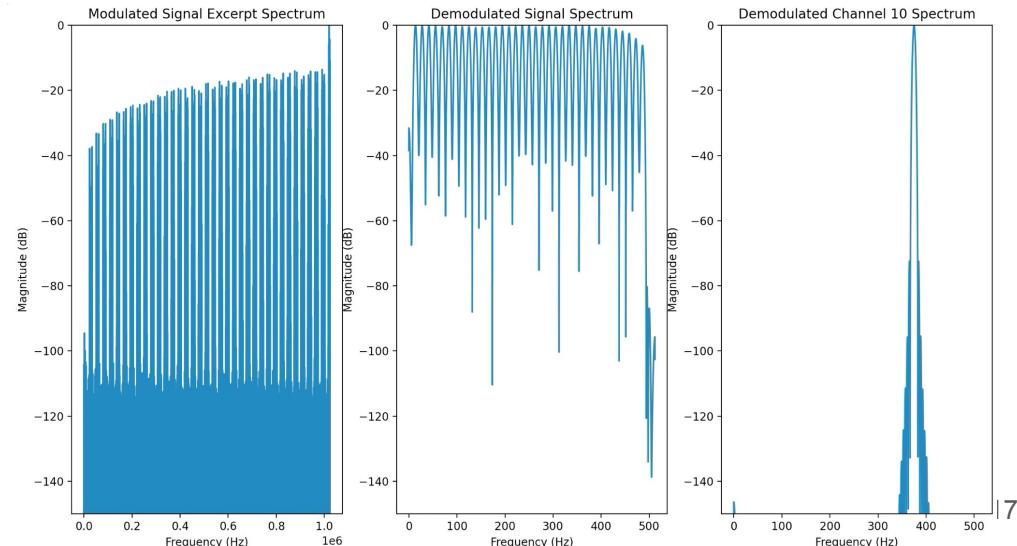
RX  
Demodulated Signal

# Python Implementation

## Motivation

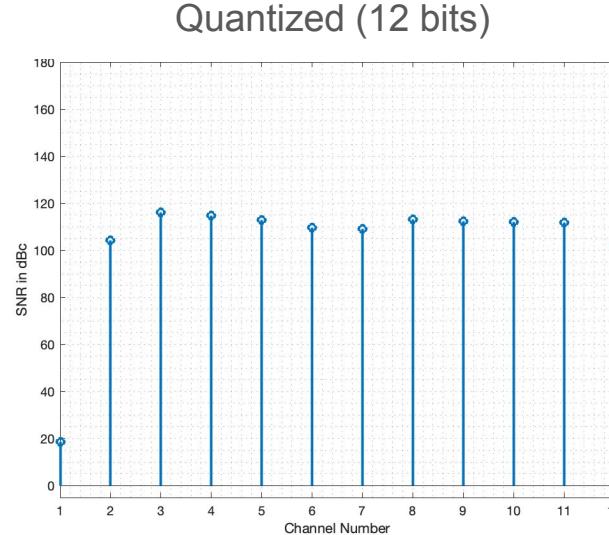
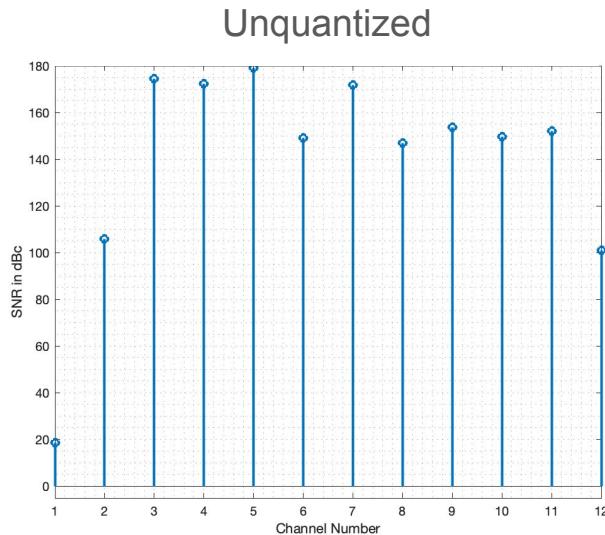
- Issues with Matlab libraries reading from our DAQ
- Python is more extensible for future use case

- Implemented RX
- Implemented real-time plotting
- Note: Python and Matlab functions don't work the same!



# Software Current Status

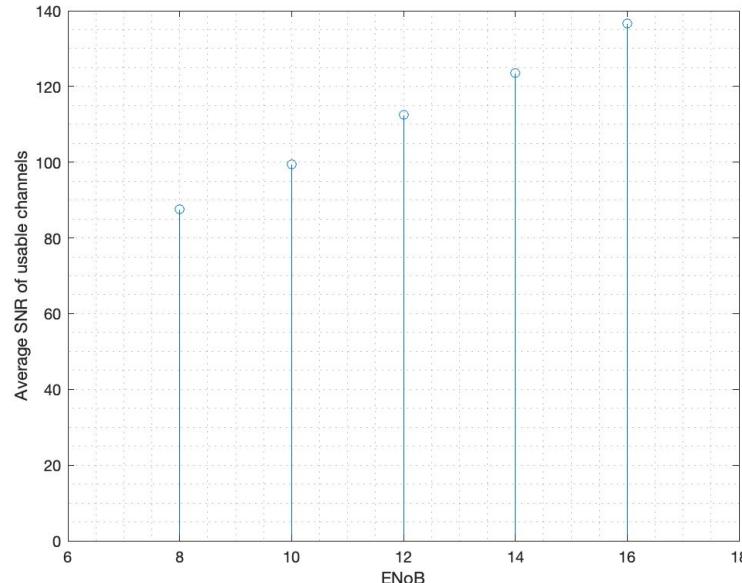
- Ready for signal acquisition
- Python implementation ready to build off of
- Remaining issue: Quantization reduces SNR



# Quantization

- Current ADC uses 12 bits
- Simulations show not enough for 140dB
- Can this be fixed with
  - More bits?
  - More bandwidth?

Average SNR vs. ENoB



# Outcomes

## Hardware

- Set up data collection pipeline
- Verified functionality of inherited rev. 1 boards
- Discovered critical flaw with rev. 1 design
- Simulated and validated improved buffer design for rev.1 board
- Designed and fabricated rev. 2 board (pending arrival)

## Software

- Transitioned from 36 to 12 channel system
- Implemented Python mirror of RX + additional plotting functions
- Discovered issue with existing setup and outlined steps to resolve

# Next Steps

## Hardware

- Validate rev 2. board with 3 channel
- Setup 12 channel system and acquire sample signals
- Pass samples off to software to recover original sensor signals

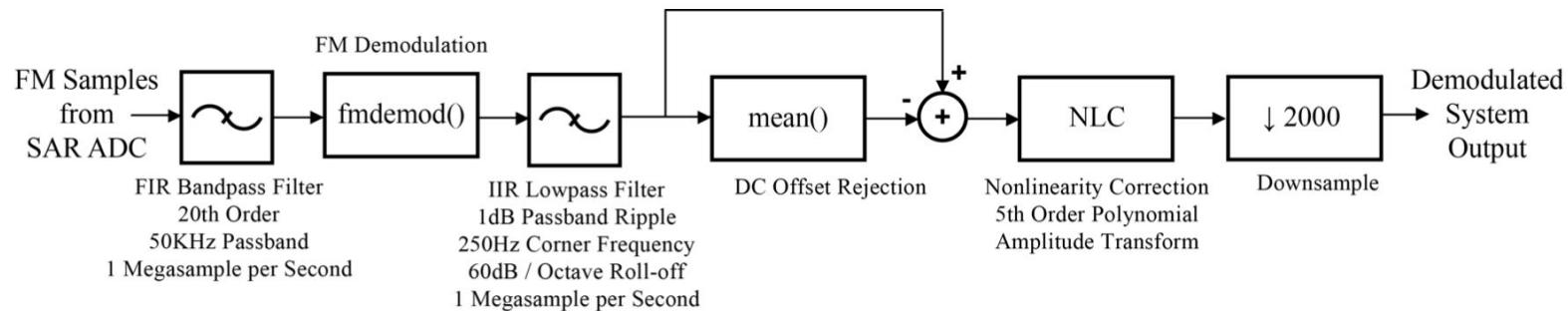
## Software

- Verify that 12 channel RX works with sample signals
- Take steps to resolve quantization issue
- Build upon Python implementation to develop machine learning algorithms



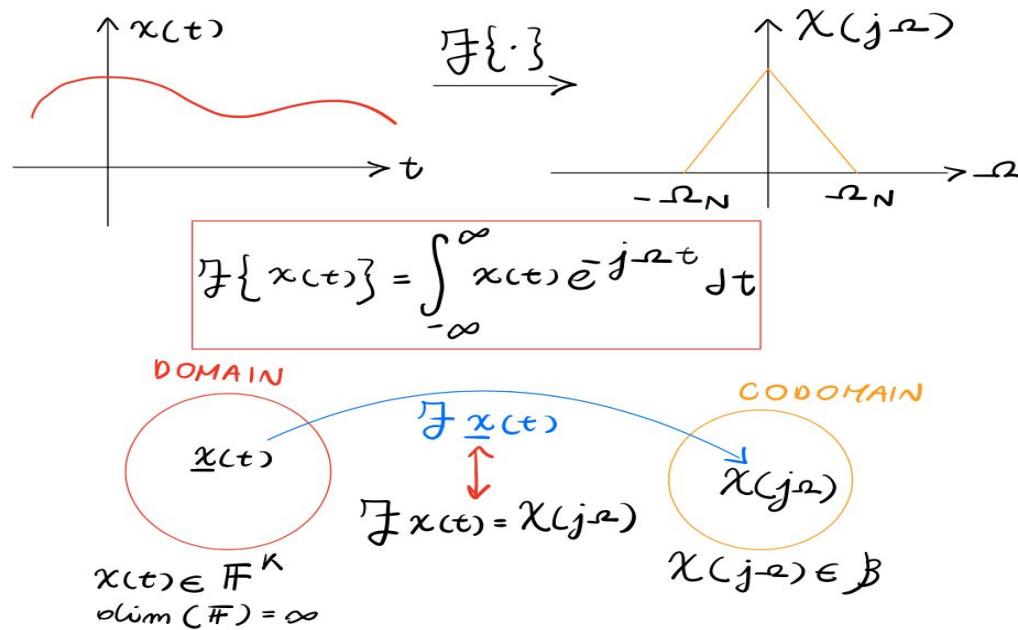
# Mathematical Formulation

- The Signal Processing aspect can be summarized by the following block diagram:
  1. Linearity of the CTFT
  2. FM and Sampling
  3. BandPass filtering, Non - Linearity, Down Sampling



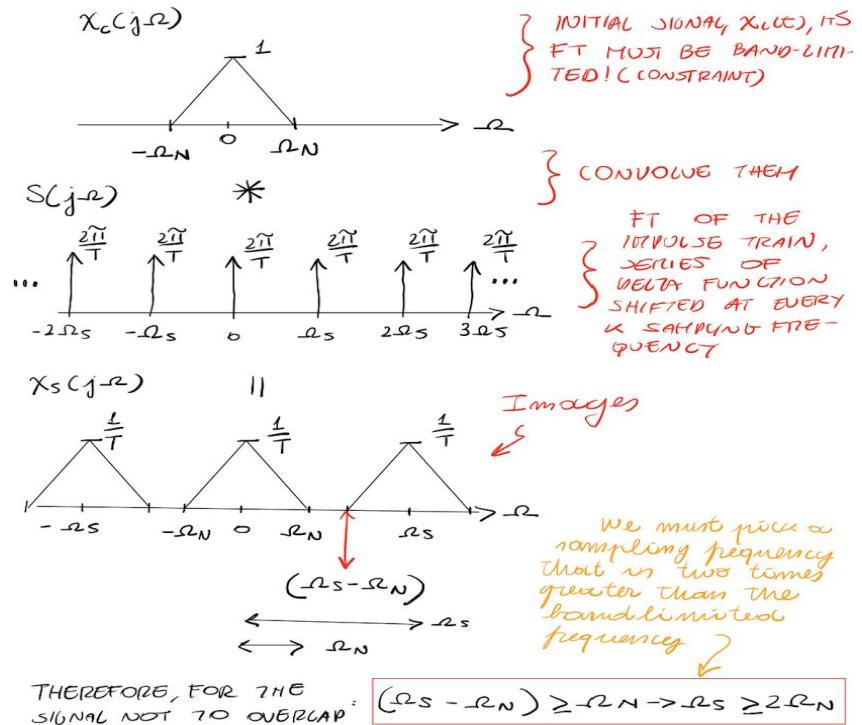
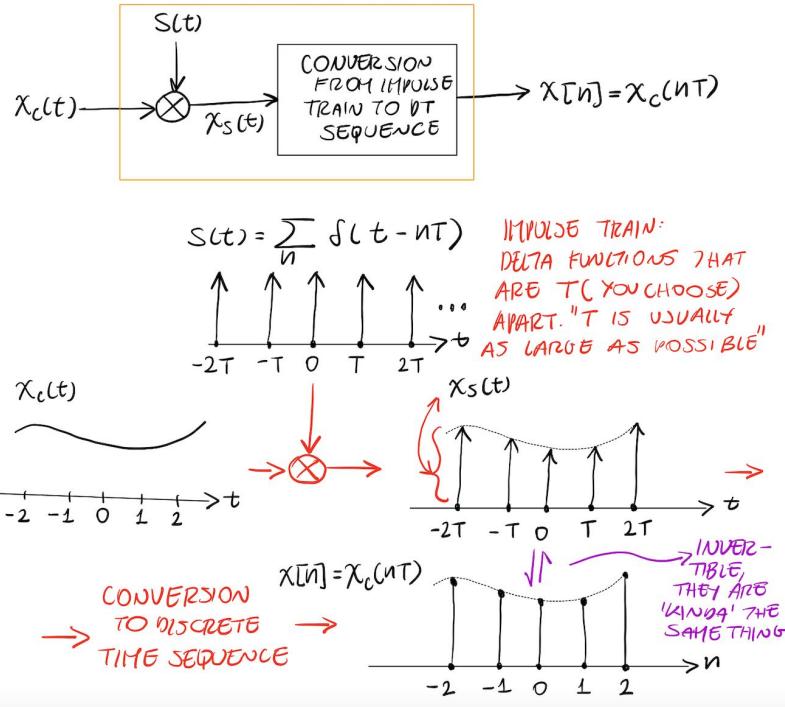
# Mathematical Formulation

- Definition of the Continuous - Time - Fourier Transform (CTFT)



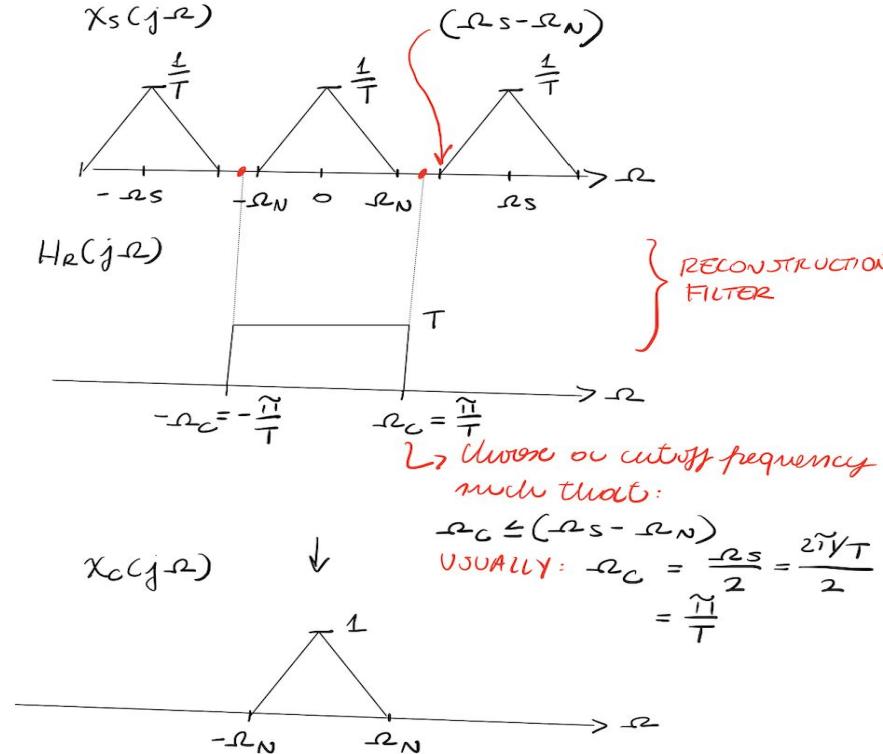
# Mathematical Formulation

## - Sampling



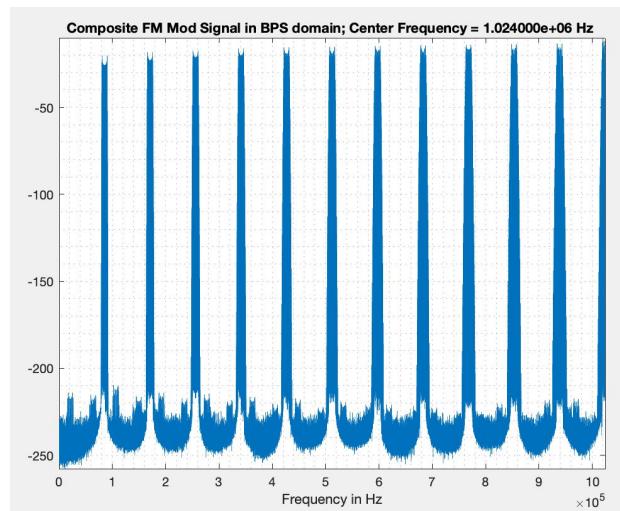
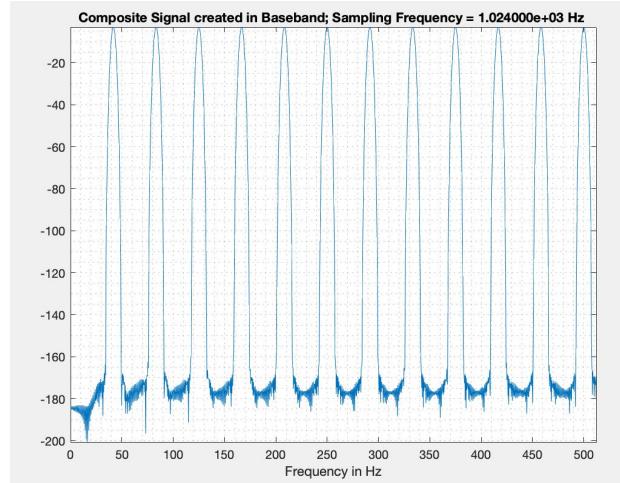
# Mathematical Formulation

## - Recovery



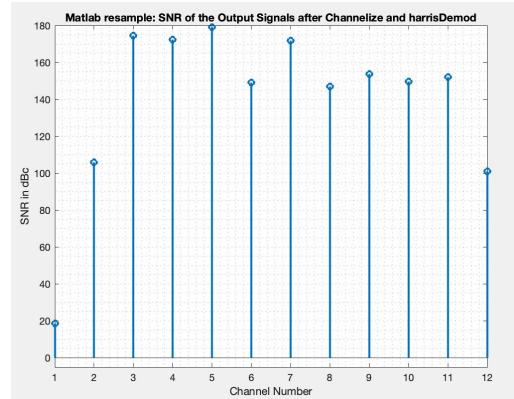
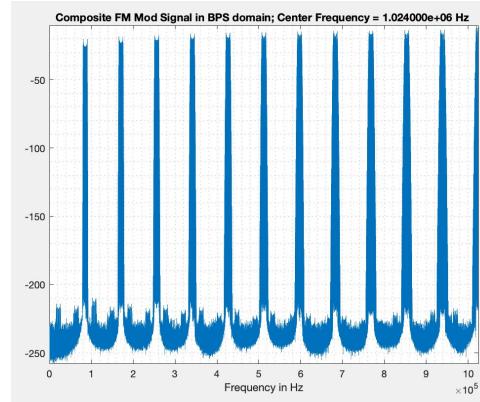
# TX

- Generates and modulates ideal signal
- Added non-ideal effects
- Cleaned up, documented, can vary channels and bandwidth



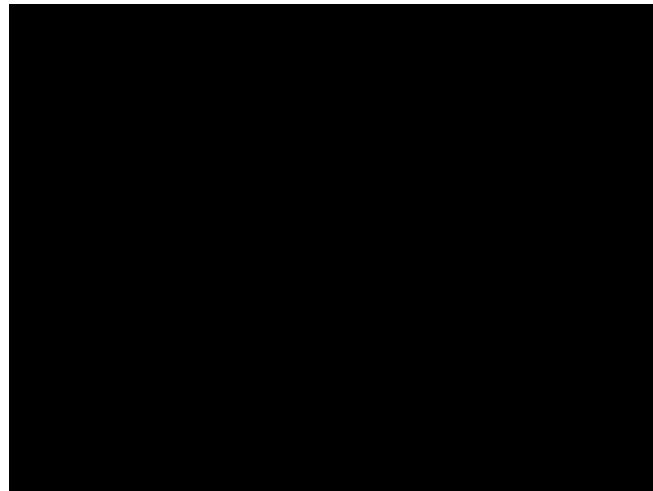
# RX

- Demodulates and channelizes signal
- Calculates SNR of test signals by comparing to original sin waves



# RX Python Implementation

- Implemented RX with Python
- Added real time plotting module in preparation for reading signal

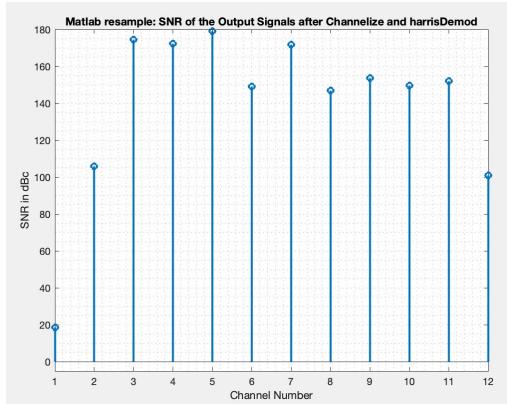


- Issues with capturing signal + other design changes -> back to Matlab

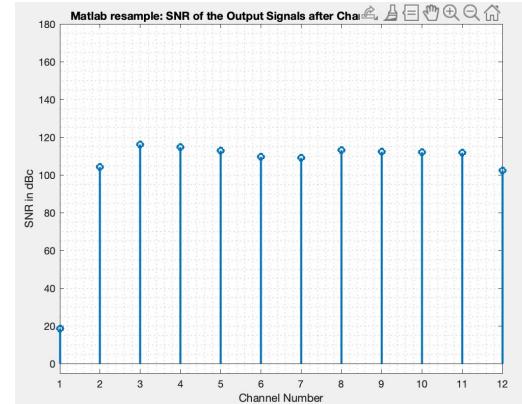
# Remaining Issues

- Redesign to give hardware more bandwidth per channel
  - Reduce channels, increase sampling rate
  - Redesign filters to account for different number of channels
- Quantization
  - Quantizing to +/- 1V with 12 bits
  - Lowers SNR too much

**Quantized**

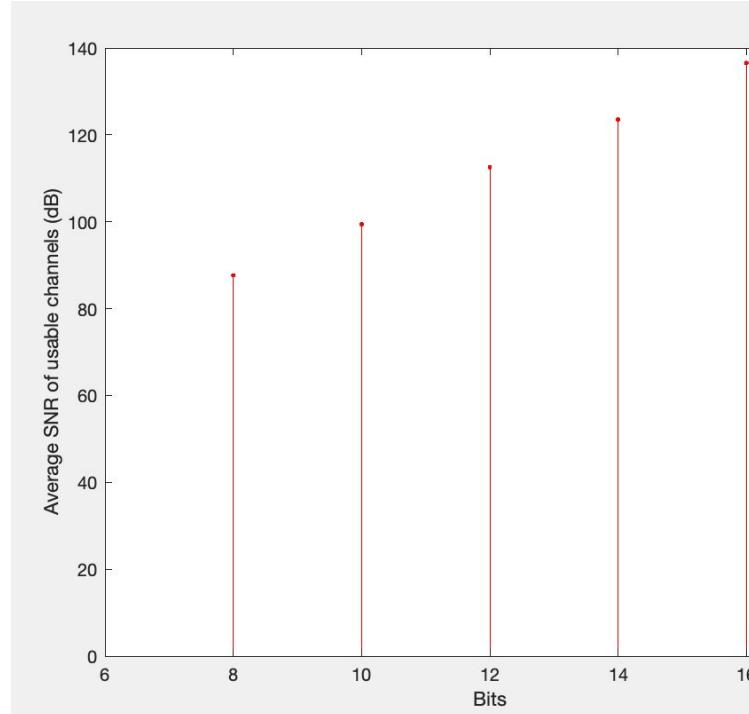


**Unquantized**



# Quantization

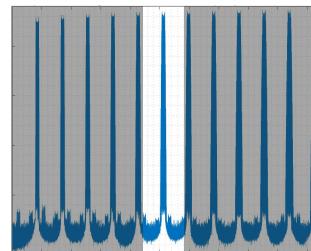
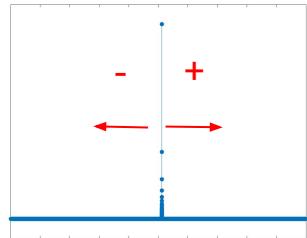
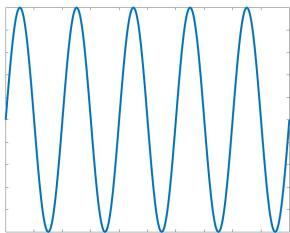
- Do we need a better ADC? (Amplitude)
- Can we fix this with more BW? (Frequency)



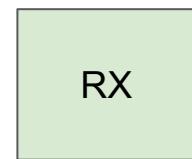
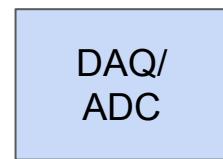
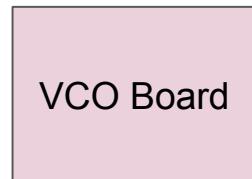
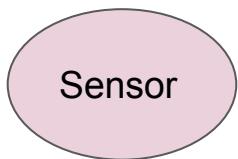
Change X axis: Bits  $\rightarrow$  ENoB

- Can always trade off amplitude domain resolution for freq domain resolution

# System Overview (Not gonna use, maybe backup)



\* More details on theory in Backup Slides



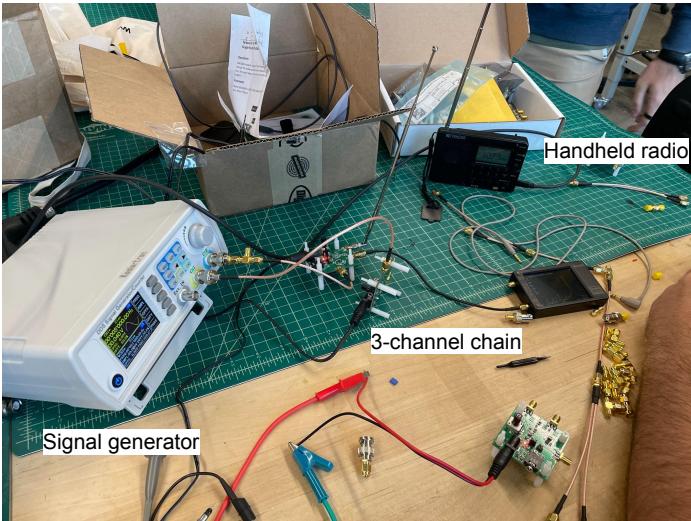
# Maxim 2606 VCO IC

- Low-power (< 1 watt)
- Low phase noise
- 70 to 150 MHz operating frequency range
- Development board available

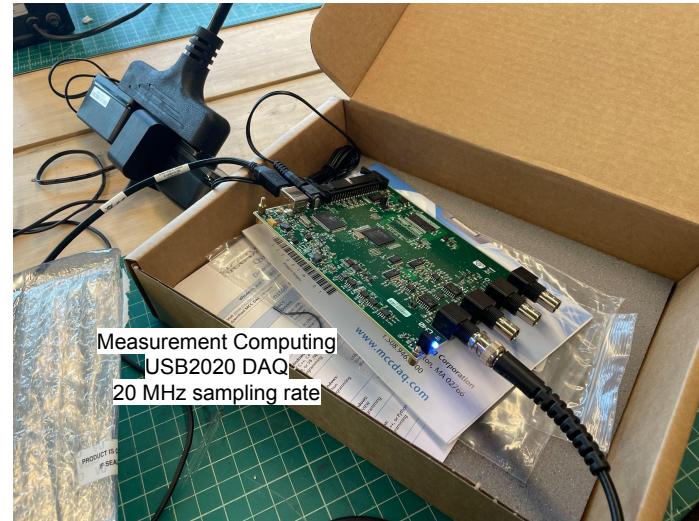


# Dev. Board 3-Channel Preliminary Experiment

- Verified FM functionality of board by feeding audio signal -> receive with radio
- Tune center frequencies using trim potentiometer, ensuring sufficient guard band
- Chain together in series
- Sample with data acquisition system (DAQ)
- Perform digital Fast Fourier Transform (FFT) to detect bands

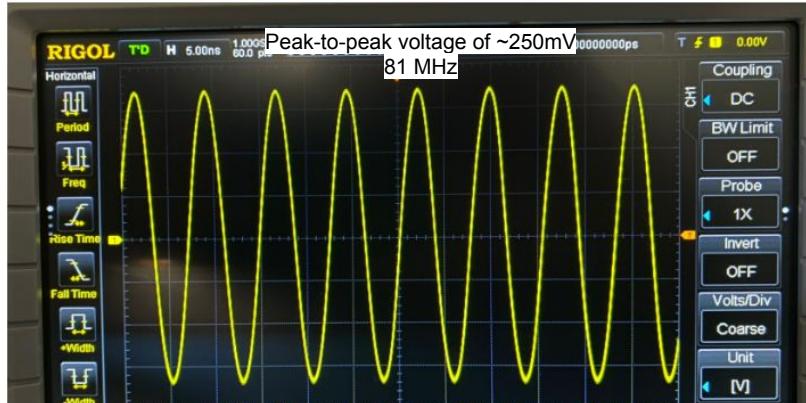


*Experimental setup*

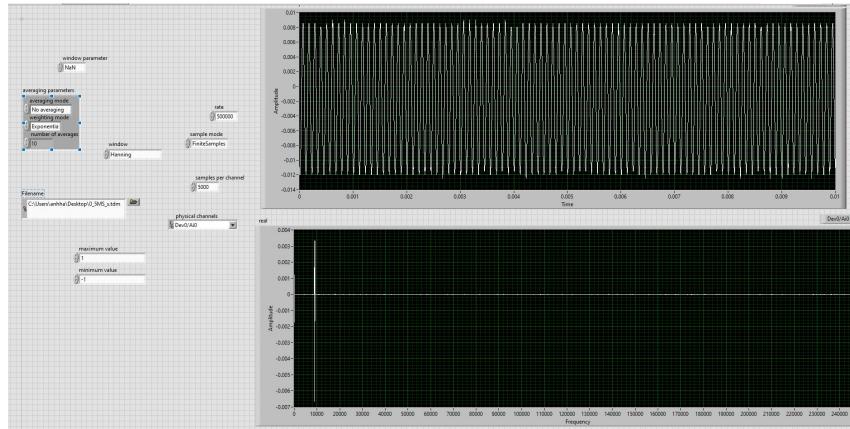


*DAQ*

# Data Collection



Oscilloscope of one channel  
with 0V message



DAQ interface collection  
through LabVIEW

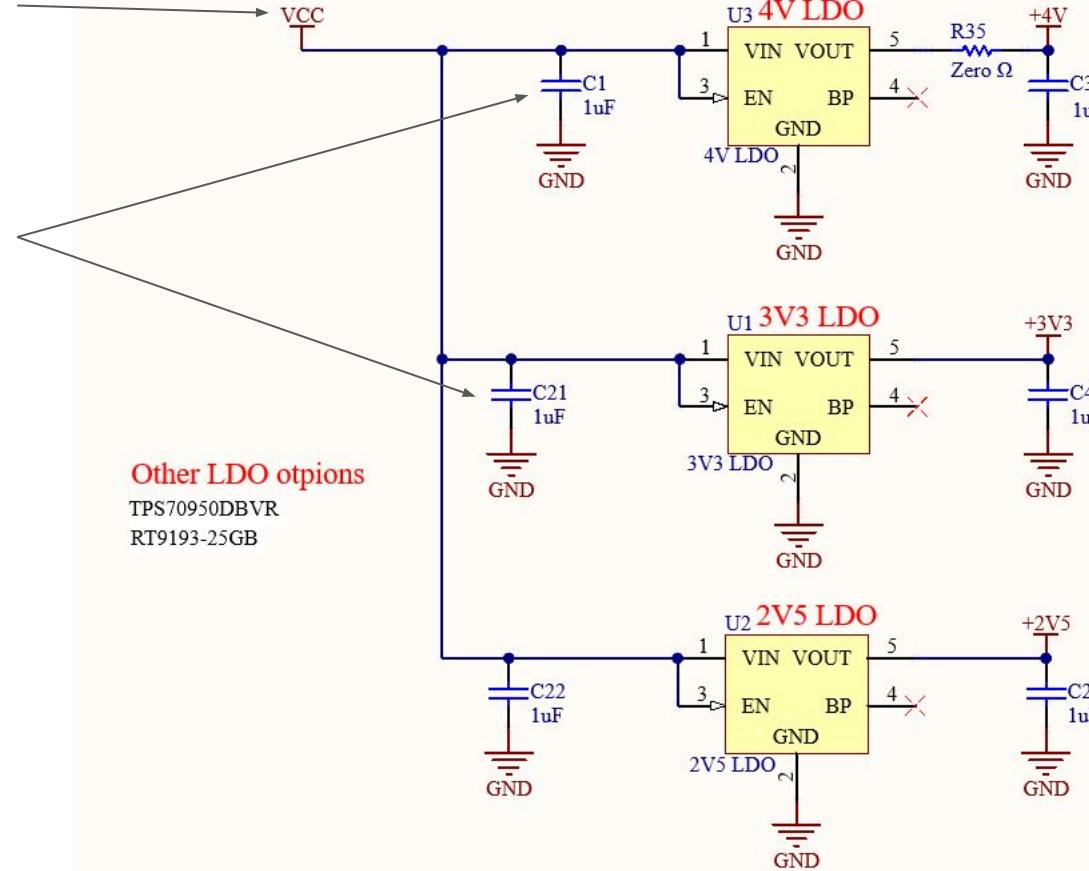
# POWER MANAGEMENT

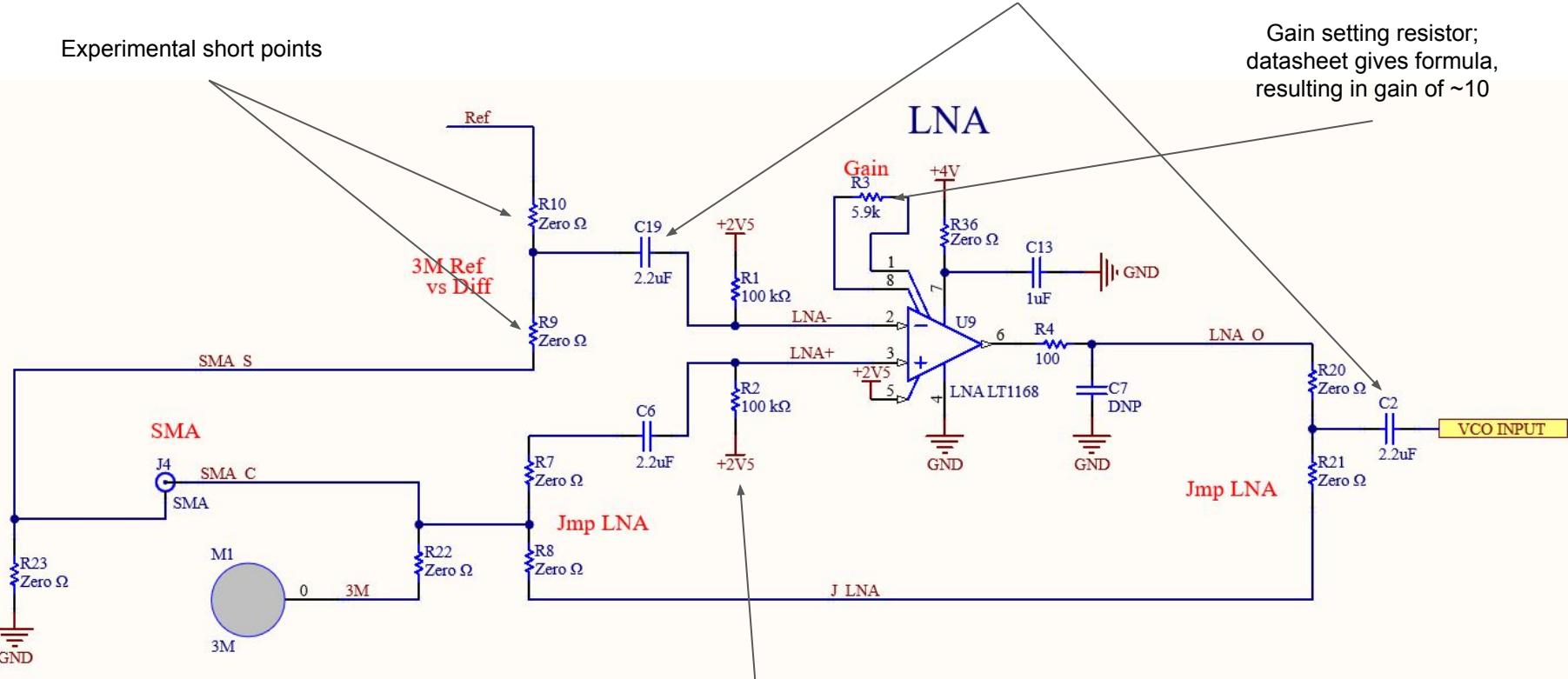
5-9V supply from  
Mini-USB  
connector

AC noise bypass  
capacitors

Other LDO options

TPS70950DBVR  
RT9193-25GB

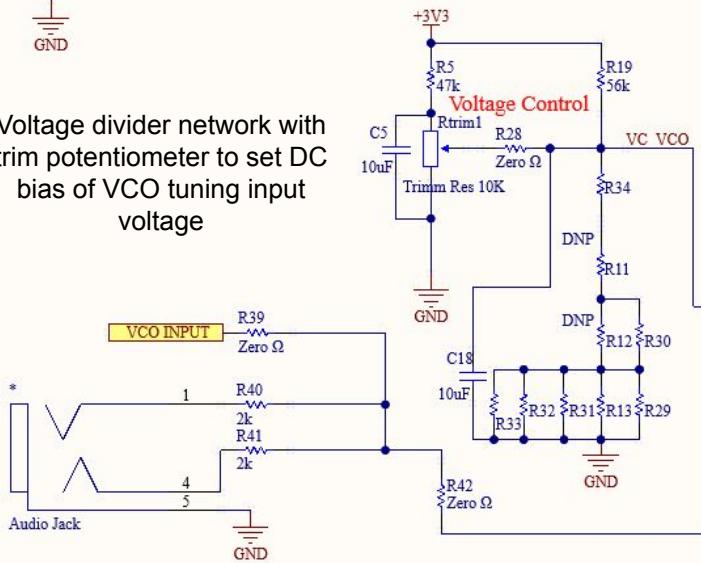




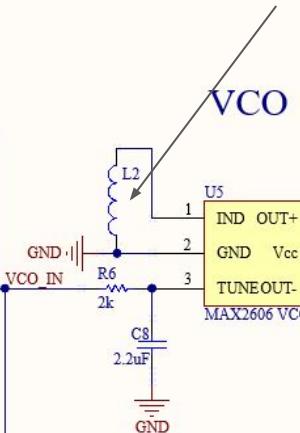
2.5V DC bias for max headroom

GND

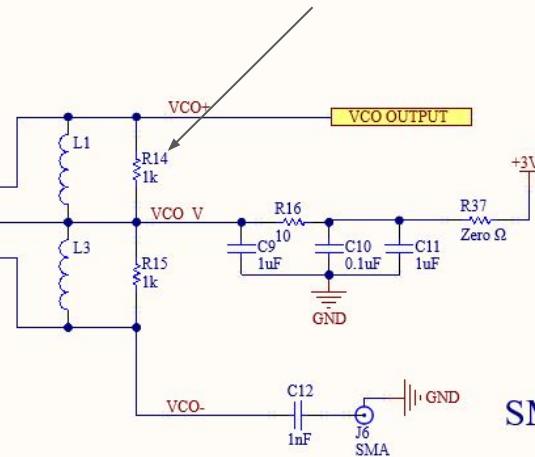
Voltage divider network with trim potentiometer to set DC bias of VCO tuning input voltage



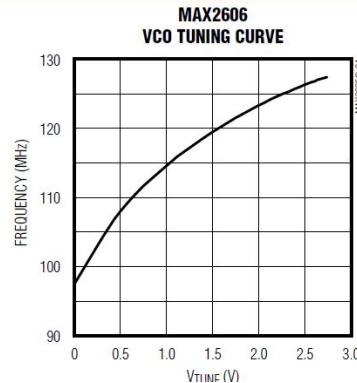
Fix center frequency using high-Q inductor



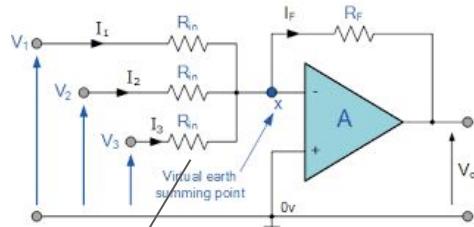
Pull up open-collector output to 3.3V as per datasheet suggestion



SMA OUT -

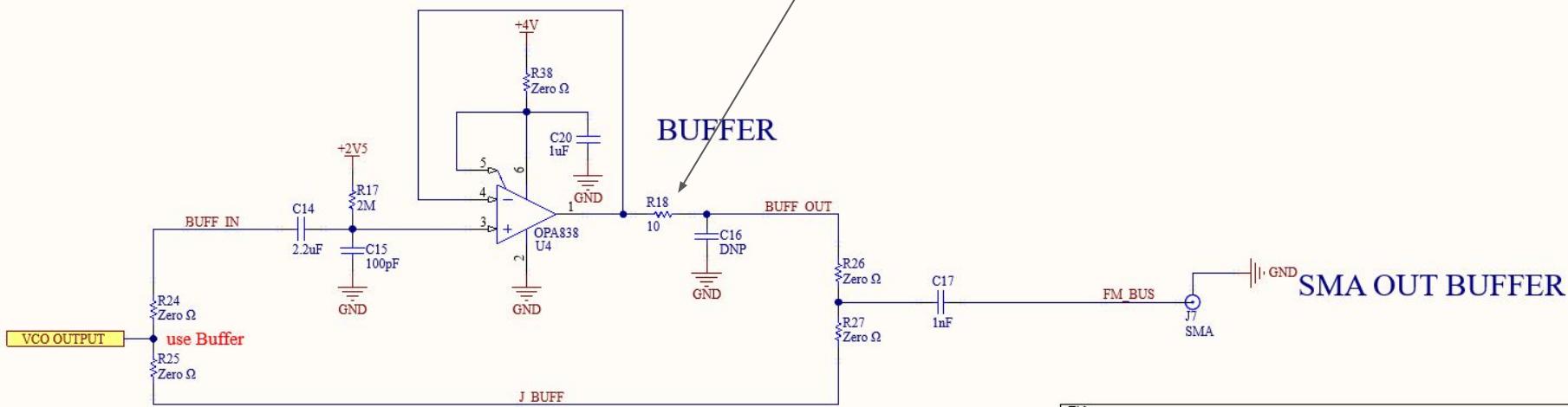


10 ohm resistor allows a current-mode summing resistive network, where the ADC at the end of FM bus receives aggregated signals



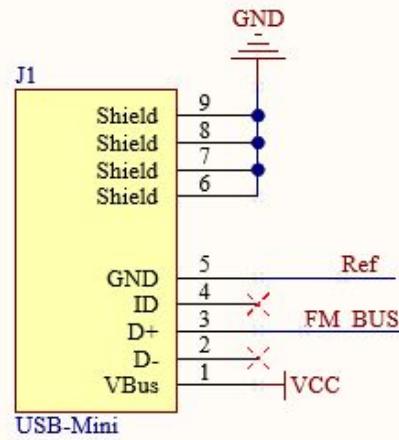
$$-V_{out} = \left[ \frac{R_F}{R_{in}} V_1 + \frac{R_F}{R_{in}} V_2 + \frac{R_F}{R_{in}} V_3 \right]$$

Figures taken from  
[https://www.electronics-tutorials.ws/opamp/opamp\\_4.html](https://www.electronics-tutorials.ws/opamp/opamp_4.html)

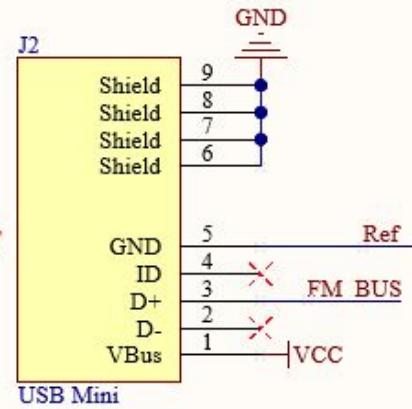


Unity-gain buffer offers isolation of active electrode from interference of other modules on the same FM bus

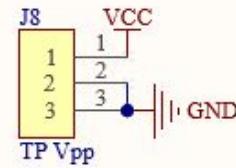
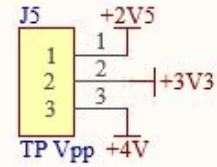
### CHAIN INPUT



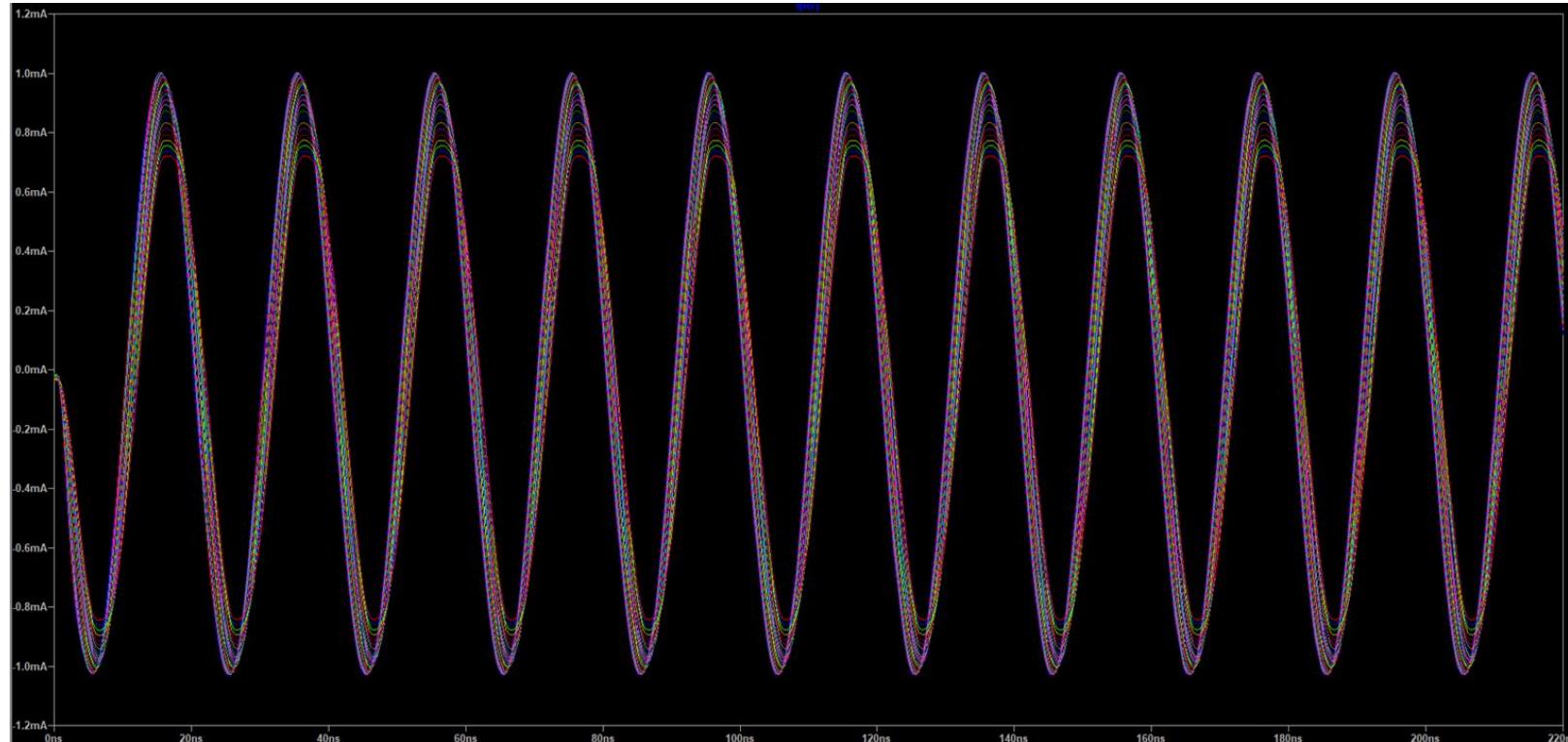
### CHAIN OUTPUT



### Test Point

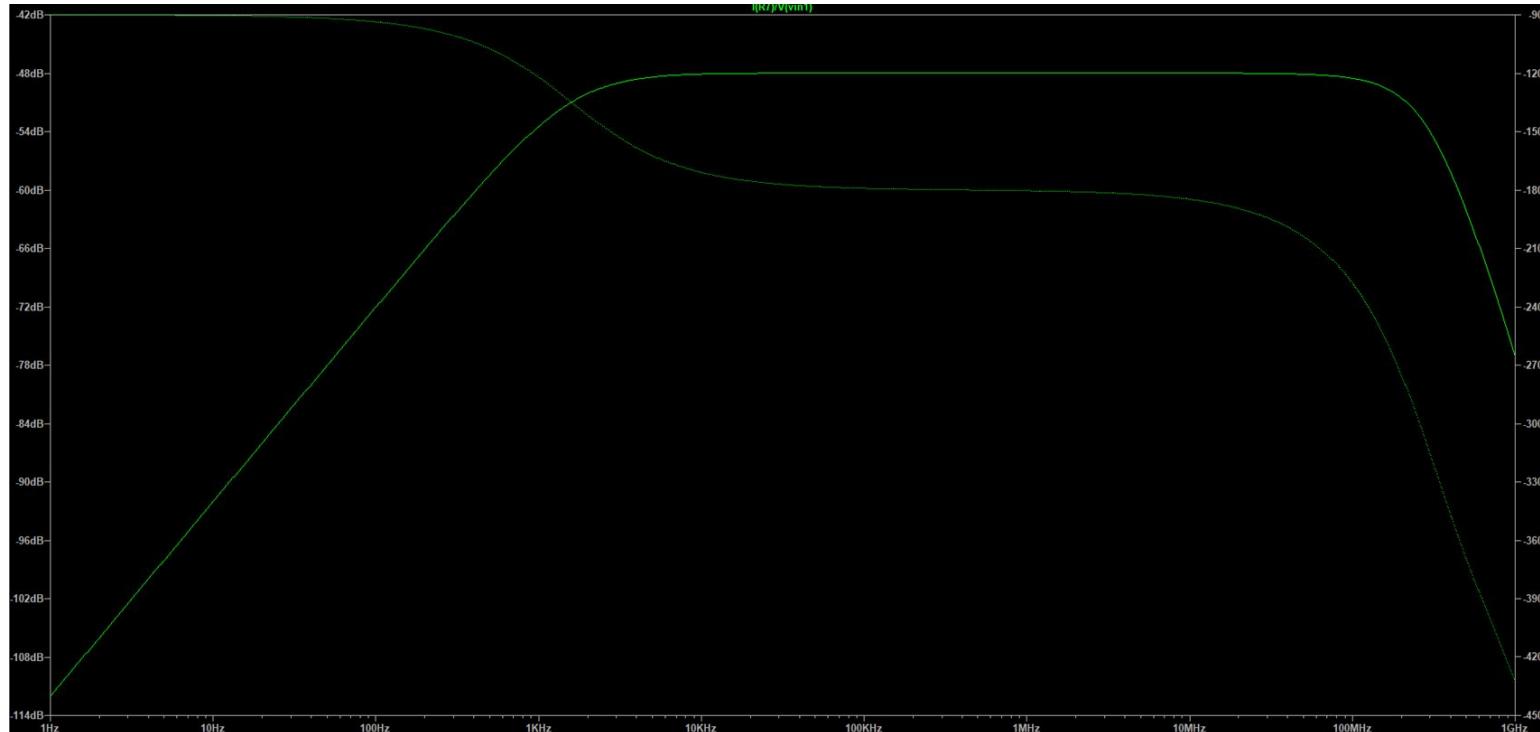


# LTS spice Simulations



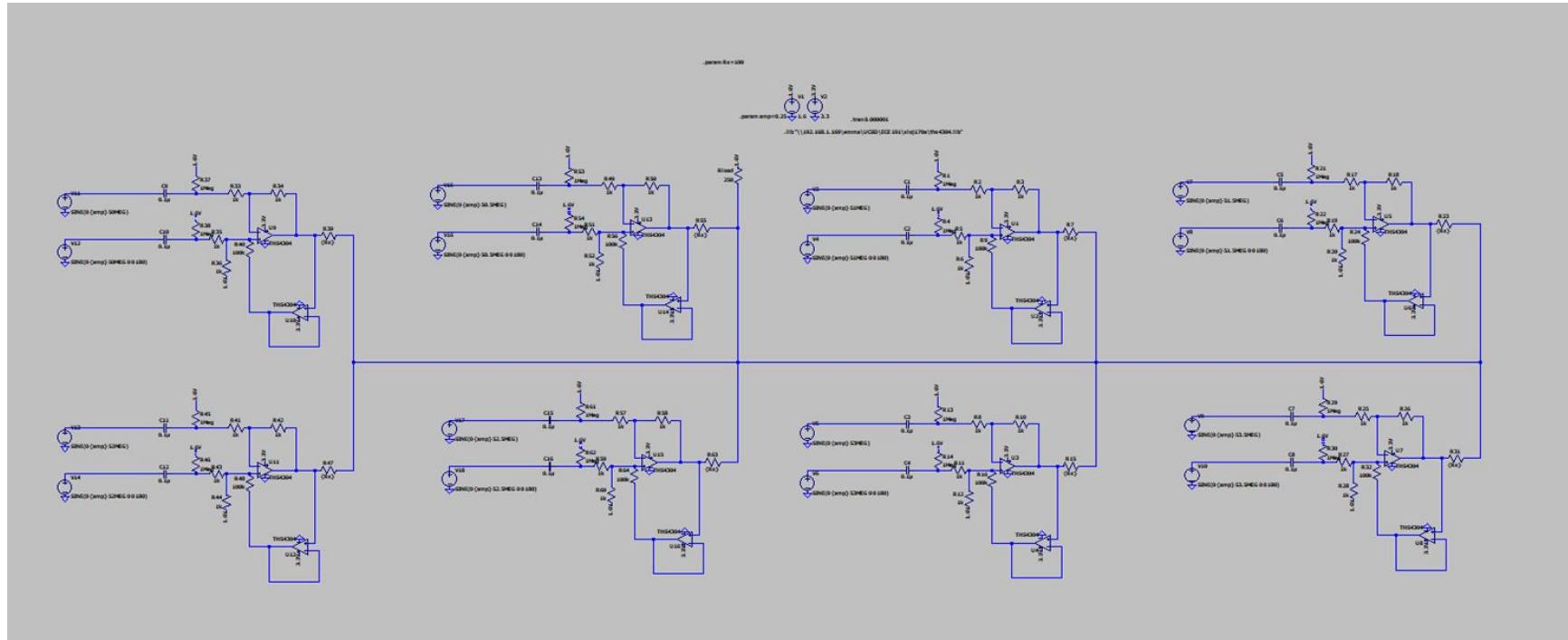
*Minimal deviation in current with load resistor sweep from 1 to 1k  
proves current source behavior*

# LTS spice Simulations



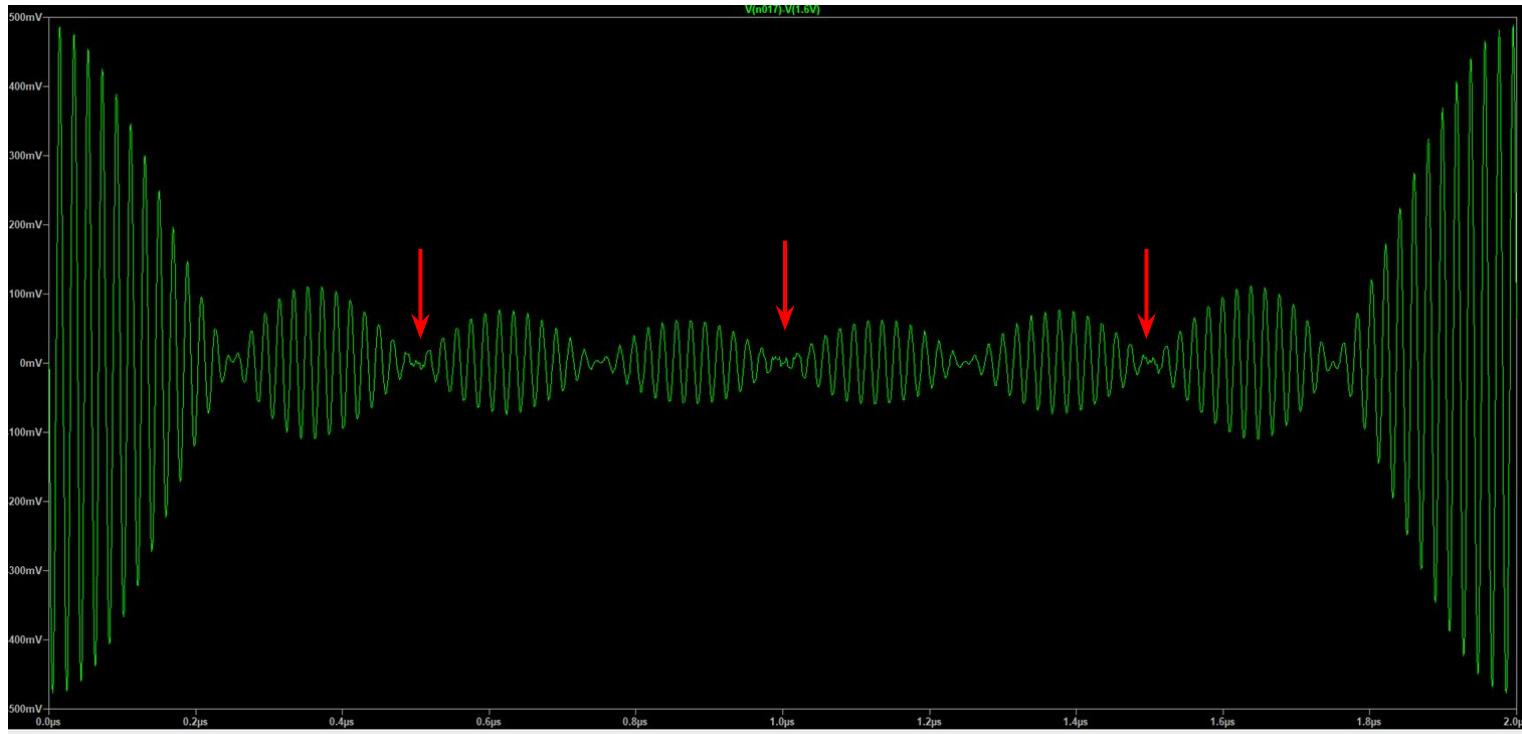
*Frequency response of  $I_{out} / V_{in}$   
Flat response in frequency band of interest is ideal to preserve signal integrity*

# LTS spice Simulations



8-channel chain  
Voltage sources set at 50 - 53.5 MHz

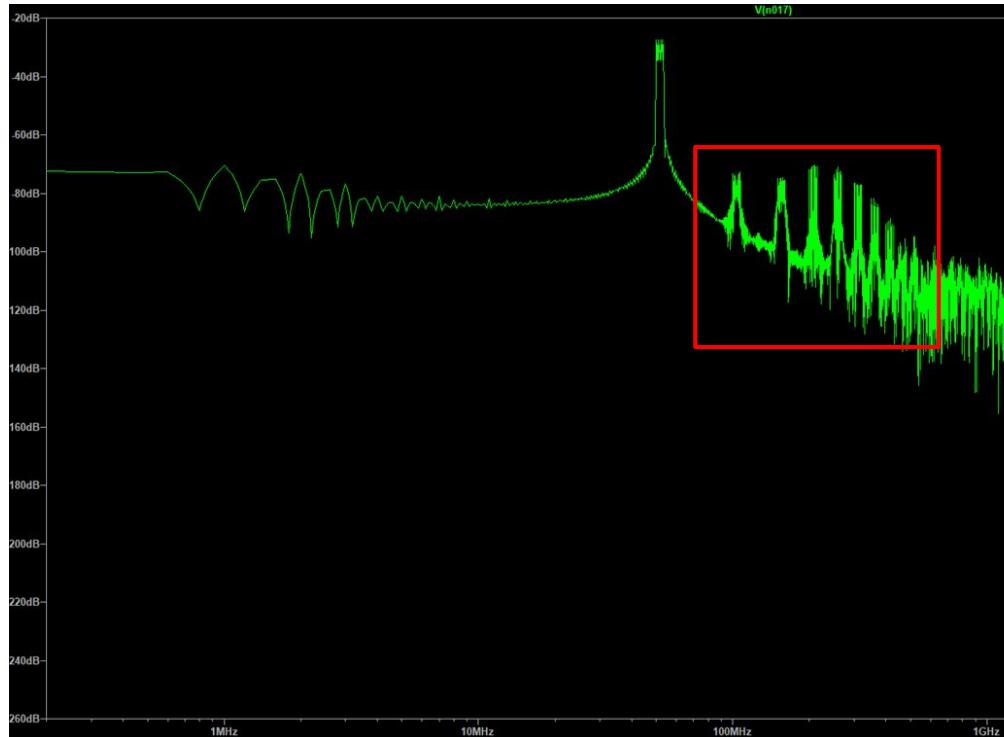
# LTS spice Simulations



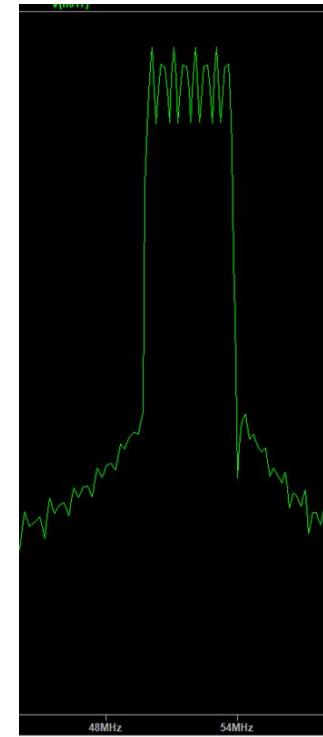
Probed voltage drop across  $R_{load}$

1 Vpp,  $\frac{1}{4}$  attenuation of the ideal aggregate waveform, **much better than 120 mVpp,  $\frac{1}{8}$  performance of old design**  
Waveform has minimal distortion, **with some high frequency harmonics**

# LTS spice Simulations



FFT shows *higher frequency harmonics*  
Can be mitigated with a bandpass filter



Peaks of interest

# Outcomes and Future in Hardware

## Outcomes:

- Set up data collection pipeline
- Verified functionality of rev. 1 board components
- Discovered critical issues with inherited design
- Simulated new voltage-to-current buffer design - shows proper signal summation
- Designed rev. 2 board to include new buffer, VCO, and remove experimental components

## Future Steps:

- Fabricate rev. 2 board and verify
- 8-channel chain experiment and acquire data with suitable DAQ
- Pass data to software Rx module to demodulate and extract separate channels

# Outcomes and Future in Software

## Outcomes:

- Transitioned from 36 to 12 channels
- Real-time plotting of demodulated artificial signals
- Realistic modelling of signal non-linearities such as noise
- Overall pipeline is improved: channelization, modulation, resampling

## Future Steps:

- Acquire ADC signals from an 12-channel system using custom board
- Develop a machine learning framework to operate on received signals
- Implement signal quantization without significant loss of information