

Single Channel Aggregation of Multiple Sensors Using Frequency Modulation and Frequency Division Multiplexing

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Executive Summary

Existing ExG (ECG, EMG, EEG, etc.) sensor systems are bulky, expensive, and have a lot of constraints. They are typically not very portable due to the weight of the large batteries and huge numbers of wires needed. Besides the increased weight, these cause a host of other problems, such as motion artifacting resulting in noisy signals, or high power draw from the battery, overvolting and distorting the signals. Both the battery sizes, and the number of wires required, can be attributed to the very large number of analogue to digital converters these sensor systems employ. Since there is an individual ADC per each electrode, this results in a lot of wires and a lot of cost. These ADCs are also very power hungry and therefore need large batteries to operate for long periods of time, further increasing the weight. To overcome these problems, this paper suggests the use of frequency modulation to chain the signals together using custom hardware, and then split and demodulate them in software for further processing. This way, the aggregate signal can be passed onto a single analogue to digital converter, significantly decreasing the power consumption and weight of the overall system, and improving the signal quality and portability. We started off this project by inheriting the existing hardware and software from our mentors. Both of these had significant issues that needed to be resolved for our approach to work. On the hardware side, we first started off with building our data collection pipeline. We learned that we can get 3.2 seconds worth of data saved onto the FIFO register on our DAQ board and then extract it and save it in binary for processing. After the data collection pipeline was built, we needed to confirm our approach with off the shelf VCO boards that have a similar design to ours. To test this, we modulated 3 signals 124.5, 125.5, and 136.5 MHz and then chained them together. We observed that the band did in fact widen with 200 kHz guard bands in between. We noticed that our DAQ was attenuating relevant frequencies and deduced that it was an issue with our buffer design. We implemented a modified version of a Howland current pump to sum all the modulated signals and create an aggregate signal. We simulated this using LTSpice and found that this attenuated signals half the amount of the original buffer design. On the software side, our main accomplishment was the conversion of the Vitor TX/RX system from 36 channels at 2MHz to 12 channels at 8MHz, as well as modifying the TX module to simulate quantization. The TX module is only used for testing. It is used to simulate realistic ExG signals which are then summed together to replicate our hardware and then sent to the RX module for separation and demodulation. On the RX side, we found that inputting quantized signals significantly reduced the signal to noise ratio of our demodulated signals. Without quantization, our SNR reached well over 140 dB while it barely reached 120 dB when quantization was introduced. We also found that if we used 16 bits for the signals instead of the 12 bits our ADC used, we could get to just below 140 dB. By further increasing either the bit depth of our signal, or the frequency granularity, we should in theory be able to reach higher levels of SNR, although this remains to be tested.

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1 Introduction

Electrocardiography (ECG), electromyography (EMG), and electroencephalography (EEG) signals are a class of measurable biopotential data that record heart, muscle, and brain activity, respectively. Typically, these general-purpose ExG signals are collected via electrode-skin interfacing on the site of interest. Collection of these signals are of immense importance to biomedical diagnostics, clinical research, and healthcare. As a result, there is considerable interest in developing high-fidelity acquisition systems that also meet a host of other constraints, such as robustness to motion/environmental artifacts during collection, power consumption, and cost of manufacturing. In this project, we have developed an ExG collection solution that enables robust acquisition of ExG signals, while maintaining a low power requirement for ambulatory application. By leveraging frequency modulation (FM) and frequency division multiplexing (FDM), our solution can aggregate ExG signals from n electrodes onto a single analog wire, which can be fed into a single ADC. This stands in contrast to traditional systems, which typically have one wire plus ADC per electrode. Thus, we have enabled considerable power savings and a wearable form factor by cutting down on wire and ADC count.

In a healthcare context, long-term collection of ECG signals play an important role in detection of irregular heart symptoms such as arrhythmia, which is a major indicator of cardiovascular diseases. This means that early detection of these fatal risks has the potential to prevent millions of deaths annually, seeing as cardiovascular diseases (CVDs) are the leading cause of death globally, accounting for 32% of all global deaths [2]. However, acquisition of these signals should be *in situ* to facilitate the most accurate diagnosis, requiring a need for acquisition outside of the lab/clinic. Thus, there arises a need for wearable sensors.

However, portable solutions for long-term, ambulatory collection of biopotential data are generally constrained by either low-fidelity signal acquisition, or high power draw from a battery, limiting the collection period. Motion artifacts are typically the most detrimental to signal quality, as they can saturate the front-end circuit, losing the micro-volt level information that ExG signals operate on. On top of this, cumbersome form factors due to increased wire count can induce even more motion artifacts via structural inertia. Thus, robustness against these factors is achieved by having a sufficient dynamic range, allowing these artifacts to be removed in digital post-processing while preserving the signal level information.

Unfortunately, dynamic range and power tend to trade-off unfavorably as well. Power consumption of traditional systems are generally dominated by their ADC count. Many solutions [10] [13] targeting wearable application may have power requirements suitable for all-day usage with sufficient battery, but their dynamic ranges (around 80 dB) are just shy of clinically useful. Minimizing ADC count thus is a feasible solution to maximize power efficiency.

On top of this, ADCs are one of the most expensive parts of this data acquisition pipeline, which means there is an economic motivation to cut down on number of ADCs. In clinical and research settings, EEG brain-wave recording devices have the highest density of recording electrodes placed on the skin, which can reach 256 electrodes per subject in some applications [5]. In the traditional one-wire-per-electrode paradigm, this can quickly pose a financial burden.

Thus, this project focuses on development of an ExG acquisition framework that addresses these major limitations. Using FM-FDM, analog signals from multiple electrode channels can be aggregated onto a single wire. This has the advantage of both: (i) lowering system inertia via reduced cable count (leading to fewer motion artifacts) and (ii) potential savings in power consumption (due to the ADC count being independent of the number of sensors) without compromising dynamic range.

2 Technical Background

Typical ExG sensor signals exhibit a maximum bandwidth of 500 Hz with an amplitude level within the micro to millivolts range [14][1]. However, due to factors such as electrode-skin static charge and motion can cause anomalous peaks of up to 100 mV, distorting readings. On top of that, in a multi-channel system which is more commonly seen, electromagnetic interference between wires creates crosstalk, amplifying the aforementioned issues. Hence, a single-wire system will mitigate motion artifacts in signal readings as well as minimize power consumption and form factor, ensuring a more comfortable and natural experience for the human subject.

Frequency modulation (FM) operates on controlling a signal's frequency to communicate some information, as opposed to amplitude modulation (AM) which controls how wide the signal's swing is. In the realm of software, this is the trivial task of feeding signal data into the frequency parameter of a sine function. However, translating this process to a real signal requires specialized hardware, namely an oscillator. Fundamentally, an oscillator is an inductor-capacitor (LC) circuit that utilizes positive feedback to maintain a persistent, repeating behavior, seen as an output voltage or current swing [3] - typically this is an output square clock or a sinusoidal signal, the latter of which is relevant to the project's scope. The properties of the sinusoid, such as frequency and amplitude, can be manipulated via the values of the inductors and capacitors. In our case, we are using an off-the-shelf oscillator, the frequency of which can be changed according to the value of an input voltage - in other words, this is a voltage-controlled oscillator (VCO).

The voltage input of the VCO is tied to the low-frequency ExG signal, and the output is an FM signal centered at some frequency. The result of N VCOs summed together is an aggregate signal with multiple frequency bands, each encoding a channel's unique signal. This can be visualized in the frequency domain via spectrum analysis that shows N bands next to each other with a sufficient guard band in between to ensure no two channels interfere.

Proper selection of a data acquisition system (DAQ) is important to capturing the aggregate signal without loss of information. According to bandpass sampling theorem [**bandpass**], the minimum sampling rate required is twice that of the total width spanned by the frequencies of interest. This is in contrast to Nyquist sampling theorem which states that the minimum is twice the absolute maximum frequency. In the lens of hardware, bandpass sampling enables

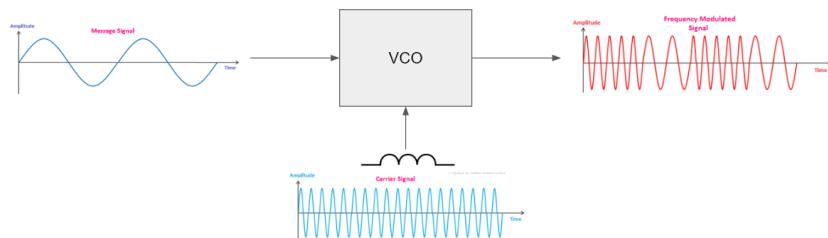


Figure 2.1: Frequency modulation of a low-frequency signal using a VCO.

lower sampling rates, a specification associated with DAQs of lower cost and power consumption. However, one must still be wary of the secondary requirement of wide intrinsic bandwidth, up to the absolute maximum frequency [**bandpass**] - this is to ensure that the signal received is not being attenuated by analog components such as the connector, cable, or parasitic capacitances. Unfortunately, most commercially-available DAQs operate on the assumption of Nyquist sampling and thus typically implement a low-pass filter that attenuates above the sampling frequency. Our selection of Measurement Computing's USB2020, despite the ample 20 MS/s sampling rate, proved to be insufficient due to the intrinsic 17 MHz hardware bandwidth.

Assuming the chosen DAQ satisfies both the sampling rate and intrinsic bandwidth criteria, the acquired digital signal will now contain a digitized version of the original FM signal shifted to baseband. Figure 2.2 provides a visual explanation of bandpass sampling. The red spectrum represents the original signal, and it contains frequencies well above the Nyquist rate ω_s . Sampling the analog signal produces copies of its spectrum shifted by multiples of the sampling frequency. As can be seen in the visual, if the sampling frequency is large enough to contain the entire spectrum of the original signal, then we are able to recover the full spectrum without aliasing at baseband. From this digitized signal the original sensor signals can be individually recovered using a three step process of demodulation, channelization, and resampling. The precise details of FM demodulation are beyond the scope of this report, so we will take for granted that various implementations for FM demodulation exist (such as Matlab's `fmdemod`). The next step, channelization, separates each channel into a separate signal by passing the demodulated signal through a series of filters to which split the signal into individual channels. The final step resamples each channel down to around 1KHz as the sensor signals themselves never exceed 500Hz.

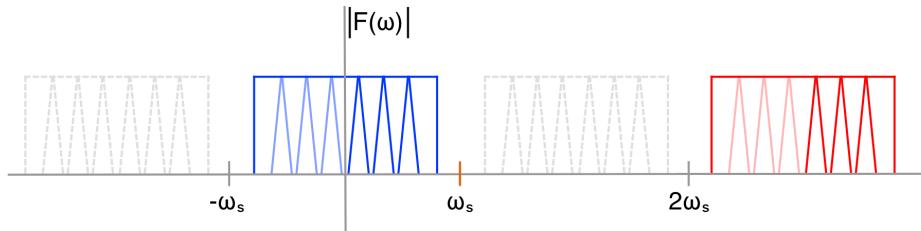


Figure 2.2: (a) Red - Spectrum of original signal, outside of sampled spectrum
 (b) Gray - Copies of original spectrum, outside of sampled spectrum
 (c) Blue - A copy of original spectrum, within sampled spectrum

3 System Design

3.1 Hardware System Design

Our active electrode design needs to be modular in order to be scalable to N channels. In that vein, each PCB board will have an input and output, enabling a daisy chain system. Not only do the I/O's conduct the aggregate signal, but they also must propagate power nets: ground, Vcc, and electrode reference. Lastly, since we are working with an ExG signal, the interface between the sensor and board must be somewhat universal, hence we've chosen to both include a button connector for ECGs, a 3.5 mm audio jack, and several SMA connectors to interface with signal generators and oscilloscopes for testing purposes.

Focusing more on the signal chain of each active electrode, the raw ExG signal, roughly 5 mV peak-to-peak, must be amplified to suitable levels at which the VCO can take in to produce an FM signal. Furthermore, the final stage of the signal before the aggregate bus should be in the form of the buffer to perform two functions: protect each channel from current backflow, and facilitate signal summation, either through voltage or current mode. In the end, we've chosen to design a custom voltage-to-current buffer for current-mode summation after discovering issues with a unity-gain buffer.

3.1.1 Amplification Stage

For amplification of the signal, we have chosen the LT1168 op-amp [6] because of its excellent noise and bandwidth performance suitable for our application. The attribute of low noise is especially important when working with the small 5 mV ExG signal. AC coupling capacitors before and after the op-amp allows biasing to middle voltage since we are operating with one supply. Moreover, the presence of do-not-populate (DNP) points allow experimental configurations post-fabrication - in other words, we can choose the source of the signal, either from the button or SMA connector.

The gain of the op-amp is set via R3. In this case, a value of $5.9\text{k}\Omega$ will give a gain of 10, according to the op-amp's datasheet [6]. The manufacturer also suggests a high-frequency bypass capacitor at the power supply to improve stability.

Once the signal has been amplified by a factor of 10, this puts the amplitude to around 50 mV, suitable to be fed into the VCO.

3.1.2 VCO Stage

The input of the VCO is selected similarly to the amplification stage - optional DNP points can use the output of the previous stage or input from a 3.5mm audio jack. The VCO we have chosen is the Maxim 2605 [7] because of its excellent phase noise performance and low power consumption. According to the datasheet [7], this VCO operates at a frequency range from 45 to 70 MHz. Thus, to maximize the real estate taken up by N channels within this spectrum, the fixed frequency of the VCO should be in the middle, around 58 MHz. This frequency is set

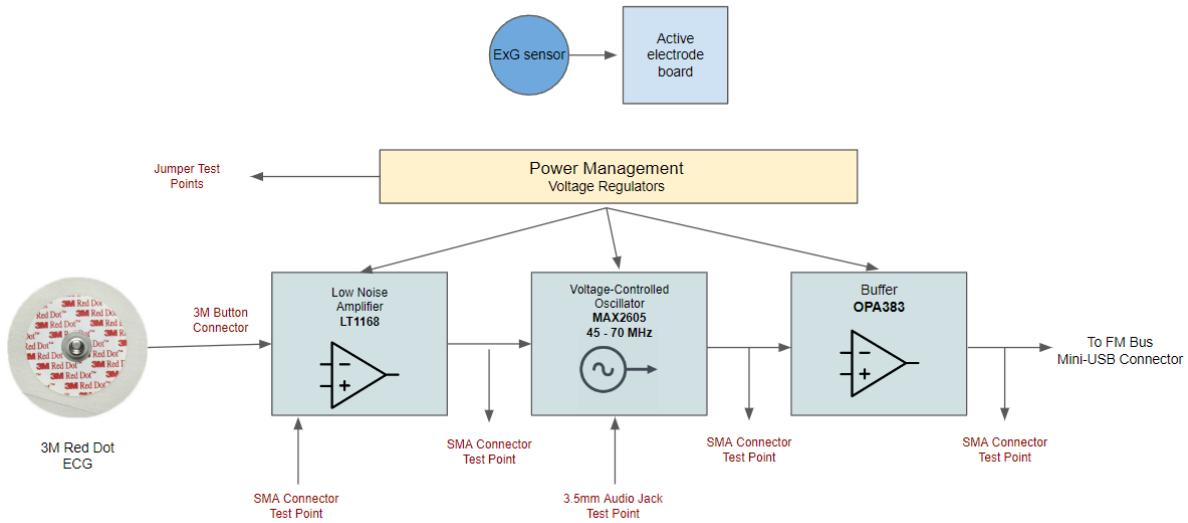


Figure 3.1: High-level overview of an active electrode board.

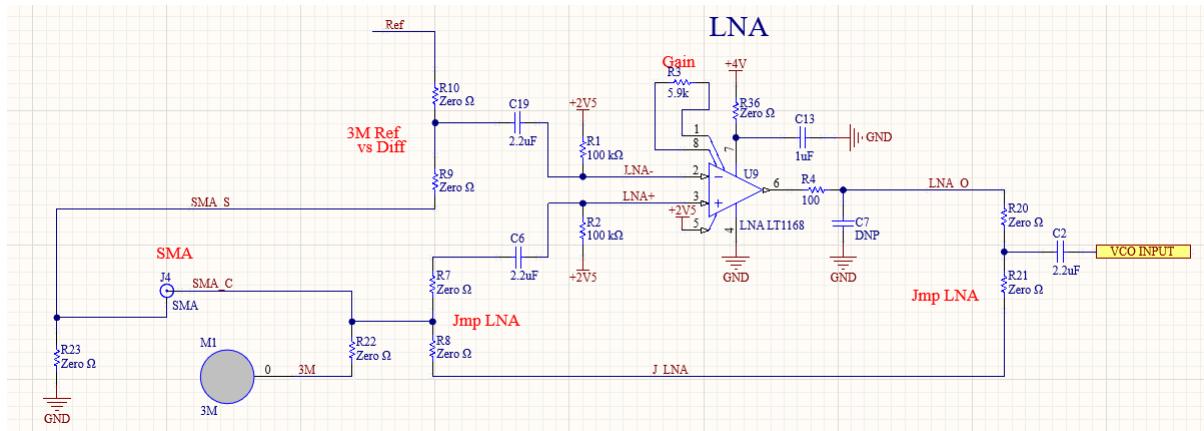


Figure 3.2: Amplification stage schematic.

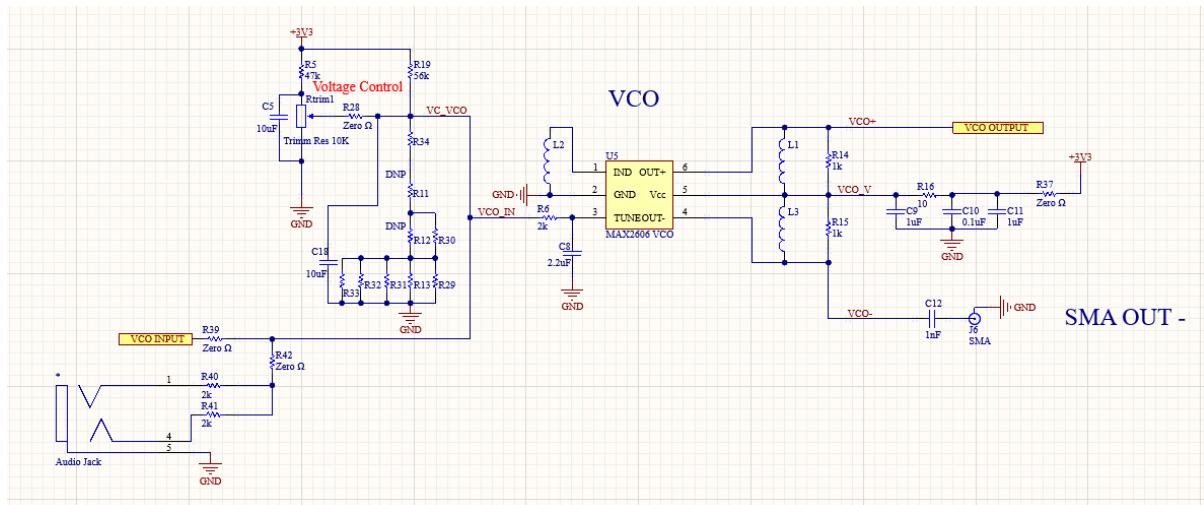


Figure 3.3: VCO stage schematic.

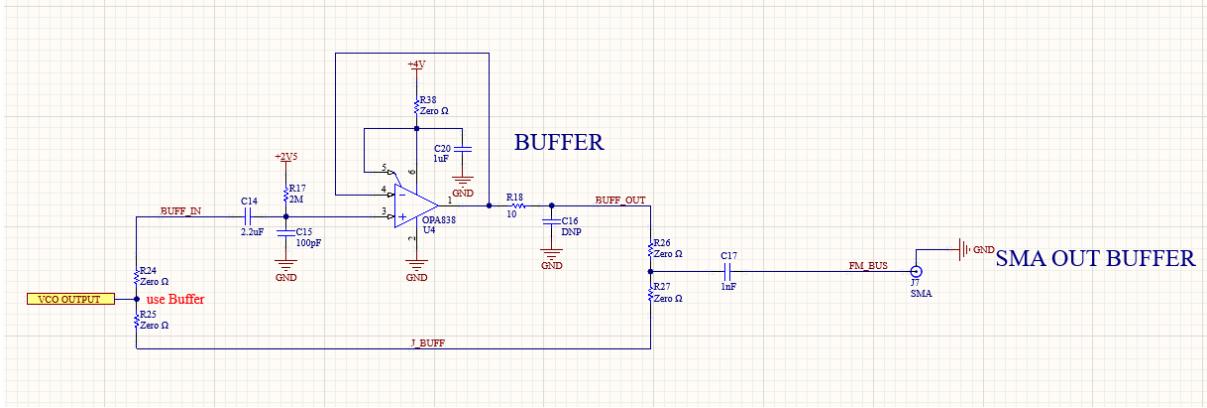


Figure 3.4: Unity-gain buffer stage schematic.

with high-Q inductor L2 value of 1100 nH, chosen based off the datasheet frequency/inductance tuning graph.

By hard setting a frequency via inductor L2, there remains only one degree of freedom to choosing each channel's center frequency - the DC bias voltage. By creating a resistor network and including a trim potentiometer, the tuning input voltage of the VCO can be finely biased to a frequency above or below 58 MHz.

The differential open-collector output of the VCO is pulled-up to Vcc via inductors as per the manufacturer's suggestion. Subsequently, each end is passed to either an SMA connector output or the next stage which is the buffer.

3.1.3 Unity-Gain Buffer Stage

The last stage before aggregation is the non-inverting unity gain buffer. The OPA838 [9] was chosen for its good bandwidth performance and compliance with the 500mV peak-to-peak output of the VCO. The design follows similar patterns seen in the previous stages: decoupling capacitors for middle voltage biasing, and bypass capacitors to filter out high-frequency noise spikes in the power supply. The output is fed to an SMA connector.

3.1.4 Alternative Voltage-to-Current Buffer Stage

Later experiments will show that the unity-gain buffer attenuates the aggregate signal proportional to the channel count. This was both verified experimentally and in LTSpice simulation. As a countermeasure, we've designed a voltage-to-current buffer that mitigates this attenuation by switching to current-mode summation. Moreover, the input is differential to utilize the full-ranged swing of the VCO.

The design is based on the Howland current pump [4] that takes advantage of op-amp feedback behavior to maintain constant current across a varying resistor - in essence, it is a current source. Our design turns the input to the differential, and also biases to middle voltage to work with single-supply op-amps. Additionally, a unity-gain buffer at the output blocks off feedback current, suppressing output current errors.

In simulation, we have discovered that the OPA838 op-amp attenuates current significantly at the frequency ranges of the MAX2605. A solution was to choose a faster op-amp, Texas Instruments' THS4304 [11], with a flat response in gain and phase within the frequencies of interest.

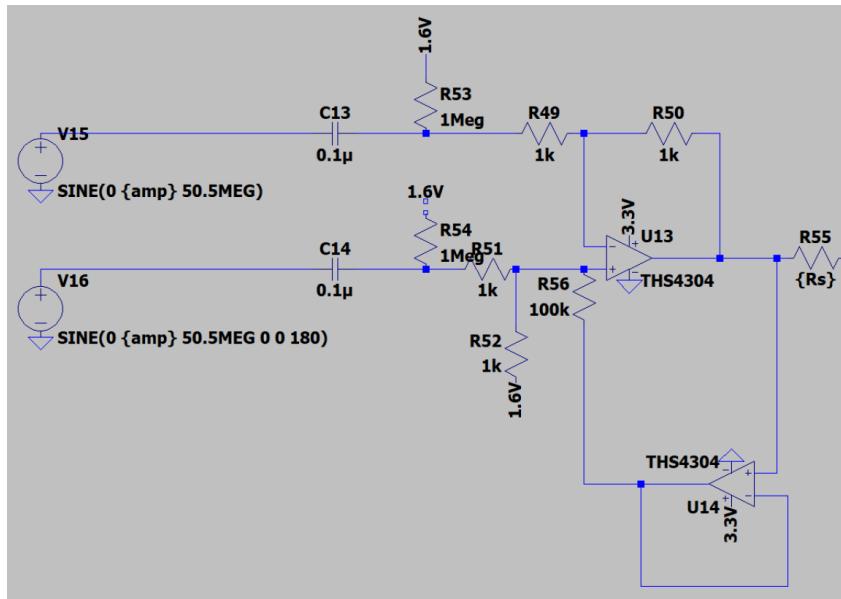


Figure 3.5: LTSpice schematic of differential voltage-to-current buffer.

3.1.5 Power Supply and Peripherals

To power the ICs of each stage, we've chosen to provide three levels of voltages: 2.5 V for middle-voltage biasing; 3.3 and 4 V for single-supply op-amps and VCO. These voltages were regulated via low-dropout voltage regulators, the specific models of which are not important and are chosen based on availability and maximum supply current. For verification purposes, jumpers are connected to each power net to be easily probed.

The boards will be chained together via mini-USB connectors.

3.1.6 PCB Design and Fabrication

The entire system schematic was laid out in Altium CircuitMaker, and the PCB was subsequently generated using the convenient manufacturer part search to import pre-made footprints. The 1st revision custom board measured 45 x 50 mm, and was composed of four signal and three dielectric layers. Both the top and bottom layers featured a ground pour for better protection against EMI. Power planes connected to the three LDOs are polygonal pours on the middle layers for IC easy access. Lastly, the button connector is placed on the bottom layer for direct connection to an electrode, allowing the entire board to be mounted on the human body. Through-holes are included for mechanical standoffs to keep the board floating within an enclosure.

PCB manufacturing files were exported and sent to PCBMinions to be quickly fabricated, leaving the populating process for us to complete.

3.2 Software System Design

3.2.1 Module Description

The software system consists of two main components - the TX module and the RX module. The TX module is designed to generate a variety of test signals that are used to validate the RX module. The RX module is actually used in production and is responsible for taking as input the FM modulated signal outputted from the DAQ and returning the preconfigured number of

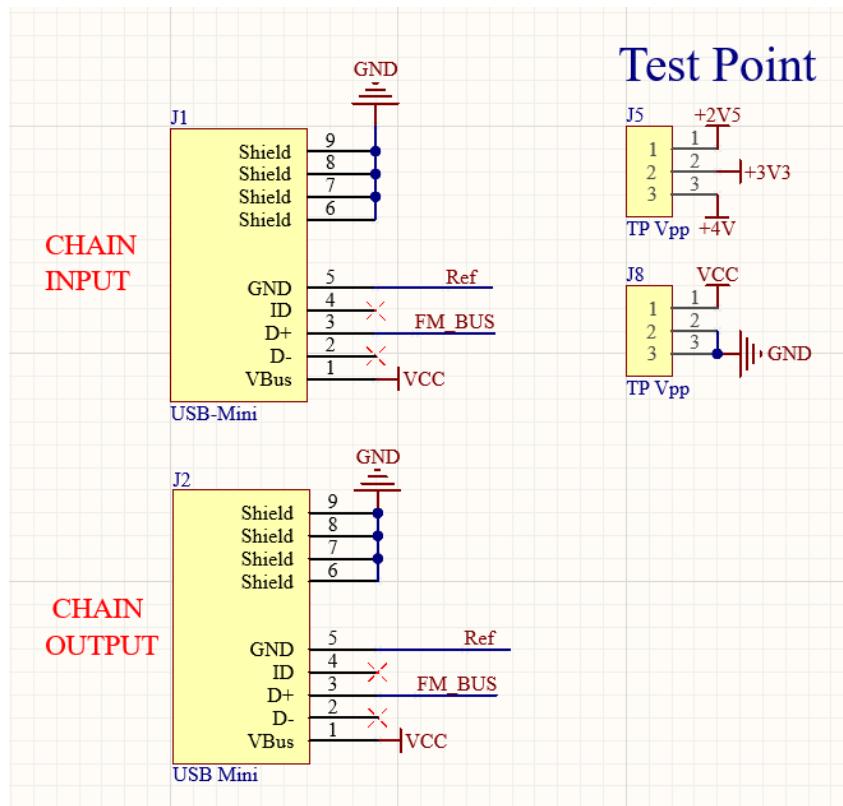


Figure 3.6: Peripherals schematic.

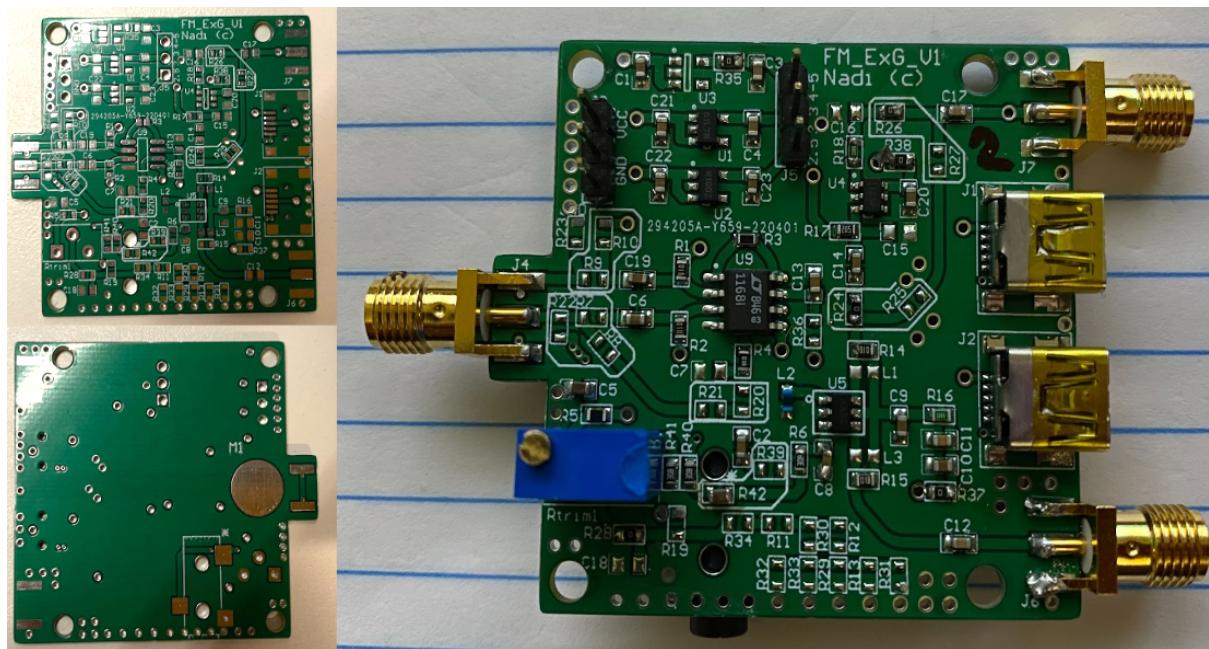


Figure 3.7: PCB pre and post-population.

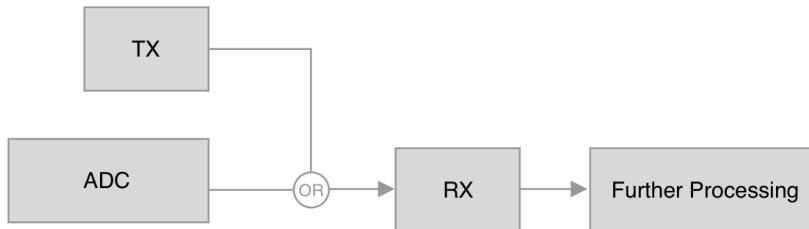


Figure 3.8: Software Data Flow

channel signals. Because of limitations to the hardware resulting in difficulties acquiring real signals, all testing, simulation, and validation happened with these two modules.

The number of channels, sampling rate, FM frequency deviation, number of quantization bits, and a number of other important system parameters can be specified to test a variety of configurations. Once these are set, the TX and RX modules will use these parameters to perform modulation/demodulation. Currently, The TX module generates sinusoidal test signals for each sensor at different frequencies between 0Hz and 500Hz for each sensor. While this is not strictly realistic, this allows us to validate the RX module across all amplitudes of signal and across all frequencies of interest which ensures that RX will work properly with the sensor signals. The TX module is also capable of simulating quantization of the final FM signal in order to simulate the non-ideal effects of the DAQ.

3.2.2 Software System

At the conclusion of this project, the software system converged to a 12 (8 useable channels hence the 8 channel name, with 2 sacrificial channels on each side of the middle 8) channel design with a 8MHz sampling rate with 12 bits of quantization. The 12 channel/8MHz combination was chosen as a balance between the number of channels which we wish to maximize and the bandwidth per channel which we also wish to maximize (up to a certain point). The main considerations for the choice of these parameters are the maximum sampling rate of the chosen ADC and the minimum required bandwidth. Due to limitations of off the shelf components, we needed to devote at least 150KHz per channel as any less we were unable to reduce the bandwidth of the channels in hardware any less. We decided to add another 150KHz of guard band per channel to further ensure that the channels do not interfere. While our ADC is capable of achieving 20MHz, we chose to use 8MHz as this is the maximum sampling rate that the ADC is capable of achieving in real time. Combining these metrics together (8MHz, 300KHz / channel), the closest combination is a 12 channel system at 8MHz which results in 333KHz per channel. Figure 3.8 shows the overall software module level diagram. The TX is meant to mimic the ADC and plug right into RX, and the output of RX will immediately (either in realtime or immediately after collection) be sent along for further processing.

4 Results

4.1 Data Acquisition Pipeline

We interfaced with the USB2020 DAQ via Measurement Computing's Universal Library [12]. According to the DAQ's user manual, there is an onboard 64 MS-capacity FIFO on board. With the sampling rate maxed out at 20 MS/s, we can achieve a total acquisition burst of 3.2 seconds, more than enough time for our purposes. On the other hand, we can achieve a max real-time transfer rate of 8 MS/s - this can potentially be used for a future plan of having a real-time demodulation interface. To initiate acquisition and read from the FIFO, UL virtual instrument (VI) blocks were used to set the voltage range and sampling rate as pictured in the LabVIEW block diagram. The front panel includes waveform displays to verify the integrity of the read signal, as well as controls to change collection parameters. It is worth noting the "Write to Measurement File" VI which is configured to output lightweight .tdms binary files. Subsequently, a Python script that leverages the npTDMS package [8] parsed the file to both plot signals and verify the 12-bit depth (this was done by observing 4096 unique values between -1 and 1).

4.2 Proof-of-Concept With MAX2606 Evaluation Board

In parallel with the fabrication of our 1st revision board, we performed a three-channel experiment with off-the-shelf MAX2606 evaluation boards of similar design - in common with our design were a 3.5 mm audio jack input, and SMA connector daisy-chain I/Os.

In order to verify the functionality of the VCO, we fed line-level music into the audio jack, and attached an antenna to the output SMA connector. Subsequently, we placed a handheld FM radio nearby, tuned to the VCO's center frequency obtained by tuning the potentiometer and

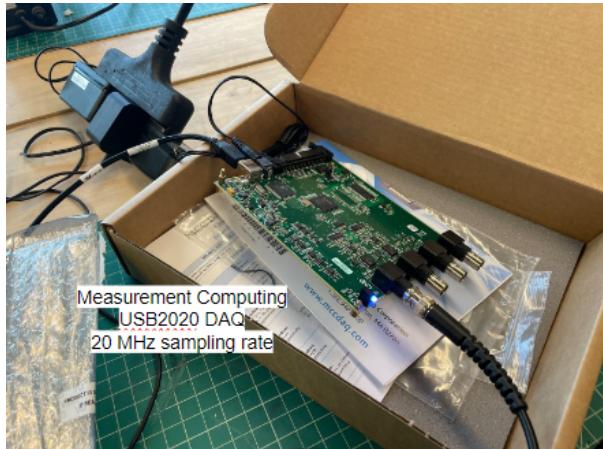


Figure 4.1: USB2020 DAQ.

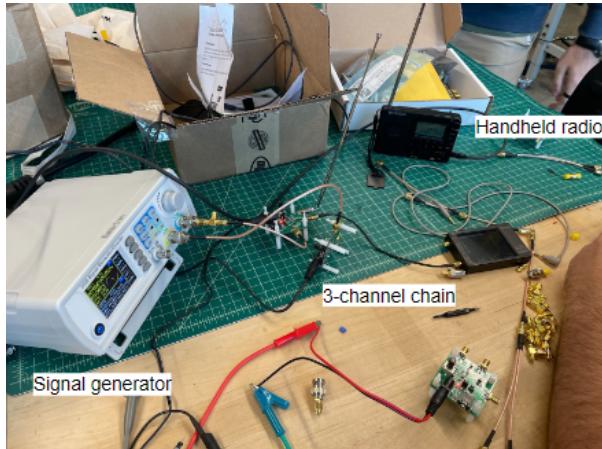


Figure 4.2: Experimental MAX2606 evaluation board setup.

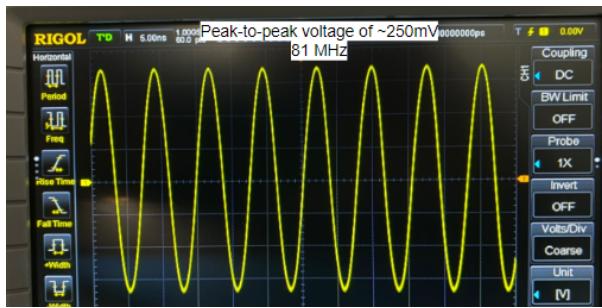


Figure 4.3: Oscilloscope reading of one channel's output to a 0 V message signal, center frequency tuned to 81 MHz.

checking with a spectrum analyzer. Hearing music was indicative of the VCO working.

Pictured in figure 4.3 is the oscilloscope reading of one channel with a 0 V message signal - we expect a pure sinusoidal output which was the case. Next, we read this output with the LabVIEW interface. Since the DAQ was sampling at 20 MHz, way below the Nyquist frequency, twice 81 MHz, the result is an alias at 1 MHz. It is worth noting that the time domain signal reading was significantly attenuated, a foreshadowing of the later-realized low-pass filter of the USB2020.

When the channels were chained together, spectrum analysis confirms the even placement of each band from 124.5 to 126.5 MHz. When a low-frequency message signal of 40 mV peak-to-peak, representing the amplified ExG signal, was fed into each channel, the bands widened, leaving a sufficient 200 kHz guard band to prevent interference.

Readings from the data collection pipeline were unintelligible and it was concluded that the USB2020 was attenuating at the relevant frequencies. This was confirmed by the datasheet, as well as experiments using a signal generator.

4.3 LTSpice Simulation of New Buffer Design

The modified Howland current pump design was simulated using LTSpice to confirm its current source behavior isolated and in an 8-channel chain. The differential output of the VCO was modeled with two voltage sources of 180 degrees phase difference, yielding a total differential peak-to-peak voltage of 1 V

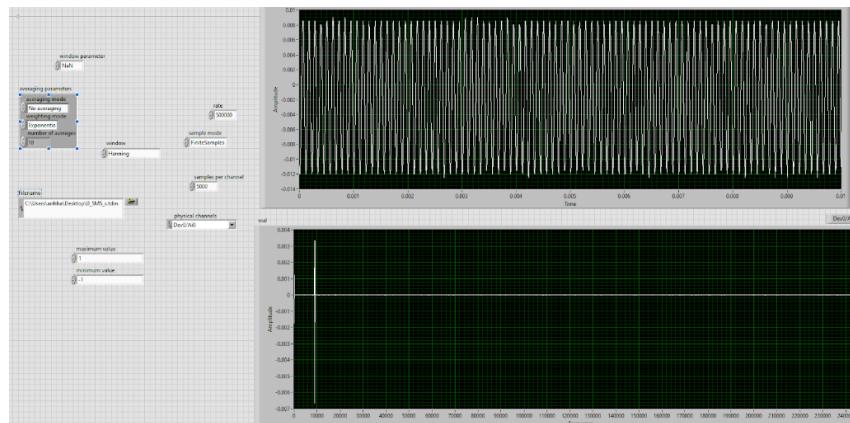


Figure 4.4: LabVIEW interface retrieving data from DAQ's buffer, displaying time and frequency domain plots.

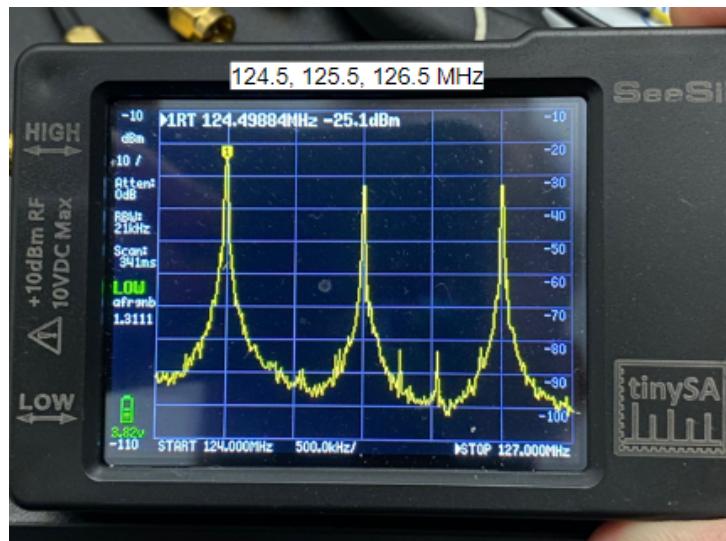


Figure 4.5: Spectrum analysis of aggregate signals of three channels.



Figure 4.6: Widened bands of each channel after low-frequency message is fed.

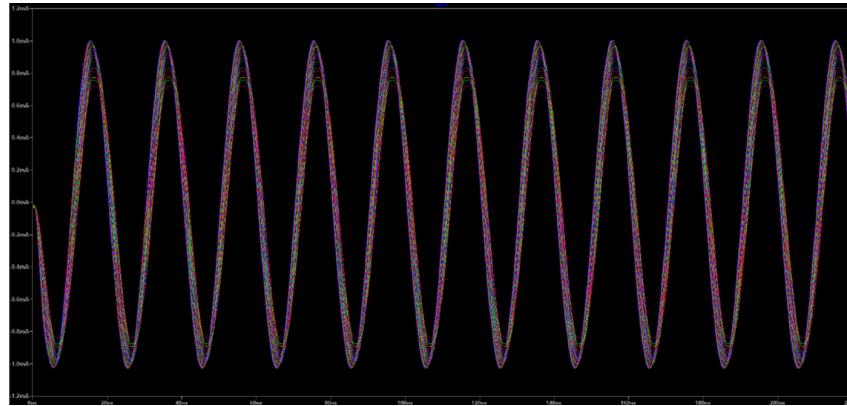


Figure 4.7: Current plot across varying load resistor of one channel.

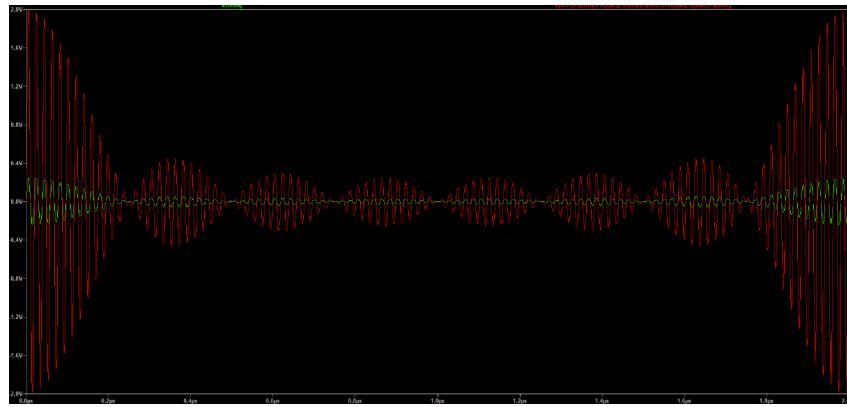


Figure 4.8: Red: plot of ideal summed voltage of 8 channels. Green: simulated summation using unity-gain buffer.

Due to the nature of current-mode summation, a load resistor near the DAQ is required to produce a readable voltage drop. One would expect the highest load resistor value possible to yield the largest voltage swing, according to Ohm's law, for the best digital resolution. However, a sweep of the load resistor from 1 to $1\text{k}\Omega$ exhibits saturation of voltage swing at higher values - moreover, when probing current, it is invariable to the load value, an ideal current source behavior, only within load resistor values from 100 to 400Ω . Thus, a load resistor value of 250Ω was chosen.

An 8-channel system was simulated, with the voltage sources ranging from 50 to 53.5 MHz. The voltage across the load resistor was plotted against an ideal arithmetic sum to visualize attenuation. Additionally, a fast Fourier transform (FFT) was performed to check signal integrity.

To highlight the benefits of our new buffer design, the old unity-gain design was additionally simulated to replicate the discovered real behavior.

In summary, only $\frac{1}{4}$ attenuation was exhibited by the voltage-to-current source design, as opposed to the $\frac{1}{8}$ attenuation of the old design. Furthermore, the individual channels' integrity of the aggregate signal is preserved from the FFT plot, albeit with some high-frequency harmonics appearing - this is mitigated with a bandpass filter, a part of the pipeline anyways.

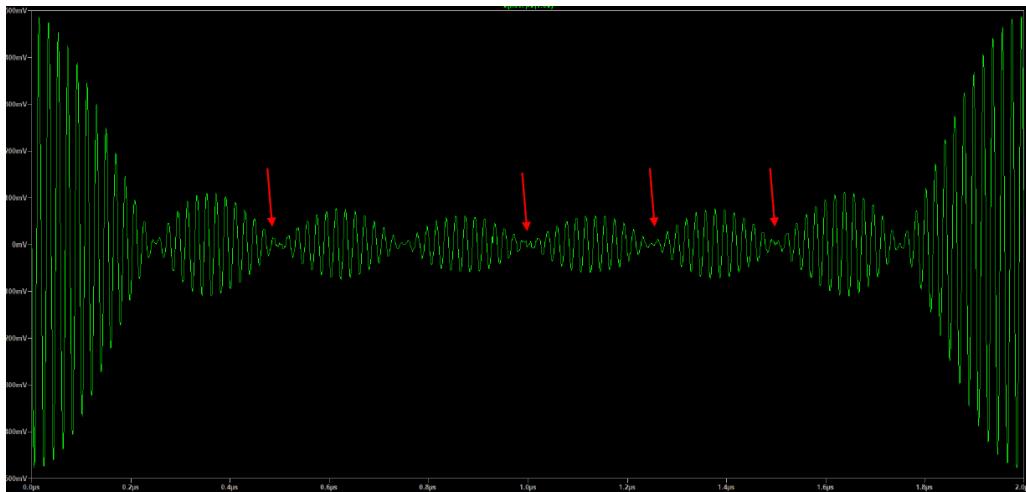


Figure 4.9: Voltage plot of aggregate signal of 8 channels using voltage-to-current buffer, with high-frequency distortion highlighted.

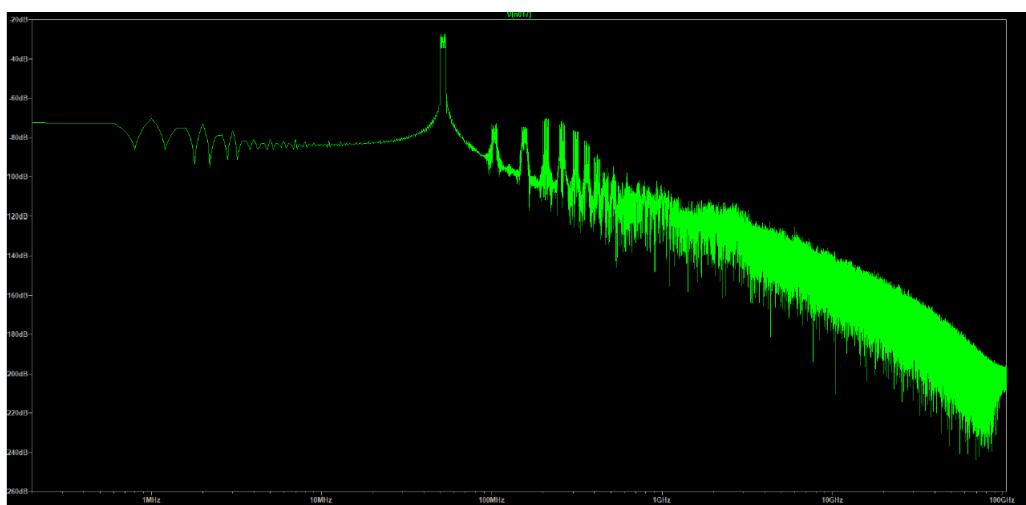
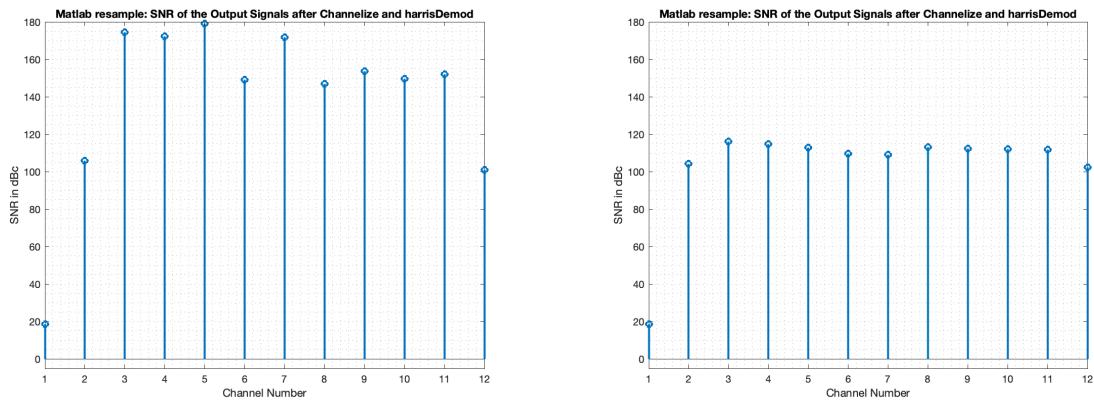


Figure 4.10: FFT of aggregate signal of 8 channels using voltage-to-current buffer, showing peaks at frequencies of interests and higher-frequency distorting harmonics.

4.4 Software Results

The main results of this project on the software side is the conversion of the existing Vitor TX/RX system from a 36 channel/2MHz system to a 12 channel/8MHz system, as well as modifications to TX to simulate quantization. Due to difficulties acquiring a signal on the hardware side, we were unable to verify any of the software modules with real sensor data, so all validation was done with simulated signals from TX. In the final system, we are able to hit the target SNR of 140dB for the 8 usable channels in the ideal system. However, when quantization is introduced, the SNR of all channels drops significantly.

Figure 4.11: Quantization SNR comparison



(a) SNR of each channel without quantization

(b) SNR of each channel with quantization

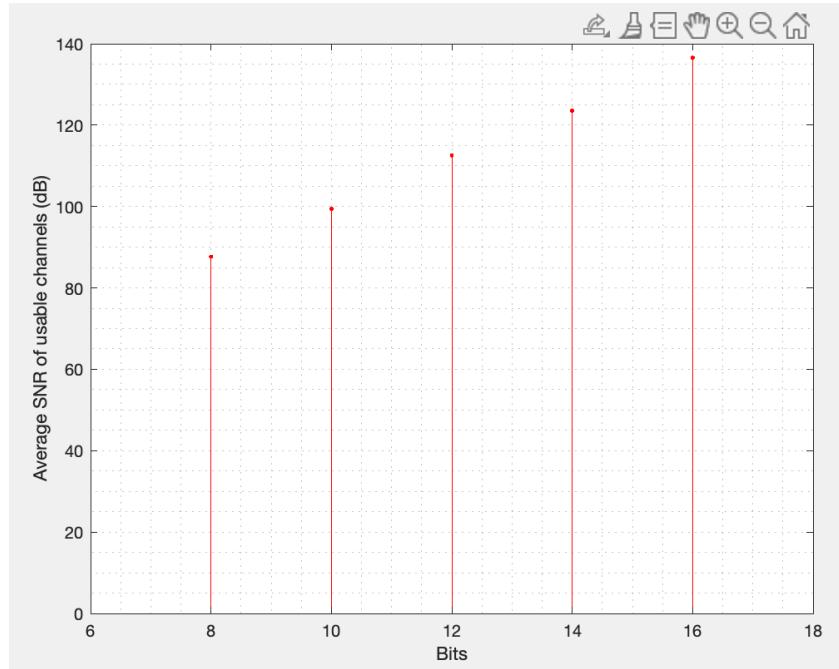


Figure 4.12: FFT of aggregate signal of 8 channels using voltage-to-current buffer, showing peaks at frequencies of interests and higher-frequency distorting harmonics.

Figure 4.11 shows a comparison of between the unquantized signal and the 12 bit quantized signal. Without quantization, the usable channels (middle 8) all reach above 140dB. With quantization, however, no channel exceeds 120dB of SNR. This is insufficient for the final system, so some simulations were performed to determine what a possible solution could be.

Figure 4.12 plots the average SNR of the 8 usable channels vs. the number of quantization bits used. As shown in the plot, even at 16 bits, the average SNR is still just shy of 140dB. However, this small difference can be made up by adjusting the FM frequency deviation. If we cannot increase granularity in the amplitude domain (by increasing the number of bits that represent our signal), we can increase the granularity in the frequency domain by increasing the number of frequencies that represent our signal). This should, in theory, increase the SNR, but more testing needs to be done to determine this. As a result, our recommended next course of action would be to simulate the possible gains in SNR as a function of added frequency range, and determine the best combination of bit depth and frequency swing to achieve 140dB. If increasing frequency swing does not increase SNR but very much, it may be better to switch from 12 bits to 16 bits so that 140dB is achievable without making too many bandwidth tradeoffs.

5 Project Impact

The overall goal of this project is to improve multichannel sensing systems for medical diagnostics and research. In the immediate time frame, the improvements of our project will mostly impact medical research. One of the immediate applications for this work is integration with work from the Center of Wearable Sensors at UCSD to create novel sensing technologies. Another application that comes immediately from our work is to use this system with existing sensors to conduct medical research. The main applications that it has in the medical field, is its vast use in the processing of medical signals, such EEG signals, which can be processed quite effectively, given the current system design.

This project will enable such systems due to three main improvements from our design: reduction in form factor, reduction in power consumption, and increased robustness against motion artifacts. The reduced form factor will serve to improve comfort for the person who is wearing a helmet - like object. As mentioned before, EEG machines - which can use up to hundreds of electrodes at once - are typically implemented on a helmet-like object with wires protruding outward from each sensor on the helmet. This is cumbersome, heavy, but necessary as there needs to be space for all the wires. With less electrodes, a more compact design is achievable with the wires efficiently routed and bundled at the back, but this is still bulky and impractical for regular wear should sensing need to be conducted outside of a clinical setting. With our design, the daisy chainable sensors can all be connected in series on something like a baseball cap with a single wire protruding out the back to the processor to record the data. This enables sensing systems to be more comfortable for the user and allows sensing outside of a clinical setting. This is also where the improved battery life and robustness against motion artifacts comes into play. Currently, there is no good solution to using EEG systems outside of a lab or a clinic, especially for any continuous sensing. In systems with enough battery life to enable all day sensing, the fidelity of the signal is not good enough to eliminate noise from motion; therefore, for high quality sensing, the patient needs to be in the lab. With our approach, this need not be the case. Due to the lightweight nature of our design, the system is less prone to motion artifacts than existing systems. This, combined with the improved battery life, will enable sensor systems to be built for long term, continuous monitoring. The increased comfort resulting from the single wire design will only serve to improve patient experiences when using these sensing systems. All in all, we hope that this project will lead to development of better, more comfortable medical diagnostics systems.

While this project is still in its early development, if this project achieves what it aims to, it could have broad implications for public health and safety, and could also have a significant social and economic effect. For public health and safety, this project would mean much better medical diagnostics for patients with chronic illnesses for which continuous monitoring solutions do not exist yet. For one simple example, there is currently no medical technology to predict or alert a patient to an incoming seizure. With this design however, EEG sensors could be arranged on a baseball cap so that the patient could wear it in their day to day life and be alerted should any strange neurological activity start to happen. This way, the patient can take precautions and place themselves in a safe location before the seizure occurs. This not

only improves the patient's health, but also the public's health as it allows the patient to remove themselves from any situation where their seizure could cause harm to others (such as driving). This is only one application of this system, but one can imagine the possibilities for improved medical monitoring and prevention with this system. In addition, this project could have significant economic effects as it would likely be incorporated in a multitude of technologies - both consumer and medical. With this system, these companies could improve their health monitoring applications and further increase accessibility and availability of high quality health monitoring systems. Overall, this project will lead to significant improvements in public health by improving medical research and diagnostics.

6 Conclusion

In conclusion, we can summarize the overall achievements of the project between the Hardware and the Software side. In terms of the Hardware, the data collection pipeline is set up, therefore the data collection process can be accelerated without running into too many issues. The first version of the board is complete, and the constituent components of the board have been verified. The inherent design of the board had some existing issues, which were later resolved by the steps that we have laid out in Chapter 3 (System Design). We have later removed some of the experimental components in the board and we have included a new buffer and VCO. In terms of the future steps, the new rev. 2 board will have to be verified by the next team that will take on the project. The board must also be verified with a new 8 - channel system and acquire data with a suitable DAQ. On the Software side we have successfully transitioned from a 36 - channel system to an 8 - channel system, thus drastically improving the overall “bulk” of the system. We have implemented simulation modules, such as the real - time plotting of a time - domain and/or frequency - domain signal, which allowed us to have a clear picture of a signal that we would expect to receive from the board. Quantization of the received signal has also been improved to the point where the information loss has been minimized. Finally, the overall pipeline, which consists of: channelization, modulation, resampling has been improved via the steps that we have laid out and described in Section 3.2 (Software System Design). If we consider the final results that were obtained in the project, and what is in store for the future, we can estimate the impact that the project will have. One of the main impacts will obviously be in the medical field, where we can analyze newborn EEG signals to determine hearing loss, biopotential data acquisition, analyzing signals outside of the work environments. The direct impact, which is indeed more tangible is that we reduce the cost of the system development by significantly reducing the weight, and bulk of the system by reducing the number of wires present. In addition to these final improvements, the signal quality is also greatly improved by reducing the number of wires, which in turn reduces the noise that is inherent within the channel.

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