POLYTECH
MARSEILLE

Validation – Date :
A remettre à :
Patrick PUJO
Responsable des PFE,
DGII Polytech Marseille.
Campus Universitaire de St Jérôme
Av Escadrille Normandie Niemen
13397 MARSEILLE Cedex 20
Tel 04 91 05 60 55 - Fax 04 91 05 60 51
E-Mail: patrick.pujo@polytech.univ-mrs.fr

PROPOSITION DE PROJETde FIN d'ETUDES (EFICAS)

IDENTIFICATION du contact GII

Nom - Prénom :

IDENTIFICATION de l'ENTREPRISE

Nom : STMicroelectronics

Adresse : ZI de Rousset – 13106 ROUSSET

http : www.st.com **Tél : 04.42.68.88.00 Fax : 04.68.54.46**

NATURE du PFE ENVISAGE :

Intitulé : Recherche de methode d'estimation de volume de production à risque

Contenu :

Le travail consistera en une etude de faisabilité sur l'evaluation des "wafer@risk" (WAR). Actuellement nous comptons le nombre de plaque de silicium travaillées entre deux contrôles (mesures). Ce comptage peux etre referencé par rapport a une machine de production ou par rapport a une technologie. Ce comptage ne tiens pas compte de l'existance de plusieurs type de parametres ni de l'interaction potentielle entre parametres. Pour l'instant les mesures effectuées sur des plaques de production et les mesures sur plaque de test liees aux qualifications periodique sont prisent en compte de la meme manière sans tenir compte de la signification de la mesure. Cette methode ne nous permet pas de regler nos outils d'echantillonnage par rapport à un rique maximal garanti.

Contact :

Responsable administratif de l'entreprise pour le PFE (Signataire de la convention) **:**

Hélène MONNIER

Titre ou **fonction**Resp. Recrutement

Tél : 04.42.68.81.83. **e-mail :helene.monnier@st.com**

Correspondant technique du PFE : Franck Gasnier

Titre ou **fonction : Engineering data Analysis**

Tél : 04 42 68 5045

e-mail : franck.gasnier@st.com

A qui adresser la convention de PFE ? (nom, service...) **Hélène MONNIER – DRH -**

Contribution au fonctionnement du PFE (forme envisagée, hauteur, conditions à remplir...:) **:**

Cachet de l'entreprise :

STMICROELECTRONICS SAS
ZI de Rousset - Avenue Coq
13790 ROUSSET
Tél. +33 (0)4 42 68 88 00 - Fax +33 (0)4 42 68 54 46
SAS au capital de 46 816 872,04 €
RCS Aix en Provence 414 969 584 - APE 2611Z
Siege social : ZI de Rousset, Av. Coq, 13790 ROUSSET

I D A b s t r a c t - I S S M 2 0 1 0 _ V 4 (2) . d o c

Optimized design of control plans based on risk exposure and resources capabilities - Belgacem Bettayeb[1]

Philippe Vialletelle[2]/ Samuel Bassetto[1]/ Michel Tollenaere[1]

belgacem.bettayeb@grenoble-inp.fr – philippe.vialletelle@st.com

[1] G-SCOP laboratory, CNRS UMR 5272 - [2] STMicroelectronics

[1]46 Avenue Félix Viallet 38031 Grenoble Cedex France

[2] 850 Rue Jean Monnet. 38926 Crolles Cedex France

[1] Phone: +33 4 76 57 43 26 Fax: +33 476574695 [2] Phone: +33 4 38 92 22 90 Fax:

Keywords: Risks, control plan, risk exposure optimization

In high mix semiconductor manufacturing lines, major scraps events are often issued from the growth, the expansion and the release of a bubble of uncertainty about products' health. Even if process control organization is supposed to protect the manufacturing system against these fearsome events, the monitoring of uncertainty is hardly effective operationally.

The numerous data sources and techniques applied today are necessary to master the process at the Angstrom level. However, the connection between production and quality control turns the management of material at risk in the line into a complicated and very often overwhelming task. As material at risks is directly linked to the plant competitiveness, the traditional process control approach has to be strengthened.

FMEA is used as the standard approach to explicit risk in semiconductor manufacturing (see [1]). Nevertheless, in most cases, it is static and control plans adjustments are then driven by capacity limitations or productivity / cycle time improvement campaigns through so called non-value added steps reduction.

Whether defined according to FMEA or not, the control plan is loaded into MES (Manufacturing Execution System) through sampling rules. These rules are based on process frequency (i.e. measure one every ten), on events (Maintenance just achieved, out-of-control just happened, etc), on product or lot characteristics (experiment lot, so called rocket, bullet or ambulance lot) and on some exceptions (Run to run regulation loop, mandatory parameter for reporting, etc). Traditional approaches proposed in most existing MES are limited and valuable alternatives have been proposed as in [2].

In this paper, the limitations of traditional approaches when applied to an advanced high-mix fab are reviewed and discussed and their main related factors presented.

With the aim to provide coherent method for quality control planning that tackles these limitations, the proposed approach (see Figure 1) consists of two stages:

- Stage 1: use the risk based allocation to define a minimum control plan that ensure a certain level of risk during the considered horizon
- Stage 2: adjust the control plan defined in phase 1 by partitioning the remaining (or the lacking) capacity according to a criterion related to process and metrology capabilities. In this phase we take also into account availabilities and capacities constraints of the control resources.

On top of breaking the barriers between control plan and FMEA, we demonstrate that this new risk based approach allows obtaining an optimized control plan that guarantees a justified use of available inspection or control capacities, while limiting the exposure to risk – or in other words, the amount of wafers in jeopardy.

An abstract from the used data model and the tested instance is shown in Table 1 and Table 2. First results obtained, when applying two different approaches of capacity partition, are summarized in Table 3.

Acknowledgments: This work is supported by the IMPROVE ENIAC European Project.

References

[1] A. Mili, S. Bassetto, A. Siadat, M. Tollenaere, "Dynamic risk management unveil productivity improvements," *Journal of Loss Prevention in the Process Industries*, vol. 22, Jan. 2009, pp. 25-34.

[2] C. Mouli, M. Scott, "Adaptive Metrology Sampling techniques enabling higher precision in variability detection and control," *Advanced Semiconductor Manufacturing Conference, 2007. ASMC 2007. IEEE/SEMI*, 2007, pp. 12-17.

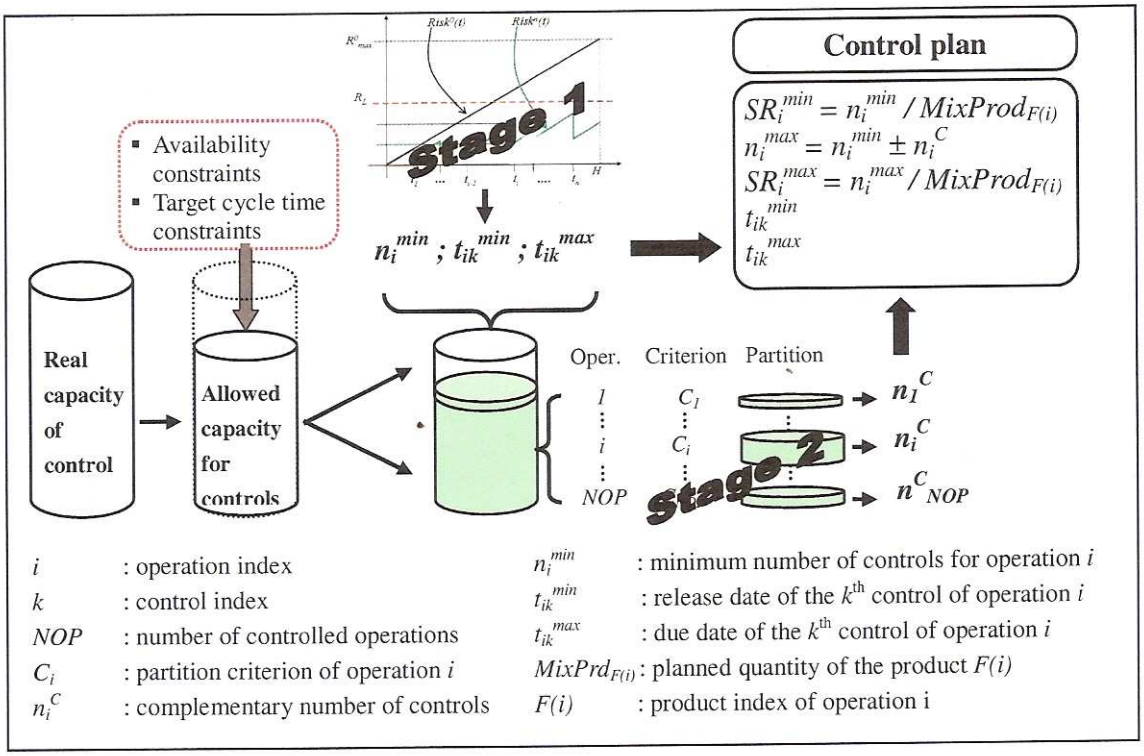

Figure 1. The proposed approach

PRD	OPER	STEP	PTIME	TOOL	DTN	Dspecs	R2R	Recipe	CP	CPM	PROC?	Ptime Eff
A	2300	100	60	CVD	10			cvd1			1	60
A	2300	150	5	SATH	600	2000	N		3,33	10,00	1	5
A	2500	100	60	CVD	10			cvd1			1	60
A	2500	150	5	SATH	1000	1000	N		1,67	5,00	1	5
A	4000	100	60	CVD	10			cvd2			1	60
A	4000	150	5	SATH	400	4000	N		7,27	8,00	1	5
A	4200	100	120	CVD	10			cvd3			1	120
A	4200	150	10	SATH	600	200	N		0,59	2,00	1	10
A	4500	100	60	CVD	10			cvd3			1	60
A	4500	150	5	SATH	10	400	Y		1,18	4,00	1	5
A	4550	100	30	CMP	10			cmp1			1	30
A	4550	150	5	SATH	600	400	N		2,00	4,00	1	5
A	5500	100	60	CVD	10			cvd3			1	60
A	5500	150	5	SATH	10	500	Y		1,47	5,00	1	5
:	:	:	:	:	:	:	:	:	:	:	:	:

6 sigma process	
cmp1	200 avec R2R
cmp2	200 avec R2R
cvd1	600
cvd2	550
cvd3	340
fur1	800

R&R mesure	
cmp1	100
cmp2	120
cvd1	200
cvd2	500
cvd3	100
fur1	300

Table 1. Simplified capacity/capability model (Abstract)

Instance			
Product	**A**	**B**	**C**
Nbop	12	8	17
MixProd	1000	800	1200
OOC%	0,05		
OBJ SAT	75,00%		
Meas. Tools Availability	70,00%		
NB of Meas. Tools	2		

Table 2. Parameters of the tested Instance. Real Meas. Tools Availability reaches 95%, but 20% to 25% is usually reserved to NPW (non Productive Wafer) and engineering tests

Results				
Approach 1: without the first stage	Meas. Tools SAT	74,99%		
	Nbre of controls	6681		
	product	A	B	C
	AVG_SR/oper/product	97%	100%	85%
	AVG_SR/oper	91%		
Approach 2: with the first stage (RL=1)	Meas. Tools SAT	75,00%		
	Nbre of controls	7649		
	product	A	B	C
	AVG_SR/oper/product	83%	86%	91%
	AVG_SR/oper	88%		
Approach 2: with the first stage (RL=20)	Meas. Tools SAT	74,99%		
	Nbre of controls	7929		
	product	A	B	C
	AVG_SR/oper/product	99%	100%	84%
	AVG_SR/oper	91%		
Approach 2: with the first stage (RL=40)	Meas. Tools SAT	74,99%		
	Nbre of controls	7789		
	product	A	B	C
	AVG_SR/oper/product	98%	100%	85%
	AVG_SR/oper	91%		

Table 3. Obtained results.

Optimizing Return On Inspection Trough Defectivity Smart Sampling

Mhamed Sahnoun[1], Philippe Vialletelle[2], Samuel Bassetto[1], Soidri Bastoini[2], Michel Tollenaere[1]

Mhamed.sahnoun@grenoble-inp.fr ; philippe.vialletelle@st.com

[1]INP Grenoble - G-SCOP, [2] STMicroelectronics

[1]46 avenue Félix Viallet 38031 Grenoble Cedex France , [2]850 Rue Jean Monnet. 38926 Crolles Cedex

Phone: +33 -4 76 57 49 15 Fax: +33-4 76 57 46 95

Over the past decade, the control of contamination in process tools has progressively moved from non-product wafers inspection toward on-product measurements. Nevertheless, in high-mix facilities, recipe creation for all products is not possible. Most of these semiconductor fabs use today "high runners" lots that are flagged for defectivity.

As in the line lots can be slow down, stopped, or can overtake each-other compared to their production planning [1], this generates disturbances in the arrival of defectivity information of lots and tools. This is the drawback of this sampling method: the efficiency of the defectivity measurement with respect to information is often under optimal.
In order to quantify this inadequacy we followed the criterion of number of products inspected unnecessarily. The control of those products could have been skipped without any loss in provided information. An algorithm has been designed to identify and monitor this criterion.

The case study described here takes place in STMicroelectronics 300mm wafer fab in Crolles, France. In order to extract tractable models and results, the focus is put on a simple case. It considers one contamination control of one manufacturing tool T (etching tool). The risk of contamination, D, increases with the number of wafers produced. If the control is labeled as "valid", the process tool and all the products processed between the last "valid" control and the current one are validated. Otherwise, actions are triggered on the machine T and the list of lots potentially "non-valid". The various delays between process tool and control device follow a stochastic law as illustrated in Figure 1. In the case study, the analysis of actual historical data reveals that this waiting time follows a gamma law.

The dynamic of the process is illustrated in fig. 2: lot P_1 is processed first and controlled fourth due to buffer behavior. Some lots can be controlled before others that were processed earlier. However, as risk of contamination is an increasing monotonous phenomenon, we assume that if lot P_4 has been released, lot P_1 is also safe and it is not necessary to control it anymore.

The decision to keep or skip inspection of a product lot is based on the value of its risk reduction [2]. This indicator may change each time another lot is inspected. Figure 2 illustrates this evolution. This indicator is then used to sort lots stack to be inspected from lots that induce the highest risk reduction to lots that can be "skipped".
A demonstrator has been built to evaluate the evolution of Wafer-At-Risk based on a historical data (Figure 3). A skip case is illustrated in figure 4. A near-real time prototype (running each 30 min) has been implemented in order to help the operator to select the lots which will be inspected permitting to reduce the risk evaluation.

The algorithm has run over 3 months of production. During that period, a very significant number of lots have been flagged for defectivity measurement. We have observed that up to 35% of the inspected wafers could have been skipped, because they didn't bring any added valuable information.

Acknowledgments: This work is supported by the IMPROVE ENIAC European Project.

References

[1] R. Nurani et J. Shanthikumar, "The impact of lot-to-lot and wafer-to-wafer variations on SPC," *Semiconductor Manufacturing Conference Proceedings, 1997 IEEE International Symposium*, 1997, pp. P69-72.

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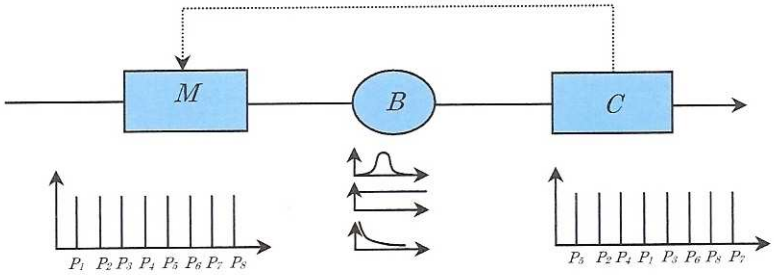

Figure 1 : The production system

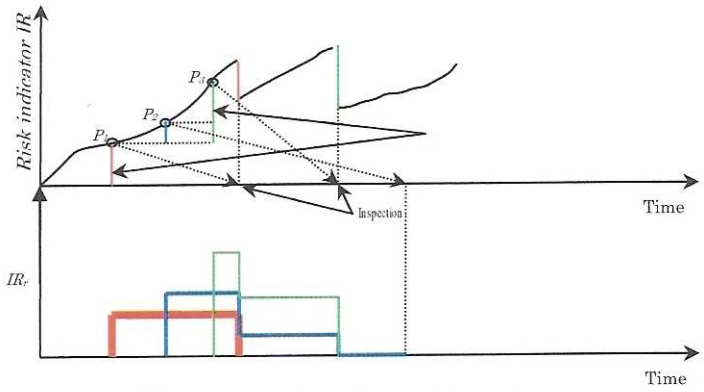

Figure 2 : Risk reduction variation

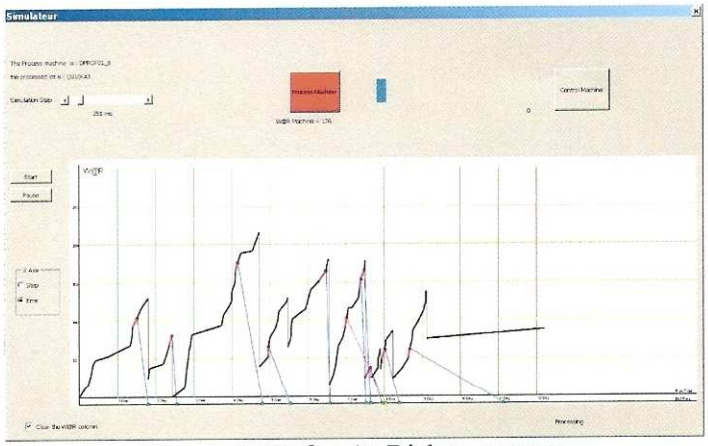

Figure 3: Wafer-At-Risk prototype

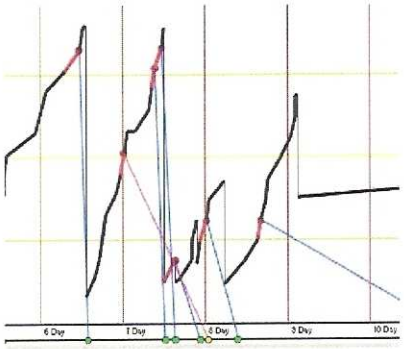

Figure 4: Zoom on case of skip

An approach for operational risk evaluation and its link to control plan

Belgacem Bettayeb[1], Philippe Vialletelle[2], Samuel Bassetto[1], Michel Tollenaere[1]

[1] {bettayeb, bassetto, tollenaere}@grenoble-inp.fr – [2] philippe.vialletelle@st.com

[1]G-SCOP laboratory, CNRS UMR 5272 46 Avenue Félix Viallet 38031 Grenoble Cedex France – Phone: +33 4 76 57 43 26 Fax: +33 476574695

[2]STMicroelectronics, 850 Rue Jean Monnet. 38926 Crolles Cedex France - Phone: +33 4 38 92 22 90 Fax:

Study motivation

Semiconductor manufacturing is characterized by complex and highly sensitive processes. Mastering the variability is one of the most important challenges to ensure the best possible quality of products with high yield performances. Statistical Process Control approaches are today widely applied across the various measurement tools and techniques to attain this objective.

In so called high mix fabrication lines, the traditional approach toward process control has come to its limits. The never ending evolution of technologies and product generations, associated to the numerous data sources and techniques available today to ensure process quality and stability have transformed the mastering of process excursions into a complicated and very often overwhelming task.

FMEA is used as the standard approach to adjust control plans in order to reduce global risk (see [1]). Nevertheless, in most cases, it is static and control plans adjustments are then driven by capacity limitations or productivity / cycle time improvement campaigns through non-value added steps reduction.

Whether defined according to FMEA or not, the control plan is translated into MES (Manufacturing Execution System) through sampling rules. These rules are based on process frequency (i.e. measure one every ten), on events (Maintenance just achieved, out-of-control just happened, etc), on lot characteristics (experiment lot, so called rocket, bullet or ambulance lot) and on some exceptions (Run to run regulation loop, mandatory parameter for reporting, etc). Traditional approaches proposed in most of the existing MES are limited and valuable alternatives have been proposed as in [2].

Description of the approach

In this paper, we propose a method for provisional operational risks evaluation which can support decision making concerning the design of control plans. The method consists of evaluating the risk evolution $R^0(.)$ during a considered horizon (H) without any control. Then, an added value (in terms of risks) could be evaluated for any control plan X (see figure 1).

The risk is computed as the multiplication of the probability of a non-desired event (NDE: failure, drift, etc) by the Potential Loss (PL) if this event occurs. The PL is expressed here by the number of lost items (Chip, wafer or lot). We suppose that when a non-desired event happens, it also impacts the quality of subsequent runs, until its next control (the control means measure and correct if not OK). In this case the PL will linearly increase with the number of runs.

Depending on the time the NDE occurs, the evolution of the PL when no control is planned can be represented as in Figure 2. When controls (measures + corrective actions in case of detection) are planned, the Potential Loss is different because:

- If the result of the planned measure is "OK", there is no need to consider Potential Loss that corresponds to a NDE occurrence previous to the measurement instant (see figure 3).
- If the measure is "not OK", an action is imminent which will "reinitialize or modify" the Probability of the non desired event and the Potential Loss becomes "Probable Loss" or "Proven Loss"

Assuming that we know the distribution of the probability of NDE along the considered horizon H (see Figure 4), the risk evolution function with a control plan X could be computed as following:

$$R^X(i) = \sum_{j=1}^{i} (i-j+1).PL_j^X(i).Pr_j$$

Results and perspectives

Figure 5 presents some experimented examples of risk evolution computation depending on the number of controls and their positions along the considered horizon.

It can be noticed that different control plans have different impacts on risk evolution and different added value compared to the risk evolution without controls. This could be used to define an optimized control plan regarding an objective function related to the added value of a control plan and other manufacturing constraints which will be the aim of our future work.

Acknowledgments: This work is supported by the IMPROVE ENIAC European Project.

References

[1] A. Mili, S. Bassetto, A. Siadat, M. Tollenaere, "Dynamic risk management unveil productivity improvements," *Journal of Loss Prevention in the Process Industries*, vol. 22, Jan. 2009, pp. 25-34.

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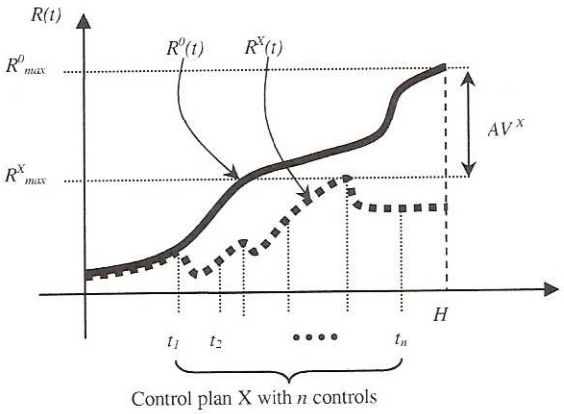

Figure 1. Added value of a control plan

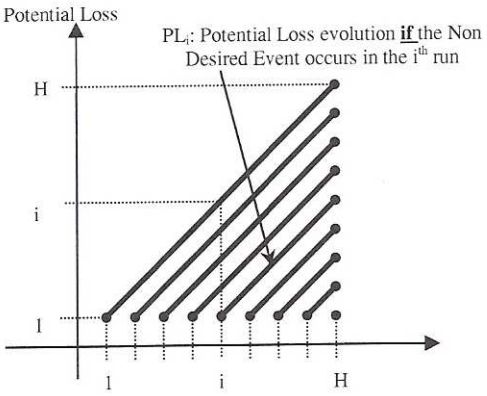

Figure 2. Potential Loss when no control is planned

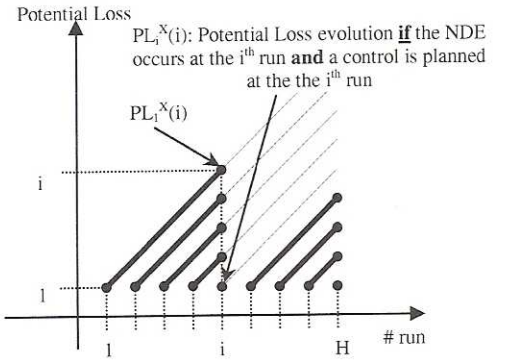

Figure 3. Potential Loss for a control with one control

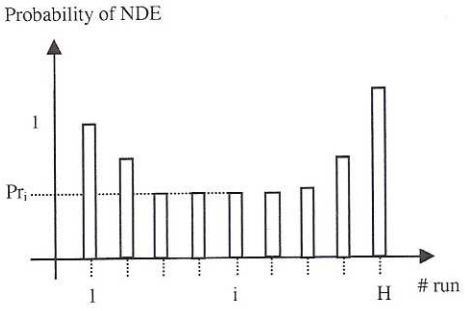

Figure 4. Probability of NDE

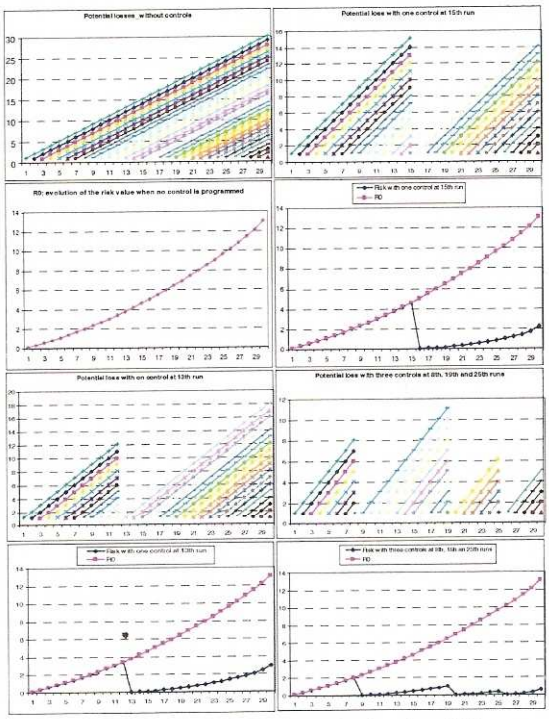

Figure 5. Examples of risk evolution for different control plans

Computation of Wafer-At-Risk from Theory to Real Life Demonstration

Mhamed Sahnoun[1], Philippe Vialletelle[2], Samuel Bassetto[1], Soidri Bastoini[2], Michel Tollenaere[1]
Mhamed.sahnoun@grenoble-inp.fr ; philippe.vialletelle@st.com
[1]INP Grenoble - G-SCOP, [2] STMicroelectronics
[1]46 avenue Félix Viallet 38031 Grenoble Cedex France , [2] 850 Rue Jean Monnet. 38926 Crolles Cedex
Phone: +33 -4 76 57 49 15 Fax: +33-4 76 57 46 95

Keywords: defectivity, skipping, Wafer-At-Risk, Wafer-At-Risk-Reduction

Study motivation:

Over the past decade, control of process tools has progressively moved from bare non-product wafers inspection toward on-product measurements. Nevertheless, in high-mix facilities, recipe creation for all products is not possible. Most of the semiconductor fabs use today "high runners" lots that are flagged for defectivity. Due to non-linearity and variability of the line [1], lots may be stopped, overtake each-other or ignore certain tools. This is the drawback of this sampling method: the efficiency of the defectivity measurement with respect to information is often under optimal.

On the other hand, the measurement equipments are very expensive and fabs are limited in capacity of inspection. Using the sampling method already quoted, we take the risk of controlling some lots unnecessarily. The aim of this study is to evaluate this risk and to propose a solution to optimize the use of control equipment.

The case study described here takes place in STMicroelectronics 300mm wafer fab in Crolles, France. It considers the global fab toolset and studies the skip, under some assumptions, of a defectivity measurement.

The Wafer-At-Risk is in use as the risk evaluation of each tool. The information brought by each lot that can be inspected is called the Wafer-At-Risk-Reduction. The problem is that this data is not directly available in fab, so, an algorithm was developed for the computation of the Wafer-At-Risk and Wafer-At-Risk-Reduction.

Description of the algorithm deployed

The first step is to identify the lots that have been actually inspected. The first difficulty there is to identify Defectivity Work Requests. DWR are special requests issued by engineering who puts lot on hold for further inspection in Defectivity. Measurement records are then used and combined with process data to identify and mark all inspected lots (figure1).

After that, Wafer-At-Risk value is computed for each process tool. The value is increased by lots quantity of wafers at each process event. It is decreased by Wafer-At-Risk-Reduction when lot is inspected. Regarding the amount of data and the complexity of links to be done, the processing horizon has been reduced to one-week. In order to match the data between successive weeks, we have defined boundary conditions, which consist of the list of lots having been processed after the last inspected lot (Figure2).

A further improvement of the algorithm was the definition of Wafer-At-Risk by recipe, recipe-type or technology and tool-module. The one may control defectivity by resist. The defectivity control model had to be refined to take into account those conditional resets and the algorithm was then adjusted to compute the various kinds of Wafer-At-Risk: global and recipe or context dependent (figure3).

Results and perspective

A skip algorithm has been added to our prototype, when we save on the directivity waiting buffer only lots which can decrease the value of Wafer-At-Risk. If the wafer-at-risk-reduction of a flagged lot is equal or less than zero, this lot is skipped. We noticed that up to 35% of inspected lots can be skipped.

The algorithm has been improved to be independent from the duration of historical data. It can be used even for a 30 minutes period which is very close to a real time implementation of the Wafer-At-risk algorithm.

Acknowledgments: This work is supported by the IMPROVE ENIAC European Project.

References

[1] R. Nurani et J. Shanthikumar, "The impact of lot-to-lot and wafer-to-wafer variations on SPC," *Semiconductor Manufacturing Conference Proceedings, 1997 IEEE International Symposium*, 1997, pp. P69-72.

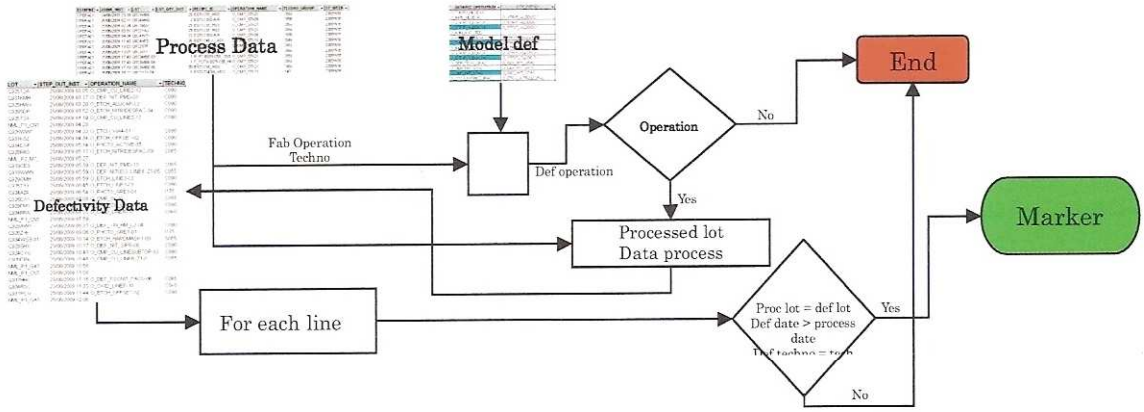

Figure 1: Flag algorithm

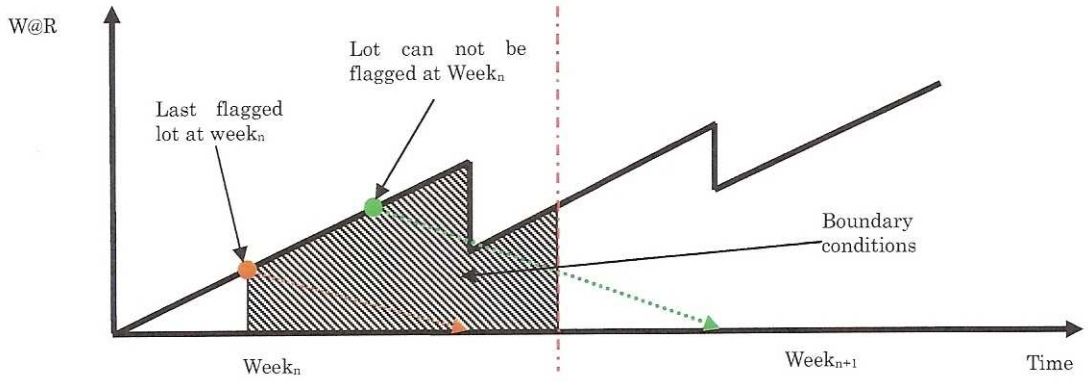

Figure 2: boundary conditions

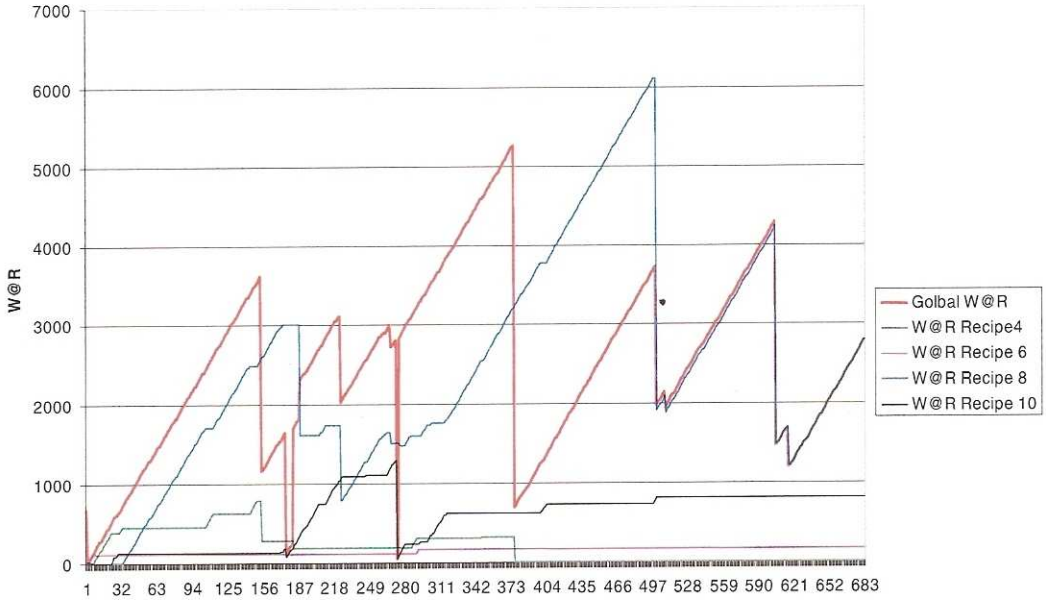

Figure 3: Global W@R and W@R by recipe