BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI

K. K. BIRLA Goa Campus

First Semester 2017-2018
CS F342 Computer Architecture

Course Project

INSTRUCTIONS

- 1. The project weightage is 10% and the deadline is 22nd November 2017.
- 2. This is a team project and the list of team members is available in course page.
- 3. You are not allowed to take help in terms of suggestions and code from other teams.
- 4. You are not allowed to use somebody else's code which includes code from internet.
- 5. If found copied, all members of the team will get -30 marks (will subtract 30 marks from their lab marks). Please see section 4.2 and 4.3 of your course handout for further details. [You are allowed to opt out from the project. In that case you are not considered for evaluation]
- 6. The project will be evaluated according to the following criteria:

STEPS TO FOLLOW FOR GETTING PROJECT ASSIGNED

- 1. Each team should decide the preference order (You should include all the 30 preferences).
- 2. One person from the team should consolidate all the 30 preferences and update. [Make sure you are updating your preferences before **08th November 2017**]. [Make sure ONLY ONE person from a team is doing it].
- 3. Allocation of project is on First Come First Serve basis. No default project allocation is available i.e. if you are not updated preference before 08th November 2017, you are not going to do the project.

Problem Statement:-

Design VLIW architecture with given* instruction set and design the Cache Memory with the given* specifications.

(* - refer your respective question after allotment)

Instructions:-

- O Your final submission should include:
 - 1. Verilog implementation of the Project
 - 2. Diagram showing the entire architecture (submit in chart sheet)
 - 3. During demonstration, you should simulate each instruction separately and combined.
 - 4. README.txt with the following details:
 - #bits used for Offset, Index and Tag (assume 32-bit physical address)
 - Total Cache Size (You should include the size of prediction circuit and halt tag array cache for Way-Prediction cache and Way-Halting cache cache respectively)
 - Based on the test case, Number of Cache Hits and CacheMiss

Group number, names of all the members and individual contributions for the project

Question 1:

Cache Specific	eations
Cache Size	512B
Cache Line Size	8B
Associativity	4
Write Policy	Write Back
Replacement policy	FIFO
Cache Type	Way Halting

Instructi on Type	Instructi on	31	3 0	2 9	2 8	2 7	2	2 5	2 4	2 3	2	2 1	2	1 9	1 8	1 7	1 6	1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3 2	2 1	0
				fur	ct7					lm	[4:0)]				rs1			f	unct	3		ı	r	d			1	оро	ode	- I	
	slli	0	0	0	0	0	0	0		shar	nt[4	1:0]				rs1			0	0	1			r	d		0	0	1	0 0	1	1
P type												Re	eg[ro	l] = F	leg[ı	rs1] <	< sha	amt														
R type				fur	ct7						rs2					rs1			f	unct	3			r	d				оро	ode		
	add	0	0	0	0	0	0	0			rs2					rs1			0	0	0			ro	d		0	1	1	0 0	1	1
												Re	g[rd] = R	eg[r	s1] +	Reg[rs2]														
						lm	m[11	.:0]								rs1			f	unct	3			r	d				оро	ode		
	jalr					lm	m[11	:0]								rs1			0	0	0			r	d		1	1	0	0 1	. 1	1
								R	eg[ro	[] = P	C +	3 (n	ext F	PC), F	C =	sExt({Imm	1[11:	0],0	}) + F	Reg[r	s1]										
I type	xori					lm	m[11	:0]								rs1			1	0	0			r	d		0	0	1	0 0	1	1
											Re	eg[ro	i] = [Reg[r	s1]	^ sExt	t(Imr	n[11	:0])													
	lh					lm	m[11	:0]								rs1			0	0	1			r	d		0	0	0	0 0) 1	1
									Reg[rd] =	sEx	t(Me	em[[Reg[rs1]	+ sEx	t(Im	m[1:	1:0])] (16	bits))										
				In	ım						rs2					rs1			f	unct	3			lm	m				opo	ode		
B type	BEQ	imm[1 2]		i	mm[[10:5]				rs2					rs1			0	0	0	İI	mm[4:1]		imm[1 1]	1	1	0	0 0	1	1
										PC(ta	arge	et) <	= sex	t12t	032	(imm	[12:0)]) , i	f rs1	==rs	2											

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		fur	ct3		Imm[5]		ı	rd				 	4:0			0	р
CI type	C.LI	0	1	0	Imm[5]		rd	(≠ 0)			lmm	4:0]			0	1
		Reg[rd] = sExt(Imm[5:0])															
		funct6 rd/rs1 funct rs2														0	р
CR type	C.AND	1	0	0	0	1	1	r	d/rs	1	1	1		rs2		0	1
					Reg[rd] = F	leg[rs	31] &	Reg	[rs2	2]							
		fur	ct3		 	5:3]			rs1		Imm	[2 6]		rs2		0	р
CS type	C.SW	1	1	0	Imm[5:3]			rs1		Imm	[2 6]		rs2		0	0
			Mem	[Reg	[rs1] + {15'k	0,lm	m[6:	2],2	'b0}] = [Reg[rs:	2]					

Question 2:

Cache Specific	eations
Cache Size	512B
Cache Line Size	8B
Associativity	4
Write Policy	Write Back
Replacement policy	FIFO
Cache Type	Way Prediction

Instructio	Instructio	3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1 0	9	8	7	6	5	4	3	2 1	. 0
n Type	n	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0		0	<u> </u>	0		7	•		
				f	unct	7				Ir	n[4:0)]				rs1			f	unct	3			rd					орс	ode	•	
	srli	0	0	0	0	0	0	0		sha	mt[4	:0]				rs1			1	0	1			rd			0	0	1	0	0 1	. 1
D tuno												Re	g[rd] = Re	eg[rs	1] >>	shar	nt														
R type				f	unct	7					rs2					rs1			f	unct	3			rd					орс	ode	•	
	xor	0	0	0	0	0	0	0			rs2					rs1			1	0	0			rd			0	1	1	0	0 1	. 1
												Re	g[rd]	= Re	g[rs1	L] ^ R	eg[r	52]														
						I	mm[11:0]						-	rs1			f	unct	3			rd					орс	ode	•	
	addi					ı	mm[11:0]							rs1			0	0	0			rd			0	0	1	0	0 1	. 1
											Re	eg[rd] = R	eg[rs	1]+:	sExt(l	lmm	[11:0)])													
I type	jalr						mm[11:0								rs1			0	0	0			rd			1	1	0	0	1 1	. 1
								F	Reg[r	d] = I	PC+	3 (ne	ext P	C), P(C = sE	xt({lı	mm[11:0],0})	+ Re	g[rs1]										
	slti						mm[11:0								rs1			0	1	0			rd			0	0	1	0	0 1	. 1
											Reg[ı	rd] =	(Reg	[rs1]	< sE	xt(Im	m[1:	1:0]))?1:0													
				lm	m[11	L: 5]					rs2					rs1			f	unct	3		lmr	ո[4։	0]				орс	ode	•	
S type	SW			lm	m[11	:5]					rs2					rs1			0	0	1		lmr	n[4:	0]		0	1	0	0	0 1	. 1
										N	1em[Reg[rs1]	+ sEx	t(Im	m[11	:0])]	= Re	g[rs2	!]												

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		f	unct	3	Imm[5]		ı	rd				Imm	4:0			0	р
CI type	C.LUI	0	1	1	Imm[5]		rd	(≠ 0)			lmm	4:0]			0	1
					Reg[rd] =	sExt({Imm	{5:0)],12	2'b0	})						
		Reg[rd] = sExt({Imm{5:0],12'b0}) funct3														р	
CB type	C.BNEZ	1	1	1	Imm[8	4:3			rs1		Im	m[7:6	2:1	.[5]		0	1
				i	f(Reg[rs1]!	= 0) F	PC = F	PC +	sEx	t(In	ım)						
		f	unct	3	Imm	[5:3]			rs1		lmm	[2 6]		rd		0	р
CL type	C.LW	0	1	0	lmm	[5:3]			rs1		Imm	[2 6]		rd		0	0
			Re	g[rd]	= Mem[Re	g[rs1] + {1	.5'b(O,Im	nm[6	5:2],2'l	o0}]					

Question 3:

Cache Specific	eations
Cache Size	512B
Cache Line Size	8B
Associativity	4
Write Policy	Write Back
Replacement policy	LRU counter
Cache Type	Way Halting

Instructi	Instructi	31	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1 1 9	8 7	6	5	4 3	2	1	0
on Type	on		0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1 0							Щ
				fun	ct7					In	n[4:0	0]				rs1			f	unct	:3	rc	<u> </u>			opco	de		
	srai	0	1	0	0	0	0	0		sha	mt[4	4:0]				rs1			1	0	1	ro	t	0	0	1 0	0	1	1
D tuno												Re	g[rd] = R	eg[rs	1] >>	>> sh	namt											
R type				fun	ct7						rs2					rs1			f	unct	:3	ro	ł			орсо	de		
	sub	0	1	0	0	0	0	0			rs2					rs1			0	0	0	rc	d	0	1	1 0	0	1	1
												Re	g[rd	[] = R	eg[rs	1] -	Reg[[rs2]											
						lmr	n[11	:0]								rs1			f	unct	:3	ro	k			орсо	de		
	addi					lmr	n[11	:0]								rs1			0	0	0	rc	k	0	0	1 0	0	1	1
											Re	eg[rd	[] = F	Reg[r	s1] +	sExt	t(Imr	n[11	L:0])										
I type	jalr					lmr	n[11	:0]								rs1			0	0	0	rc	k	1	1	0 0	1	1	1
								R	eg[rd] = F	PC +	3 (ne	ext P	PC), F	C = s	Ext({lmn	n[11	:0],0	})+	Reg[rs1]							
	sltiu					lmr	n[11	:0]								rs1			0	1	1	ro	t	0	0	1 0	0	1	1
										R	eg[r	d] =	(Reg	[rs1]	<{20	'b0,	lmm	[11:	0]})?	1:0									
				lm	m						rs2					rs1			f	unct	:3	lm	m			орсо	de		\neg
B type	BLT	imm[1 2]		i	mm[10:5]				rs2					rs1			1	0	0	imm[4:1]	imm[1 1]	1	1	0 0	0	1	1
										PC(targ	et) <	= se	xt12	to32(imm	1[12:	0]),	if rs	1 <rs< td=""><td>2</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></rs<>	2								

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			fur	nct4			rd	/rs1				rs	2			0	р
CR type	C.MV	1	0	0	0		rd	(≠ 0)			rs2 (≠ 0)			1	0
		Reg[rd] = Reg[rs2]															
		fun	ct3		Imm	5:3]			rs1		Imm	[2 6]		rd		0	р
CL type	C.LW	0	1	0	Imm	5:3]			rs1		Imm	[2 6]		rd		0	0
			Reg[ı	rd] =	Mem[Reg[ı	·s1] +	{15'l	اا,0c	mm	[6:2],2'b0}	·]					
		fun	ct3		Imm	5:3]			rs1		Imm	[2 6]		rs2		0	р
CS type	C.SW	1	1	0	Imm	5:3]			rs1		Imm	[2 6]		rs2		0	0
			Mem	[Reg[rs1] + {15'k	0,lm	m[6:	2],2	'b0}] = [Reg[rs2	2]					

Question 4:

Cache Specific	eations
Cache Size	512B
Cache Line Size	8B
Associativity	4
Write Policy	Write Through
Replacement policy	Pseudo LRU
Cache Type	Way Prediction

Instructio n Type	Instructio n	3 1	3	2 9	2 8	2 7	2	2	2	2	2 2	2	0		1 8	1 7	1 6	1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	,	6 5		3	2	1	0
,,			1	f	unct	7				ı	lm[4:	0]				rs1	1		1	unct	3			rd	l					орсо	ode		
	srli	0	0	0	0	0	0	0			namt[rs1			1	0	1			rd				0 0		. 0			1
Datumo												R	eg[r	rd] = F	eg[rs	1] >:	> sha	mt															
R type				f	unct	7					rs2					rs1			1	unct	3			rd					(эрсс	ode		
	xor	0	0	0	0	0	0	0			rs2					rs1			1	0	0			rd				0 1	. 1	. 0	0	1	1
												Re	eg[r	d] = R	eg[rs	1] ^	Reg[r	ˈs2]															
						l	mm[11:0]							rs1			1	unct	3			rd					(орсс	ode		
	jalr						lmm[11:0]							rs1			0	0	0			rd				1 1	. (0 (1	1	1
I type								F	Reg[r	d] =	PC +	3 (n	ext	PC), F	C = s	Ext({	Imm	[11:0],0})	+ Re	g[rs1]											
	addi						lmm[11:0]							rs1			0	0	0			rd				0 0	1	. 0	0	1	1
											R	eg[ro	d] =	Reg[r	s1] +	sExt	(Imm	[11:0)])														
				lm	m[11	L: 5]					rs2					rs1			1	unct	3	I	lmr	n[4:	[0]				(opco	ode		
S type	SW			Im	m[11	.:5]					rs2					rs1			0	0	1		lmr	n[4:	0]			0 1	. (0 0	0	1	1
											Mem	[Reg	[rs1	L] + sE	xt(Im	m[1:	1:0])]	= Re	g[rs2	2]													
											Ir	nm												rd					. (opco	ode		
U type	AUIPC									i	imm	31:1	2]											rd				0 0	1	. 0	1	1	1
												Reg[rd] :	= PC +	{imn	n[31	:12],:	12'd0	}														

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				funct	:4		rd	/rs1				rs	2			0	р
CR type	C.MV	1	0	0	0		rd	(≠ 0)			rs2 (≠ 0)			1	0
					Re	g[rd]	= Re	g[rs:	2]								
		Reg[rd] = Reg[rs2] funct3 Imm[5:3] rs1 Imm[2 6] rd														0	р
CL type	C.LW	0	1	0	lmm[5:3]			rs1		Imm	[2 6]		rd		0	0
			Re	g[rd]	= Mem[Re	g[rs1] + {1	.5'b(O,Im	m[6	5:2],2'l	o0}]					
		f	unct	3	Imm[8	4:3]		rs1		lm	m[7:6	2:1	L[5]		0	р
CB type	C.BEQZ	1	1	0	Imm[8	4:3			rs1		lm	m[7:6	2:1	[5]		0	1
				if	f(Reg[rs1] =	= 0) I	PC = I	PC +	sEx	t(In	nm)						

Question 5:

Cache Specific	eations
Cache Size	512B
Cache Line Size	8B
Associativity	4
Write Policy	Write Back
Replacement policy	LRU counter
Cache Type	Way Prediction

Instructi on Type	Instructi on	31	3 0	2 9	2 8	2 7	2	2 5	2 4	2	2 2	2 1	2	1 9	1 8	1 7	1 6	1 5	1 4	1	1 2	1 1 0 9 8	7	6	5 .	4 3	3 2	1	. 0
				fun	ct7					lm	[4:0)]				rs1			f	unct	3	rd				opc	ode		
	slli	0	0	0	0	0	0	0		shar	nt[4	:0]				rs1			0	0	1	rd		0 ()	1 (0	1	. 1
P type												Re	g[rd] = R	eg[r	s1] <	< sh	amt											
R type				fun	ct7						rs2					rs1			f	unct	3	rd				opc	ode		
	sltu	0	0	0	0	0	0	0			rs2					rs1			0	1	1	rd		0	1	1 (0	1	. 1
									Reg	g[rd]	= (uı	nsigi	ned(Reg[rs1])	< ur	nsign	ed(F	Reg[r	·s2]))?1:0)							
						lmr	n[11	:0]								rs1			f	unct	3	rd				opc	ode		
	addi					lmr	n[11	:0]								rs1			0	0	0	rd		0 ()	1 (0	1	. 1
I type											Re	g[rd] = R	leg[r	s1] +	sExt	(Imr	n[11	:0])										
	lh					lmr	n[11	:0]								rs1			0	0	1	rd		0 ()) (0	1	. 1
									Reg[rd] =	sExt	t(Me	m[[l	Reg[rs1] -	⊦ sEx	t(Im	m[1:	1:0])] (16	bits	5))							
										li	mm											rd				opc	ode		
U type	LUI									imm	[31::	12]										rd		0	1	1 () 1	1	. 1
												Re	g[rd]	= {iı	nm[31:12	2],12	2'd0}											
				lm	m						rs2					rs1			f	unct	3	lmm				opc	ode		
B type	BLTU	2]									rs2					rs1			1	1	0	imm[4:1]	imm[1 1]	1	1		0	1	. 1
							PC	(tar	get) <	<= se	xt12	to32	2(im	m[12	2:0])	, if rs	1 <r< th=""><th>s2 (u</th><th>nsig</th><th>ned</th><th>com</th><th>parision)</th><th></th><th></th><th></th><th></th><th></th><th></th><th></th></r<>	s2 (u	nsig	ned	com	parision)							

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			fu	nct4			rd	/rs1				rs	2			0	р
CR type	C.MV	1	0	0	0		rd	(≠ 0)			rs2 (≠ 0)			1	0
		Reg[rd] = Reg[rs2]															
		funct3 Imm[5:3] rs1 Imm[2 6] rs2														0	р
CS type	C.SW	1	1	0	Imm	[5:3]			rs1		Imm	[2 6]		rs2		0	0
			Mem	[Reg	[rs1] + {15'l	o0,Im	m[6:	2],2	'b0]	}] =	Reg[rs	2]					
		fur	nct3					lm	nm[:	10:0)]					0	р
CJ type	C.JALR	0	0	1				lm	nm[:	10:0)]					0	1
			Reg	[x1] :	= PC + 3 (ne	ew PO	C), PC	= P	C +	sEx	t(Imm)						

Question 6:

Cache Specific	eations
Cache Size	512B
Cache Line Size	8B
Associativity	4
Write Policy	Write Back
Replacement policy	Pseudo LRU
Cache Type	Way Halting

Instructio n Type	Instructio n	3 1	3 0	2 9	2 8	2 7	2 6	2	2 2 2 2 2 2 5 4 3 2 1 Im[4:0]						1 8	1 7	1 6	1 5	1 4	1	1 2	1	1	9	8	7	6	5	4	3	2 :	1 0
, pc		_			unct				•			_ <u>-</u> 01		9		rs1				unct				rd					go	cod	<u> </u>	
	srai	0	1	0	0	0	0	0			amt[4					rs1			1	0	1			rd			0	0			0 :	1 1
		<u> </u>											g[rd] = Re	g[rs2	1] >>>	> sha	mt														
R type				f	unct	7					rs2					rs1			f	unct	3			rd					ор	cod	•	
	srl	0	0	0	0	0	0	0			rs2					rs1			1	0	1			rd			0	1	1	0	0 :	1 1
											F	Reg[r	d] =	Reg[rs1] >	>> Re	g[rs2][4:0]		•											
						ı	mm	[11:0]							rs1			f	unct	3			rd					ор	cod	•	
	addi						lmm[[11:0]]							rs1			0	0	0			rd			0	0	1	0	0 3	1 1
I type											R	eg[ro	l] = l	Reg[rs	51] +	sExt(lmm	[11:0)])													
	ori						lmm[[11:0]							rs1			1	1	0			rd			0	0	1	0	0 2	1 1
											R	eg[ro	l] = I	Reg[r	s1]	sExt(lmm	[11:0)])													
				lmı	n[11	:5]					rs2					rs1			f	unct	3		lmr	n[4:	0]				op	cod	<u> </u>	
S type	sb			lmi	n[11	:5]					rs2					rs1			0	0	0		Imr	n[4:	0]		0	1	0	0	0 1	1 1
		ı								Me	em[R	eg[rs	1] +	sExt(lmm	[11:0]])] =	Reg[ı	rs2][7	7:0]												
											In	ım												rd					op	cod	•	
U type	AUIPC	imm[31																						rd			0	0	1	0	1 1	1 1
												Reg[r	d] =	PC+	{imn	n[31:	12],1	2'd0	}													

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		f	unct	3	Imm[5]		rd	/rs1				lmm[4:0			0	р
CR type	C.JALR	1	0	0	1		rs1	(≠ 0))		0	0	0	0	0	1	0
		Reg[1] = PC + 3 (new PC), PC = Reg[rs1]															
		funct3 Imm[5:3] rs1 Imm[2 6] rd 0															р
CL type	C.LW	0	1	0	lmm[5:3]			rs1		Imm	[2 6]		rd		0	0
			Re	g[rd]	= Mem[Re	g[rs1] + {1	.5'b(O,Im	m[6	5:2],2'l	00}]					
		f	unct	3	Imm[8	4:3]		rs1		lm	m[7:6	2:1	L[5]		0	р
CB type	C.BNEZ	1	1	1	Imm[8	4:3			rs1		lm	m[7:6	2:1	[5]		0	1
				if	f(Reg[rs1]!	= 0) F	PC = F	PC +	sEx	t(Im	nm)						

Question 7:

Cache Specific	eations
Cache Size	512B
Cache Line Size	8B
Associativity	4
Write Policy	Write Back
Replacement policy	Pseudo LRU
Cache Type	Way Prediction

Instructio n Type	Instructio n	3 1	3	2 9	2	2 7	2 6	2 5	2	2	2 2	2	2	1 9	1 8	1 7	1 6	1 5	1 4	1	1 2	1 1	L (9	8	7	6	5	4	3	2 1	ı
				f	unct	7				In	n[4:0	0]				rs1	· ·		f	unct	3		rd						ор	cod	•	
	slli	0	0	0	0	0	0	0		sha	mt[4	1:0]				rs1			0	0	1		rd				0	0	1	0	0 1	1
P type												Re	g[rd]	= Re	g[rs	1] <<	shar	nt														
R type				f	unct	7					rs2					rs1			f	unct	3		rd						ор	cod	•	
	or	0	0	0	0	0	0	0			rs2					rs1			1	1	0		rd				0	1	1	0	0 2	1
												Re	g[rd]	= Re	g[rs1	L] R	eg[rs	52]														
						ı	mm[11:0								rs1			f	unct	3		rd						ор	cod	•	
	lh					I	mm[11:0								rs1			0	0	1		rd				0	0	0	0	0 2	l 1
									Reg	[rd] =	= sEx	t(Me	m[[R	eg[rs	s1] +	sExt(lmm	[11:	0])](16 b	its))											
I type	xori					I	mm[11:0]								rs1			1	0	0		rd				0	0	1	0	0 1	1 1
											Re	eg[rd] = Re	eg[rs	1] ^ :	sExt(I	mm	[11:0)])													
	jalr					I	mm[11:0]								rs1			0	0	0		rd				1	1	0	0	1 1	1 1
								F	leg[r	d] = [PC+	3 (ne	xt PC	C), PC	C = sE	xt({Ir	mm[11:0],0}) -	⊦ Re{	g[rs1]]										
											lm	ım											rd						ор	cod	9	
U type	LUI									ir	nm[31:12	2]										rd				0	1	1	0	1 1	l 1
												Re	g[rd]	= {im	nm[3	1:12]	,12'0	(0b														

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		fun	ct3		Imm[5]		rd	/rs1				Imm	4:0			0	р
CR type	C.ADDI	0 0 0 Imm[5] rs1/rd (≠ 0) Imm[4:0]														0	1
		Reg[rd] = Reg[rs1] + sExt(Imm[5:0])															
																0	р
CB type	C.BEQZ	1	1	0	Imm[8	4:3			rs1		lm	m[7:6	2:1	.[5]		0	1
				if(R	eg[rs1] == ()) PC	= PC	+ sE	Ext(I	mm	1)						
		fun	ct3		lmm[5:3]			rs1		lmm	[2 6]		rs2		0	р
CS type	C.SW	1	1	0	lmm[5:3]			rs1		Imm	[2 6]		rs2		0	0
			Mem	[Reg[rs1] + {15'b	0,lm	m[6:	2],2	'b0}	·] = [Reg[rs2	2]					

Question 8:

Cache Specific	eations
Cache Size	512B
Cache Line Size	8B
Associativity	4
Write Policy	Write Back
Replacement policy	Random
Cache Type	Way Halting

Instructi	Instructi	31	3	2	2	2	2	2	2	2	2 2	2	1	1	1	1	1	1	1	1	1	1	9 8		7	6	5	4	3 2	1	0
on Type	on	5	0	9	8	7	6	5	4	3	2 1	0	9	8	7	6	5	4	3	2	1	0	J 8			U	,	7	3 2		
				fun	ct7					Im	4:0]				rs1			f	unc	t3			rd					оро	ode		
	srai	0	1	0	0	0	0	0		sham	nt[4:0]			rs1			1	0	1			rd			0	0	1	0 0	1	1
D 4											R	eg[ro	d] = R	eg[rs	51] >:	>> sh	amt														
R type				fun	ct7					r	s2				rs1			f	unc	t3			rd					оро	ode		
	add	0	0	0	0	0	0	0		r	s2				rs1			0	0	0			rd			0	1	1	0 0	1	1
											F	Reg[r	d] = F	Reg[r	s1] +	Reg	[rs2]														
						lmr	n[11	:0]							rs1			f	unc	t3			rd					оро	ode		
	jalr					lmr	n[11	:0]							rs1			0	0	0			rd			1	1	0	0 1	. 1	1
I type								R	eg[rd] = PC	2+3(next	PC), I	PC = 9	sExt({Imn	า[11:	:0],0	<u>})</u> +	Reg[rs1]										
	andi					lmr	n[11	:0]							rs1			1	1	0			rd			0	0	1	0 0	1	1
											Reg[ı	rd] =	Reg[ı	rs1] 8	k sEx	t(Imi	m[11	L:0])													
			ı	mm[11:5]				r	s 2				rs1			f	unc	t3		lr	nm[4	:0]				оре	ode		
S type	sh		I	mm[11:5]				r	s2				rs1			0	0	1		lr	nm[4	:0]		0	1	0	0 0	1	1
									1	Mem[Reg[r	s1] +	sExt((Imm	[11:0)])] =	Reg	[rs2][15	:0]											
					r	s 2				rs1			f	unc	t3			lmm					ор	ode							
B type	BGE	BGE imm[1 imm[10:5]								r	s2				rs1			1	0	1	iı	nm[4	1:1]	in	nm[1 1]	1	1	0	0 0	1	1
	PC(target												xt12	to32	(imm	า[12:	0]),	if rs	1>rs	2											

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			1	funct	4		rd	/rs1				rs	2			0	р
CR type	C.MV	1	0	0	0		rd	(≠ 0)			rs2 (≠ 0)			1	0
		Reg[rd] = Reg[rs2]															
		funct3 Imm[5] rd Imm[4:0]															р
CI type	C.LI	0	1	0	Imm[5]		rd	(≠ 0)			lmm[4:0]			0	1
					Reg[ro	d] = s	Ext(Ir	nm[5:0])							
		f	unct	3	lmm[5:3]			rs1		Imm	[2 6]		rd		0	р
CL type														0	0		
			Re	g[rd]	= Mem[Re	g[rs1] + {1	.5'b(O,Im	m[6	5:2],2'k	00}]					

Question 9:

Cache Specific	eations
Cache Size	512B
Cache Line Size	8B
Associativity	4
Write Policy	Write Back
Replacement policy	Random
Cache Type	Way Prediction

Instructio	Instructio	3	3	2	2	2	2	2	2	2	2	2	2	1	1	1 7	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	L O
n Type	n	1	0	9	8		6	5	4	3	2	1	0	9	8		6	5	4	3	2	1	0									
				f	unct	7				Ir	n[4:0	0]				rs1			f	unct	3		r	d					op	cod	е	
	srli	0	0	0	0	0	0	0		sha	mt[4	1:0]				rs1			1	0	1		r	d			0	0	1	0	0 :	l 1
D tuno												Re	g[rd] = Re	eg[rs	1] >>	shar	nt														
R type				f	unct	7					rs2					rs1			f	unct	3		r	d					op	cod	е	
	sltu	0	0	0	0	0	0	0			rs2					rs1			0	1	1		r	d			0	1	1	0	0 :	l 1
									Re	g[rd]	= (u	ınsigı	ned(Reg[r	s1]) ·	< uns	igne	d(Re	g[rs2]))?1	:0											
						ı	mm[11:0								rs1			f	unct	3		r	d					op	cod	е	
	addi					I	mm[11:0]								rs1			0	0	0		r	d			0	0	1	0	0 :	l 1
											Re	eg[rd] = R	eg[rs	1] + :	sExt(Imm	[11:0)])													
I type	lbu					I	mm[11:0]								rs1			1	0	0		r	d			0	0	0	0	0 :	l 1
									Reg[rd] =	{24	'b0,N	1em	[[Reg	[rs1]	+ sEx	kt(Im	m[1:	1:0])]	(8 b	its)}											
	xori					I	mm[11:0]								rs1			1	0	0		r	d			0	0	1	0	0 :	l 1
											Re	eg[rd] = R	eg[rs	1] ^	sExt(lmm	[11:0)])													
											lm	ım											r	d					op	cod	е	
U type	AUIPC									ir	nm[3	31:12	2]										r	d			0	0	1	0	1 :	l 1
											F	Reg[r	d] =	PC +	{imr	า[31::	12],1	2'd0	}													

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			fur	nct4			rd	/rs1				rs	2			0	р
CR type	C.JALR	1	0	0	1		rs1	(≠ C))		0	0	0	0	0	1	0
		Reg[1] = PC + 3 (new PC), PC = Reg[rs1]															
		funct3 Imm[8 4:3] rs1 Imm[7:6														0	р
CB type	C.BEQZ	1	1	0	Imm[8	[4:3]			rs1		lm	m[7:6	2:1	.[5]		0	1
				if(R	eg[rs1] == () PC	= PC	+ sE	xt(I	mm	1)						
		fun	ict3		Imm	5:3]			rs1		Imm	[2 6]		rs2		0	р
CS type	C.SW	1	1	0	Imm	5:3]			rs1		Imm	[2 6]		rs2		0	0
			Mem	[Reg[rs1] + {15'k	0,lm	m[6:	2],2	'b0}] = F	Reg[rs2	2]					

Question 10:

Cache Specific	eations
Cache Size	512B
Cache Line Size	8B
Associativity	4
Write Policy	Write Through
Replacement policy	LRU Counter
Cache Type	Way Halting

Instructio n Type	Instructio n	3 1	3	2 9	2 8	2 7	2	2 5	2	2	2 2	2	2	1 9	1 8	1 7	1 6	1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	' (5 5	4	3	2	1	0
		1 0 9 8 7 6 5 4 3 2 funct7 Im[4:0] 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0											1		l	rs1		l	f	unct	3		ı	rd		<u> </u>		l l	0	pcod	de	I	
	slli	0	0	0	0	0	0	0		sha	amt[4	4:0]				rs1			0	0	1		ı	rd			(0 0	1	0	0	1	1
P type												Re	eg[ro	l] = R	eg[rs	1] <<	shar	nt															
R type				f	unct	7					rs2					rs1			f	unct	3		ı	rd					0	рсос	de		
	or	0	0	0	0	0	0	0			rs2					rs1			1	1	0		ı	rd			() 1	1	0	0	1	1
												Re	g[rd] = Re	g[rs2	1] R	eg[r	s2]															
							mm[11:0]							rs1			f	unct	3		ı	rd					0	рсос	de		
	jalr						lmm[11:0]							rs1			0	0	0		ı	rd				l 1	0	0	1	1	1
I type								F	Reg[r	d] =	PC+	3 (n	ext P	C), P	C = sE	Ext({Iı	nm[11:0],0})	+ Reg	g[rs1]]											
	sltiu						lmm[11:0]							rs1			0	1	1		l	rd			(0 (1	0	0	1	1
										F	Reg[r	d] =	(Reg	[rs1]	<{20'	b0,In	nm[1	l1:0]	})?1:)													
				lm	m[11	.:5]					rs2					rs1			f	unct	3	I	mn	า[4:	0]				0	рсос	de		
S type	sb			lm	m[11	.:5]					rs2					rs1			0	0	0	I	mm	า[4:	0]		() 1	0	0	0	1	1
										Me	m[R	eg[rs	1] +	sExt(I	mm[[11:0])] =	Reg[rs2][ː	7:0]													
											lmm	[19:0)]										ı	rd					0	рсос	de		
J type	JAL										imm	[10:0)]											rd				l 1	0	1	1	1	1
								Р	C(tar	get)	<= S	ext20	Oto3	2(imr	n[20:	([0:	PC,	rd = 1	PC+	3 (ne	w PC	C)											

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				funct	:4		rd	/rs1				rs	2			0	р
CR type	C.MV	1	0	0	0		rd	(≠ 0)			rs2 (≠ 0)			1	0
		Reg[rd] = Reg[rs2]															
		f	unct	3	lmm[[5:3]			rs1		Imm	[2 6]		rd		0	р
CL type	C.LW	0	1	0	lmm[[5:3]			rs1		Imm	[2 6]		rd		0	0
			Re	g[rd]	= Mem[Re	g[rs1] + {1	.5'b(O,Im	ım[6	5:2],2'l	o0}]					
		f	unct	3	Imm[5]		rd	/rs1				lmm[4:0			0	p
CI type	C.ADDI														0	1	
				ı	Reg[rd] = Re	eg[rs	1] + s	Ext(lmr	n[5:	0])						

Question 11:

Cache Specific	eations
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Back
Replacement policy	FIFO
Cache Type	Way Halting

Instructi on Type	Instructi on	31	3 0	2 9	2 8	2 7	2 6	2 5	2	2	2 2	2 1	2	1 9	1 8	1 7	1 6	1 5	1 4	1	1 2	1 1	1 0	9 8	7	6	5	4 3	3 2	1	0
				fur	nct7					lm	[4:0]				rs1	l.		f	unct	3			rd				орс	ode		
	slli	0	0	0	0	0	0	0		shar	nt[4	:0]				rs1			0	0	1			rd		0	0	1 (0 (1	1
P type												Re	g[rd] = R	leg[r	s1] <	< sha	amt													
R type				fur	rct7						rs2					rs1			f	unct	3			rd				орс	ode		
	add	0	0	0	0	0	0	0			rs2					rs1			0	0	0			rd		0	1	1 (0 0	1	1
				Re	g[rd]] = R	eg[rs	51] +	Reg[rs2]																					
						lm	n[11	L: 0]								rs1			f	unct	3			rd				орс	ode		
	jalr										rs1			0	0	0			rd		1	1	0 0) 1	1	1					
		Imm[11:0] Reg[rd] = PC + 3 (next														Ext((Imm	[11:	0],0]	}) + F	Reg[r	s1]									
I type	xori					lm	n[11	L:0]								rs1			1	0	0			rd		0	0	1 (0 0	1	1
											Re	g[rd] = R	leg[r	s1] ^	· sExt	t(Imn	n[11	:0])												
	lh					lmi	n[11	L:0]								rs1			0	0	1			rd		0	0	0 0	0 0	1	1
									Reg[rd] =	sExt	t(Me	m[[l	Reg[rs1] ·	+ sEx	t(Im	m[11	L:0])] (16	bits))									
			1	In	ım						rs2					rs1			f	unct	3			lmm				орс	ode	1	
B type	BEQ	imm[1 2]		i	mm[[10:5]				rs2					rs1			0	0	0	ir	mm[4	1:1]	imm[1 1]	1	1	0 0	0	1	1
										PC(ta	arge	t) <=	sex	t12t	032(imm	[12:0]) , il	f rs1	==rs	2										

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		fur	ct3		Imm[5]		ı	rd				 	4:0			0	р
CI type	C.LI	0	1	0	Imm[5]		rd	(≠ 0)			lmm	4:0]			0	1
		Reg[rd] = sExt(Imm[5:0])															
		funct6 rd/rs1 funct rs2														0	р
CR type	C.AND	1	0	0	0	1	1	r	d/rs	1	1	1		rs2		0	1
					Reg[rd] = F	leg[rs	31] &	Reg	[rs2	2]							
		fur	ct3		 	5:3]			rs1		Imm	[2 6]		rs2		0	р
CS type	C.SW	1	1	0	Imm[5:3]			rs1		Imm	[2 6]		rs2		0	0
			Mem	[Reg	[rs1] + {15'k	0,lm	m[6:	2],2	'b0}] = [Reg[rs:	2]					

Question 12:

Cache Specific	eations
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Back
Replacement policy	FIFO
Cache Type	Way Prediction

Instructio	Instructio	3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3 2	2 1	. 0
n Type	n	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1 (0									
				f	unct	7				Ir	n[4:0	0]				rs1			f	unct	3		r	d					opo	ode)	
	srli	0	0	0	0	0	0	0		sha	ımt[4	1:0]				rs1			1	0	1		r	d			0	0	1	0 () 1	. 1
D tuno												Re	g[rd] = Re	eg[rs	1] >>	shar	nt														
R type				f	unct	7					rs2					rs1			f	unct	3		r	d					оро	ode)	
	xor	0	0	0	0	0	0	0			rs2					rs1			1	0	0		r	d			0	1	1	0 () 1	. 1
												Re	g[rd]	= Re	g[rs1	L] ^ R	eg[rs	52]														
						ı	mm[11:0]							rs1			f	unct	3		r	d					оро	ode)	
	addi					I	mm[11:0								rs1			0	0	0		r	d			0	0	1	0 () 1	. 1
											Re	eg[rd] = R	eg[rs	1] + :	sExt(l	mm	[11:0)])													
I type	jalr					I	mm[11:0								rs1			0	0	0		r	d			1	1	0	0 :	1 1	. 1
								F	Reg[r	d] = I	PC +	3 (ne	ext P	C), PO	C = sE	Ext({II	mm[11:0],0})	+ Re	g[rs1]										
	slti					I	mm[11:0								rs1			0	1	0		r	d			0	0	1	0 () 1	1
										I	Reg[ı	rd] =	(Reg	[rs1]	< sE	xt(Im	m[1:	1:0]))?1:0													
				lmı	m[11	:5]					rs2					rs1			f	unct	3	Ir	nm	[4:0)]				оро	ode	1	
S type	SW			lmı	m[11	:5]					rs2					rs1			0	0	1	Ir	nm	[4:0)]		0	1	0	0 () 1	. 1
										N	/lem	Reg[rs1]	+ sEx	t(Im	m[11	:0])]	= Re	g[rs2]												

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		f	unct	3	Imm[5]		ı	rd				Imm	4:0			0	р
CI type	C.LUI	0	1	1	Imm[5]		rd	(≠ 0)			lmm	4:0]			0	1
		Reg[rd] = sExt({Imm{5:0],12'b0})															
		f	unct	3	Imm[8	4:3]		rs1		lm	m[7:6	2:1	.[5]		0	р
CB type	C.BNEZ	1	1	1	Imm[8	4:3			rs1		Im	m[7:6	2:1	.[5]		0	1
				i	f(Reg[rs1]!	= 0) F	PC = F	PC +	sEx	t(In	ım)						
		f	unct	3	Imm	[5:3]			rs1		lmm	[2 6]		rd		0	р
CL type	funct3 Imm[5:3] rs1 Imm[2 6] rd C.LW 0 1 0 Imm[5:3] rs1 Imm[2 6] rd														0	0	
			Re	g[rd]	= Mem[Re	g[rs1] + {1	.5'b(O,Im	nm[6	5:2],2'l	o0}]					

Question 13:

Cache Specific	eations
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Back
Replacement policy	LRU counter
Cache Type	Way Halting

Instructi on Type	Instructi on	31	3	2 9	2	2 7	2	2 5	2	2 3	2 2	2	2 0		1 8	1 7	1 6	1 5	1 4	1 3	1 2	1	1 0	9	8	7	6	5 4	3	2	1 0)
				fun	ct7				l	In	ո[4:0	0]				rs1		ı	f	unct	:3			r	d			C	рсо	de		٦
	srai	0	1	0	0	0	0	0		shai	mt[4	1:0]				rs1			1	0	1			r	d		0	0 1	. 0	0	1 1	L
P type												Re	g[r	d] = R	eg[rs	51] >	>> sl	ham	t													
R type				fun	ct7						rs2					rs1			f	unct	:3			r	d			C	рсо	de		
	sub	0	1	0	0			rs2					rs1			0	0	0			r	d		0	1 1	. 0	0	1 1	ı.			
												Re	eg[r	rd] = F	leg[r	s1] -	Reg	[rs2]]													
						lmı	m[11	:0]								rs1			f	unct	:3			r	d			C	рсо	de		
	addi					lmı	m[11	:0]								rs1			0	0	0			r	d		0	0 1	. 0	0	1 1	L
											Re	eg[ro	d] =	Reg[r	·s1] -	- sEx	t(Im	m[1	1:0])													
I type	jalr					lmı	n[11	:0]								rs1			0	0	0			r	d		1	1 0	0	1	1 1	L
								R	eg[ro	d] = P	C +	3 (n	ext	PC), F	PC = :	sExt({{lmr	n[11	1:0],0)}) +	Reg[rs1]										
	sltiu					lmı	m[11	:0]								rs1			0	1	1			r	d		0	0 1	. 0	0	1 1	Ĺ
										Re	eg[r	d] =	(Re	eg[rs1]	<{2	0'b0,	,Imm	ո[11	:0]})?	21:0												
				lm	m						rs2					rs1			f	unct	:3			lm	ım			C	pco	de		
B type	BLT	imm[1 2]		i	mm	[10:5	5]				rs2					rs1			1	0	0	ii	mm[4:1]		imm[1 1]	1	1 0	0	0	1 1	L
										PC(t	targ	et) <	= s	ext12	to32	(imn	n[12	:0])	, if rs	1 <rs< td=""><td>2</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></rs<>	2											

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			fur	nct4			rd	/rs1				rs	2			0	р
CR type	C.MV	1	0	0	0		rd	(≠ 0)			rs2 (≠ 0)			1	0
		Reg[rd] = Reg[rs2]															
		funct3 Imm[5:3] rs1 Imm[2 6] rd														0	р
CL type	C.LW	0	1	0	Imm	5:3]			rs1		Imm	[2 6]		rd		0	0
			Reg[ı	rd] =	Mem[Reg[ı	·s1] +	{15'l	اا,0c	mm	[6:2],2'b0}	·]					
		fun	ct3		Imm	5:3]			rs1		Imm	[2 6]		rs2		0	р
CS type	C.SW	1	1	0	Imm	5:3]			rs1		Imm	[2 6]		rs2		0	0
			Mem	[Reg[rs1] + {15'k	0,lm	m[6:	2],2	'b0}] = [Reg[rs2	2]					

Question 14:

Cache Specific	eations
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Back
Replacement policy	LRU counter
Cache Type	Way Prediction

Instructi on Type	Instructi on	31	3 0	2 9	2 8	2 7	2	2 5	2 4	2	2 2	2 1	2	1 9	1 8	1 7	1 6	1 5	1 4	1	1 2	1 1 0 9 8	7	6	5 .	4 3	3 2	1	. 0
				fun	ct7					lm	[4:0)]				rs1			f	unct	3	rd				opc	ode		
	slli	0	0	0	0	0	0	0		shar	nt[4	:0]				rs1			0	0	1	rd		0 ()	1 (0	1	. 1
P type												Re	g[rd] = R	eg[r	s1] <	< sh	amt											
R type				fun	ct7						rs2					rs1			f	unct	3	rd				opc	ode		
	sltu	0	0	0	0	0	0	0			rs2					rs1			0	1	1	rd		0	1	1 (0	1	. 1
									Reg	g[rd]	= (uı	nsigi	ned(Reg[rs1])	< ur	nsign	ed(F	Reg[r	·s2]))?1:0)							
						lmr	n[11	:0]								rs1			f	unct	3	rd				opc	ode		
	addi					lmr	n[11	:0]								rs1			0	0	0	rd		0 ()	1 (0	1	. 1
I type											Re	g[rd] = R	leg[r	s1] +	sExt	(Imr	n[11	:0])										
	lh					lmr	n[11	:0]								rs1			0	0	1	rd		0 ()) (0	1	. 1
									Reg[rd] =	sExt	t(Me	m[[l	Reg[rs1] -	⊦ sEx	t(Im	m[1:	1:0])] (16	bits	5))							
										li	mm											rd				opc	ode		
U type	LUI									imm	[31::	12]										rd		0	1	1 () 1	1	. 1
												Re	g[rd]	= {iı	nm[31:12	2],12	2'd0}											
				lm	m						rs2					rs1			f	unct	3	lmm				opc	ode		
B type	BLTU	imm[1 2]		i	mm[10:5]				rs2					rs1			1	1	0	imm[4:1]	imm[1 1]	1	1		0	1	. 1
							PC	(tar	get) <	<= se	xt12	to32	2(im	m[12	2:0])	, if rs	1 <r< th=""><th>s2 (u</th><th>nsig</th><th>ned</th><th>com</th><th>parision)</th><th></th><th></th><th></th><th></th><th></th><th></th><th></th></r<>	s2 (u	nsig	ned	com	parision)							

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			fu	nct4			rd	/rs1				rs	2			0	р
CR type	C.MV	1	0	0	0		rd	(≠ 0)			rs2 (≠ 0)			1	0
		Reg[rd] = Reg[rs2]															
		funct3 Imm[5:3] rs1 Imm[2 6] rs2														0	р
CS type	C.SW	1	1	0	lmm[5:3]			rs1		Imm	[2 6]		rs2		0	0
			Mem	[Reg	[rs1] + {15'l	o0,Im	m[6:	2],2	'b0	}] =	Reg[rs	2]					
		fur	ict3					lm	ım[ː	10:0)]					0	р
CJ type	C.JALR	0	0	1		10:0)]					0	1				
			Reg	[x1] :	= PC + 3 (ne	ew PC	C), PC	= P	C +	sEx	t(Imm)						

Question 15:

Cache Specific	eations
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Back
Replacement policy	Pseudo LRU
Cache Type	Way Halting

Instructio n Type	Instructio n	3 1	3 0	2 9	2 8	2 7	2 6	2 5	2	2	2 2	2	2		1 8	1 7	1 6	1 5	1 4	1	1 2	1	1	9	8	7	6	5	4	3	2 :	1 0
, pc		_			unct				•		 m[4:	_ <u>-</u> 01				rs1				unct				rd					go	cod	<u> </u>	
	srai	0	1	0	0	0	0	0			amt[4					rs1			1	0	1			rd			0	0			0 :	1 1
		<u> </u>											g[rd] = Re	g[rs2	1] >>>	> sha	mt														
R type				f	unct	7					rs2					rs1			f	unct	3			rd					ор	cod	•	
	srl	0	0	0	0	0	0	0			rs2					rs1			1	0	1			rd			0	1	1	0	0 :	1 1
											F	Reg[r	d] =	Reg[rs1] >	>> Re	g[rs2][4:0]		•											
						ı	mm	[11:0]							rs1			f	unct	3			rd					ор	cod	•	
	addi						lmm[[11:0]]							rs1			0	0	0			rd			0	0	1	0	0 3	1 1
I type											R	eg[ro	l] = l	Reg[rs	51] +	sExt(lmm	[11:0)])													
	ori						lmm[[11:0]							rs1			1	1	0			rd			0	0	1	0	0 2	1 1
											R	eg[ro	l] = I	Reg[r	s1]	sExt(lmm	[11:0)])													
				lmı	n[11	:5]					rs2					rs1			f	unct	3		lmr	n[4:	0]				op	cod	<u> </u>	
S type	sb			lmi	n[11	:5]					rs2					rs1			0	0	0		Imr	n[4:	0]		0	1	0	0	0 1	1 1
		ı								Me	em[R	eg[rs	1] +	sExt(lmm	[11:0]])] =	Reg[ı	rs2][7	7:0]												
											In	ım												rd					op	cod	•	
U type	AUIPC									i														rd			0	0	1	0	1 1	1 1
		imm[31:12] Reg[rd												PC+	{imn	n[31:	12],1	2'd0	}													

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		f	unct	3	Imm[5]		rd	/rs1				lmm[4:0			0	р
CR type	C.JALR	1	0	0	1		rs1	(≠ 0))		0	0	0	0	0	1	0
		Reg[1] = PC + 3 (new PC), PC = Reg[rs1]															
																	р
CL type	C.LW	0	1	0	lmm[5:3]			rs1		Imm	[2 6]		rd		0	0
			Re	g[rd]	= Mem[Re	g[rs1] + {1	.5'b(O,Im	m[6	5:2],2'l	00}]					
		f	unct	3	Imm[8	4:3]		rs1		lm	m[7:6	2:1	L[5]		0	р
CB type	C.BNEZ	1	1	1	Imm[8	4:3			rs1		lm	m[7:6	2:1	[5]		0	1
				if	f(Reg[rs1]!	= 0) F	PC = F	PC +	sEx	t(Im	nm)						

Question 16:

Cache Specific	eations
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Back
Replacement policy	Pseudo LRU
Cache Type	Way Prediction

Instructio	Instructio	3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	1 0
n Type	n	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0									
				f	unct	7				lm	1[4:0)]				rs1			f	unct	3			rd					O	ocod	е	
	slli	0	0	0	0	0	0	0		shar	nt[4	:0]				rs1			0	0	1			rd			0	0	1	0	0	1 1
P type												Re	g[rd]] = Re	eg[rs	1] <<	shar	nt														
R type				f	unct	7					rs2					rs1			f	unct	3			rd					O	cod	е	
	or	0	0	0	0	0	0	0			rs2					rs1			1	1	0			rd			0	1	1	0	0	1 1
												Re	g[rd]	= Re	g[rs:	1] R	eg[rs	52]														
						ı	mm[11:0]							rs1			f	unct	3			rd					O	cod	е	
	lh						mm[11:0								rs1			0	0	1			rd			0	0	0	0	0	1 1
									Reg	[rd] =	sEx	t(Me	m[[F	Reg[r	s1] +	sExt(lmm	1[11:	0])] (:	16 bi	ts))											
I type	xori					ı	mm[11:0								rs1			1	0	0			rd			0	0	1	0	0	1 1
											Re	g[rd] = R	eg[rs	1] ^	sExt(I	mm	[11:0)])													
	jalr					I	mm[11:0								rs1			0	0	0			rd			1	1	0	0	1	1 1
								F	Reg[ro	d] = P	C + :	3 (ne	xt P	C), P(C = sE	Ext({Ir	nm[11:0],0}) -	- Re	g[rs1]										
											lm	m												rd					O	cod	е	
U type	LUI									in	nm[3	31:12	2]			•								rd			0	1	1	0	1	1 1
												Re	g[rd]	= {in	nm[3	1:12]	,12'	(0b														

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		funct3 Imm[5] rd/rs1 Imm[4:0]													0	р	
CR type	C.ADDI	0 0 0 Imm[5] rs1/rd (≠ 0)											4:0]			0	1
				Re	g[rd] = Reg	[rs1]	+ sEx	t(Im	ım[5:0]))						
		funct3 Imm[8 4:3] rs1 Imm[7:6 2:1 5] op														р	
CB type	C.BEQZ	1	1	0	Imm[8	4:3			rs1		lm	m[7:6	2:1	.[5]		0	1
				if(R	eg[rs1] == ()) PC	= PC	+ sE	Ext(I	mm	1)						
		fun	ct3		lmm[5:3]			rs1		lmm	[2 6]		rs2		0	р
CS type	C.SW	1	1	0	lmm[5:3]			rs1		Imm	[2 6]		rs2		0	0
			Mem	[Reg[rs1] + {15'b	0,lm	m[6:	2],2	'b0}	·] = [Reg[rs2	2]					

Question 17:

Cache Specifications											
Cache Size	1KB										
Cache Line Size	16B										
Associativity	4										
Write Policy	Write Back										
Replacement policy	Random										
Cache Type	Way Halting										

Instructi	Instructi	31	3	2	2	2	2	2	2	2 2	2 2	2	1	1	1	1	1	1	1	1	1	1	9 8	7		6 6	_	2	2	1 0
on Type	on	31	0	9	8	7	6	5	4	3 2	2 1	0	9	8	7	6	5	4	3	2	1	0	ه ا و	,		6 5	4	3	2	1 0
			funct7						Im[4:0]					rs1			funct3			rd					opcode					
	srai	0	1	0	0	0	0	0	shamt[4:0]				rs1				1	0	1	rd					0 0 1 0 0 1 1					
R type	Reg[rd] = Reg[rs1] >>> shamt																													
it type		funct7							rs2					rs1			funct3			rd				opcode						
	add	0	0	0	0	0	0	0		rs	2			rs1 0 0 0 rd							0 1 1 0 0 1 1									
	Reg[rd] = Reg[rs1] + Reg[rs2]																													
		Imm[11:0]												rs1				f	unct	3	rd				opcode					
	jalr	Imm[11:0]													rs1 0 0				0	0	rd					1 1 0 0 1 1				
I type		Reg[rd] = PC + 3 (next PC)												PC), PC = sExt({Imm[11:0],0}) + Reg[rs1]																
	andi					lmr	n[11	:0]							rs1			1	1	0		rd				0 0 1 0 0 1 1				1 1
											Reg[ro	d] = F	Reg[r	s1] &	sExt	t(Imi	m[11	L:0])												
			lı	mm[11:5]			rs2						rs1			f	unct	3	Imm[4:0]					opcode				
S type	sh		- 1	mm[11:5]			rs2						rs1			0	0	1	Imm[4:0]					0 1 0 0 0 1 1				
									1	∕lem[l	Reg[rs	1] + 9	sExt(lmm[11:0)])] =	Reg	[rs2]	[15:	0]	ı									
		lmm							rs2						rs1			funct3			lmm				opcode					
B type	BGE	imm[1 2]		i	mm[10:5]			rs	2				rs1			1	0	1	ir	mm[4	:1]	imm 1]	1	1 1	0	0	0	1 1
										PC(ta	rget) <	= se	xt12	to32(imm	ո[12։	0]),	if rs	1>rs	2										

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
			1	funct	4		rd	/rs1			rs2						р								
CR type	C.MV	1	0	0	0	rd (≠ 0)					rs2 (≠ 0)						0								
		Reg[rd] = Reg[rs2]																							
		f	unct	3	Imm[5]	rd					Imm[4:0]					ор									
CI type	C.LI	0	1	0	Imm[5]		rd	(≠ 0)		Imm[4:0]					0	1								
		Reg[rd] = sExt(Imm[5:0])																							
		f	unct	3	lmm[5:3]		rs1			Imm	rd			0	р									
CL type	C.LW	0	1	0	lmm[5:3]	5:3] rs1				Imm[2 6]			rd		0	0								
			Re	g[rd]	= Mem[Re	g[rs1] + {1	.5'b(O,Im	m[6	5:2],2'k	$Reg[rd] = Mem[Reg[rs1] + \{15'b0,Imm[6:2],2'b0\}]$													

Question 18:

Cache Specific	eations
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Back
Replacement policy	Random
Cache Type	Way Prediction

Instructio	Instructio	3	3	2	2	2	2	2	2	2	2	2	2	1	1	1 7	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	L O
n Type	n	1	0	9	8		6	5	4	3	2	1	0	9	8		6	5	4	3	2	1	0									
				f	unct	7				Ir	n[4:0	0]				rs1			f	unct	3		r	d					op	cod	е	
	srli	0	0	0	0	0	0	0		sha	mt[4	1:0]				rs1			1	0	1		r	d			0	0	1	0	0 :	l 1
D tuno												Re	g[rd] = Re	eg[rs	1] >>	shar	nt														
R type				f	unct	7					rs2					rs1			f	unct	3		r	d					op	cod	е	
	sltu	0	0	0	0	0	0	0			rs2					rs1			0	1	1		r	d			0	1	1	0	0 :	l 1
									Re	g[rd]	= (u	ınsigı	ned(Reg[r	s1]) ·	< uns	igne	d(Re	g[rs2]))?1	:0											
						ı	mm[11:0								rs1			f	unct	3		r	d					op	cod	е	
	addi					I	mm[11:0]								rs1			0	0	0		r	d			0	0	1	0	0 :	l 1
											Re	eg[rd] = R	eg[rs	1] + :	sExt(Imm	[11:0)])													
I type	lbu					I	mm[11:0]								rs1			1	0	0		r	d			0	0	0	0	0 :	l 1
									Reg[rd] =	{24	'b0,N	1em	[[Reg	[rs1]	+ sEx	kt(Im	m[1:	1:0])]	(8 b	its)}											
	xori					I	mm[11:0]								rs1			1	0	0		r	d			0	0	1	0	0 :	l 1
											Re	eg[rd] = R	eg[rs	1] ^	sExt(lmm	[11:0)])													
											lm	ım											r	d					op	cod	е	
U type	AUIPC									ir	nm[3	31:12	2]										r	d			0	0	1	0	1 :	l 1
											F	Reg[r	d] =	PC +	{imm	า[31::	12],1	2'd0	}													

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			fur	nct4			rd	/rs1				rs	2			0	р
CR type	C.JALR	1	0	0	1		rs1	(≠ C))		0	0	0	0	0	1	0
				Reg[1] = PC + 3	(new	PC),	PC =	= Re	g[rs	1]						
		Reg[1] = PC + 3 (new PC), PC = Reg[rs1] funct3														0	р
CB type	C.BEQZ	1	1	0	Imm[8	[4:3]			rs1		lm	m[7:6	2:1	.[5]		0	1
				if(R	eg[rs1] == () PC	= PC	+ sE	xt(I	mm	1)						
		fun	ict3		Imm	5:3]			rs1		Imm	[2 6]		rs2		0	р
CS type	C.SW	1	1	0	Imm	5:3]			rs1		Imm	[2 6]		rs2		0	0
			Mem	[Reg[rs1] + {15'k	0,lm	m[6:	2],2	'b0}] = F	Reg[rs2	2]					

Question 19:

Cache Specific	eations
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Buffer
Replacement policy	FIFO
Cache Type	Way Halting

Instructi on Type	Instructi on	31	3	2 9	2	2	2	2	2	2	2 2	2	2	1 9	1 8	1 7	1 6	1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2 1	1 0
on type	On			<u> </u>	ict7	<u> </u>			7		- 1[4:0					rs1		<u> </u>		unct	<u> </u>	-		r	d 				Or	code	<u> </u>	\dashv
	slli	0	0	0	0	0	0	0		shar						rs1			0					r			0	0	1			1 1
													eg[rd] = R	eg[r	s1] <	< sh	amt							-							
R type				fun	nct7						rs2		0.	•	<u> </u>	rs1			f	unct	3			r	d				or	code	:	
	add	0	0	0	0	0	0	0			rs2					rs1			0	0	0			r	d		0	1	1			1 1
												Re	g[rd]] = R	eg[rs	1]+	Reg[rs2]														
						lm	m[11	:0]								rs1			f	unct	3			r	d				op	code	;	
	jalr					lm	m[11	:0]								rs1			0	0	0			r	d		1	1	0	0	1 1	1 1
								R	.eg[ro	d] = P	C +	3 (ne	ext P	C), P	C = s	Ext((Imr	ո[11:	0],0	}) + F	Reg[r	s1]										
I type	xori					lm	m[11	:0]								rs1			1	0	0			r	d		0	0	1	0) 1	1 1
											Re	eg[rd] = R	leg[r	s1] ^	sExt	:(Imr	n[11	:0])													
	lh					lm	m[11	:0]								rs1			0	0	1			r	d		0	0	0	0) 1	1 1
									Reg[rd] =	sEx	t(Me	em[[I	Reg[rs1] -	+ sEx	t(Im	m[11	L:0])] (16	bits))										
				In	ım						rs2					rs1			f	unct	3			lm	ım				op	code	:	_
B type	BEQ	imm[1 2]		i	mm	[10:5]				rs2					rs1			0	0	0	ii	mm[4:1]]	imm[1 1]	1	1	0	0) 1	1 1
										PC(ta	arge	et) <=	sex	t12t	o3 <mark>2(</mark> i	imm	[12:0)]) , i	f rs1	==rs	2					·						

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		fur	ct3		Imm[5]		ı	rd				 	4:0			0	р
CI type	C.LI	0	1	0	Imm[5]		rd	(≠ 0)			lmm	4:0]			0	1
		Reg[rd] = sExt(Imm[5:0])															
		funct6 rd/rs1 funct rs2 op														р	
CR type	C.AND	1	0	0	0	1	1	r	d/rs	1	1	1		rs2		0	1
					Reg[rd] = F	leg[rs	31] &	Reg	[rs2	2]							
		fur	ct3		 	5:3]			rs1		Imm	[2 6]		rs2		0	р
CS type	C.SW	1	1	0	Imm[5:3]			rs1		Imm	[2 6]		rs2		0	0
			Mem	[Reg	[rs1] + {15'k	0,lm	m[6:	2],2	'b0}] = [Reg[rs:	2]					

Question 20:

Cache Specific	eations
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Buffer
Replacement policy	FIFO
Cache Type	Way Prediction

Instructio	Instructio	3	3	2	2	2	2	2	2	2	2 2	2	2	1	1	1 7	1	1	1	1	1 2	1	L (9 8	8	7	6	5	4	3	2 1	LO
n Type	n	1	0	9	8		О	5	4				U	9	8		6	5	4			1 ,										
				f	unct	7				In	า[4:0)]				rs1			f	unct	3		rd						op	code)	
	srli	0	0	0	0	0	0	0		sha	mt[4	:0]				rs1			1	0	1		rd				0	0	1	0	0 1	1 1
Datase												Re	g[rd]	= Re	g[rs:	L] >>	shan	nt														
R type				f	unct	7					rs2					rs1			f	unct	3		rd						ор	code	;	
	xor	0	0	0	0	0	0	0			rs2					rs1			1	0	0		rd				0	1	1	0	0 1	1
												Re	g[rd]	= Re	g[rs1	.] ^ Re	eg[rs	2]														
						I	mm[11:0								rs1			f	unct	3		rd						ор	code	:	
	addi					I	mm[11:0]								rs1			0	0	0		rd				0	0	1	0	0 1	1
											Re	g[rd]] = Re	g[rs:	1] + 9	Ext(I	mm[11:0])													
I type	jalr					I	mm[11:0]								rs1			0	0	0		rd				1	1	0	0	1 1	1
								R	leg[ro	d] = F	PC + 3	3 (ne	xt PC	:), PC	: = sE	xt({In	nm[:	11:0]	,0}) -	⊦ Re	g[rs1]										
	slti					I	mm[11:0]								rs1			0	1	0		rd				0	0	1	0	0 1	1
										F	Reg[r	d] =	(Reg[rs1]	< sEx	kt(lmi	m[11	L:0]))	?1:0													
				lmı	m[11	:5]					rs2					rs1			f	unct	3	Ir	nm[4:0]					ор	code	•	
S type	SW			lmı	m[11	:5]					rs2					rs1			0	0	1	Ir	nm[4:0]			0	1	0	0	0 1	1
										M	lem[Reg[rs1] +	- sExt	t(Imr	n[11:	0])]	= Re	g[rs2]												

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		f	unct	3	Imm[5]		ı	rd				Imm	4:0			0	р
CI type	C.LUI	0	1	1	Imm[5]		rd	(≠ 0)			lmm	4:0]			0	1
		Reg[rd] = sExt({Imm{5:0],12'b0})															
		Reg[rd] = SExt({Imm{5:0],12'b0}}) funct3															р
CB type	C.BNEZ	1	1	1	Imm[8	4:3			rs1		Im	m[7:6	2:1	.[5]		0	1
				i	f(Reg[rs1]!	= 0) F	PC = F	PC +	sEx	t(In	ım)						
		f	unct	3	Imm	[5:3]			rs1		lmm	[2 6]		rd		0	р
CL type	C.LW	0	1	0	lmm	[5:3]			rs1		Imm	[2 6]		rd		0	0
			Re	g[rd]	= Mem[Re	g[rs1] + {1	.5'b(O,Im	nm[6	5:2],2'l	o0}]					

Question 21:

Cache Specific	eations
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Buffer
Replacement policy	LRU counter
Cache Type	Way Halting

Instructi on Type	Instructi on	31	3	2 9	2	2 7	2	2 5	2	2	2 2	2	2	1 9	1 8	1 7	1 6	1 5	1 4	1 3	1 2	1 1 0 9 8	7	6	5	4 3	2	1	0
on type	0			fun					•	_	լ <u>-</u> n[4։					rs1				unct		rd				opco	de		=
	srai	0	1	0	0	0	0	0			mt[4					rs1			1	0	1	rd		0		1 0		1	1
	0.0												g[rd] = R	eg[rs		>> sh	namt				1.0						<u> </u>	
R type				fun	ct7						rs2		<u> </u>		0.	rs1				unct	:3	rd				орсс	de		П
	sub	0	1	0	0	0	0	0			rs2					rs1			0	0	0	rd		0		1 0	_	1	1
												Re	g[rd] = R	eg[r	s1] -	Reg[rs2]								ı			
						lmı	n[11	:0]								rs1			f	unct	:3	rd				орсс	de		
	addi					lmr	n[11	:0]								rs1			0	0	0	rd		0	0	1 0	0	1	1
											Re	eg[ro	[] = F	Reg[r	s1] +	sExt	t(Imr	n[11	:0])										
I type	jalr					lmr	n[11	:0]								rs1			0	0	0	rd		1	1	0 0	1	1	1
								R	eg[rd	[] = F	PC +	3 (n	ext P	C), F	C = 9	Ext({lmn	า[11:	:0],0	}) +	Reg[rs1]							
	sltiu					lmr	n[11	:0]								rs1			0	1	1	rd		0	0	1 0	0	1	1
										R	eg[r	d] =	(Reg	[rs1]	<{20)'b0,	lmm	[11:0	0]})?	1:0				ı					
				lm	m						rs2					rs1			f	unct	:3	Imm	,		1	opco	de	1 1	
B type	BLT	imm[1 2]		i	mm[10:5]				rs2					rs1			1	0	0	imm[4:1]	imm[1 1]	1	1	0 0	0	1	1
										PC(targ	et) <	= se	xt12	to32	(imm	1[12:	0]),	if rs	1 <rs< th=""><th>2</th><th></th><th></th><th></th><th></th><th></th><th>·</th><th></th><th></th></rs<>	2						·		

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			fur	nct4			rd	/rs1				rs	2			0	р
CR type	C.MV	1	0	0	0		rd	(≠ 0)			rs2 (≠ 0)			1	0
		Reg[rd] = Reg[rs2]															
		funct3														р	
CL type	C.LW	0	1	0	Imm	5:3]			rs1		Imm	[2 6]		rd		0	0
			Reg[ı	rd] =	Mem[Reg[ı	·s1] +	{15'l	اا,0c	mm	[6:2],2'b0}	·]					
		fun	ct3		Imm	5:3]			rs1		Imm	[2 6]		rs2		0	р
CS type	C.SW	1	1	0	Imm	5:3]			rs1		Imm	[2 6]		rs2		0	0
			Mem	[Reg[rs1] + {15'k	0,lm	m[6:	2],2	'b0}] = [Reg[rs2	2]					

Question 22:

Cache Specific	eations
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Buffer
Replacement policy	LRU counter
Cache Type	Way Prediction

Instructi on Type	Instructi on	31	3	2	2	2 7	2	2	2	2	2 2	2	2	1 9	1 8	1 7	1 6	1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3 2	2 1	L O
7,1			<u> </u>	fun	ct7						n[4:0					rs1				unct	<u> </u>			r	d				ор	code	<u> </u>	
	slli	0	0	0	0	0	0	0			mt[4					rs1			0	0	1			r	d		0	0	1			l 1
D tuno												Re	eg[rd] = R	leg[r	s1] <	< sh	amt														
R type				fun	ct7						rs2					rs1			f	unct	3			r	d				ор	code)	
	sltu	0	0	0	0	0	0	0			rs2					rs1			0	1	1			r	d		0	1	1	0 () 1	l 1
									Reg	[rd]	= (u	ınsig	ned(Reg[rs1])	< ur	nsigr	ned(I	Reg[rs2]))?1:0)										
						lmr	n[11	:0]								rs1			f	unct	3			r	d				ор	code	<u> </u>	
	addi					Imr	n[11	:0]								rs1			0	0	0			r	d		0	0	1	0 () 1	l 1
I type											Re	eg[rd] = F	leg[r	s1] +	· sExt	t(Imi	m[1:	L:0])													
	lh					lmr	n[11	:0]								rs1			0	0	1			r	d		0	0	0	0 () 1	l 1
									Reg[rd] =	sEx	t(Me	em[[I	Reg[rs1] ·	+ sEx	ct(Im	m[1	1:0]] (16	bits	())										
										ı	mm													r	d				ор	code	<u> </u>	
U type	LUI									imm	า[31:	12]												r	d		0	1	1	0 :	L 1	l 1
												Re	g[rd]	= {i	mm[31:1	2],12	2'd0	}													
		lmm									rs2					rs1			f	unct	3			lm	m				ор	code)	
B type	BLTU	imm[1 2]		i	mm[10:5]				rs2					rs1			1	1	0	ir	nm[4	4:1]	į	imm[1 1]	1	1	0	0 () 1	1 1
							PC	(tar	get) <	= se	ext12	2to32	2(im	m[12	2:0])	, if r	s1 <r< th=""><th>s2 (ι</th><th>ınsig</th><th>ned</th><th>com</th><th>paris</th><th>ion)</th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th></r<>	s2 (ι	ınsig	ned	com	paris	ion)									

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			fu	nct4			rd	/rs1				rs	2			0	р
CR type	C.MV	1	0	0	0		rd	(≠ 0)			rs2 (≠ 0)			1	0
		Reg[rd] = Reg[rs2] funct3 Imm[5:3] rs1 Imm[2 6] rs2															
		fur	nct3		Imm	[5:3]			rs1		lmm	[2 6]		rs2		0	р
CS type	C.SW	1	1	0	Imm	[5:3]			rs1		Imm	[2 6]		rs2		0	0
			Mem	[Reg	[rs1] + {15'l	o0,Im	m[6:	2],2	'b0]	}] =	Reg[rs	2]					
		fur	nct3					lm	nm[:	10:0)]					0	р
CJ type	C.JALR	0	0	1				lm	nm[:	10:0)]					0	1
			Reg	[x1] :	= PC + 3 (ne	ew PO	C), PC	= P	C +	sEx	t(Imm)						

Question 23:

Cache Specific	eations
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Buffer
Replacement policy	Pseudo LRU
Cache Type	Way Halting

Instructio	Instructio	3	3	2	2	2	2	2	2	2	2	2	2	2 1		1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	1 ()
n Type	n	1	0	9	8	7	6	5	4	3	2	1	() 9)	8	7	6	5	4	3	2	1	0		Ŭ			9	•	•	_		
				f	unct	7					Im[4	:0]					rs1			f	unct	3			rd					op	cod	е		
	srai	0	1	0	0	0	0	0		sł	namt	[4:0]					rs1			1	0	1			rd			0	0	1	0	0	1	1
Datumo												Re	eg[r	d] = F	Reg[[rs1]] >>>	sha	mt															
R type				f	unct	7					rs2						rs1			f	unct	3			rd					op	cod	е		
	srl	0	0	0	0	0	0	0			rs2						rs1			1	0	1			rd			0	1	1	0	0	1 :	1
												Reg[rd] :	= Reg	g[rs1	1] >>	> Reg	[rs2][4:0)]														
						l	mm[11:0]								rs1			f	unct	3			rd					op	cod	е		
	addi						mm[11:0]								rs1			0	0	0			rd			0	0	1	0	0	1 :	L
I type											F	leg[r	d] =	Reg[rs1]] + s	Ext(I	mm	[11:0)])														
	ori						mm[11:0]								rs1			1	1	0			rd			0	0	1	0	0	1	Ī
											F	Reg[r	d] =	Reg[[rs1]] s	Ext(I	mm	[11:0)])														
				lm	m[11	L: 5]					rs2	2					rs1			f	unct	3		lm	m[4	:0]				op	cod	е		
S type	sb			lm	m[11	.:5]					rs2						rs1			0	0	0		lm	m[4	:0]		0	1	0	0	0	1 :	Ĺ
										M	em[R	eg[r	s1] -	+ sEx	t(Im	nm[1	L1:0])] = [Reg[ı	rs2][ː	7:0]													
											lı	nm													rd					ор	cod	е		
U type	AUIPC											[31:1	.2]												rd			0	0	1	0	1	1 :	Ĺ
												Reg	rd]	= PC	+ {ir	mm	[31:1	2],1	2'd0	}														

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		f	unct	3	Imm[5]		rd	/rs1				lmm[4:0]			0	р
CR type	C.JALR	1	0	0	1		rs1	(≠ C)		0	0	0	0	0	1	0
		Reg[1] = PC + 3 (new PC), PC = Reg[rs1]															
		funct3														р	
CL type	C.LW	0	1	0	lmm[5:3]			rs1		Imm	[2 6]		rd		0	0
			Re	g[rd]	= Mem[Re	g[rs1] + {1	.5'b(O,Im	m[6	5:2],2'k	00}]					
		f	unct	3	Imm[8	4:3]		rs1		lm	m[7:6	2:1	.[5]		0	р
CB type	C.BNEZ	1	1	1	Imm[8	4:3			rs1		lm	m[7:6	2:1	.[5]		0	1
				if	f(Reg[rs1]!	= 0) F	PC = F	PC +	sEx	t(Im	nm)						

Question 24:

Cache Specific	eations
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Buffer
Replacement policy	Pseudo LRU
Cache Type	Way Prediction

Instructio n Type	Instructio n	3 1	3 0	2 9	2 8	2 7	2 6	2	2 4	2	2 2	2	2 0	1 9	1 8	1 7	1 6	1 5	1 4	1	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0
				f	unct	7				Ir	n[4:0	0]				rs1			f	unct	3			rd					O	ocod	е		
	slli	0	0	0	0	0	0	0		sha	mt[4	1:0]				rs1			0	0	1			rd			0	0	1	0	0	1	1
Datama												Re	g[rd] = Re	eg[rs	1] <<	sha	mt															
R type				f	unct	7					rs2					rs1			f	unct	3			rd					O	ocod	е		
	or	0	0	0	0	0	0	0			rs2					rs1			1	1	0			rd			0	1	1	0	0	1	1
												Re	g[rd]	= Re	g[rs:	1] F	Reg[r	s2]															
						ı	mm[11:0]							rs1			f	unct	3			rd					O	ocod	е		
	lh					ı	mm[11:0]							rs1			0	0	1			rd			0	0	0	0	0	1	1
									Reg[[rd] =	= sEx	t(Me	m[[l	Reg[r	s1] +	sExt	(Imn	า[11:	0])](16 b	its))												
I type	xori					ı	mm[11:0]							rs1			1	0	0			rd			0	0	1	0	0	1	1
											Re	eg[rd] = R	eg[rs	1] ^	sExt(lmm	[11:0)])														
	jalr					١	mm[11:0]							rs1			0	0	0			rd			1	1	0	0	1	1	1
								F	Reg[ro	l = [b	PC +	3 (ne	ext P	C), P(C = sl	Ext({I	mm	11:0],0}) -	+ Re	g[rs1]											
											lm	ım												rd					O	ocod	е		
U type	LUI									ir	nm[31:12	2]											rd			0	1	1	0	1	1	1
												Re	g[rd]	= {in	nm[3	1:12],12'	d0}															

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		fun	ct3		Imm[5]		rd	/rs1				Imm	4:0			0	р
CR type	C.ADDI	0	0	0	Imm[5]		rs1/r	d (≠	0)			Imm	4:0]			0	1
		Reg[rd] = Reg[rs1] + sExt(Imm[5:0]) funct3															
		funct3 Imm[8 4:3] rs1 Imm[7:6 2:1 5] op														р	
CB type	C.BEQZ	1	1	0	Imm[8	4:3			rs1		lm	m[7:6	2:1	.[5]		0	1
				if(R	eg[rs1] == ()) PC	= PC	+ sE	Ext(I	mm	1)						
		fun	ct3		lmm[5:3]			rs1		lmm	[2 6]		rs2		0	р
CS type	e C.SW 1 1 0 Imm[5:3] rs1										Imm	[2 6]		rs2		0	0
			Mem	[Reg[rs1] + {15'b	0,lm	m[6:	2],2	'b0}	·] = [Reg[rs2	2]					

Question 25:

Cache Specific	eations
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Buffer
Replacement policy	Random
Cache Type	Way Halting

Instructi	Instructi	31	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	9	8	7	6 5	4	3	2	1	0
on Type	on	31	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	0		0 3	4	3	2	_	U
				fun	ct7					In	ո[4:0)]				rs1				func	t3			r	ď			0	ococ	le		
	srai	0	1	0	0	0	0	0		shai	mt[4	1:0]				rs1			1	0	1			r	ď		0 0	1	0	0	1	1
P typo												Re	g[ro	d] = R	eg[rs	1] >	>> s	ham	nt													
R type				fun	ct7						rs2					rs1				func	t3			r	ď			0	ococ	le		
	add	0	0	0	0	0	0	0			rs2					rs1			0	0	0			r	ď		0 1	. 1	0	0	1	1
												Re	g[ro	d] = R	eg[r	s1] +	Reg	[rs2	2]													
			n[11	:0]								rs1				func	t3			r	ď			0	ococ	le						
	jalr		n[11	:0]								rs1			0	0	0			r	ď		1 1	. 0	0	1	1	1				
I type								R	eg[ro	l] = P	C +	3 (ne	ext	PC), F	C = 9	Ext(({Imr	n[1	1:0],)}) +	Reg[rs1]										
	andi					lmr	n[11	:0]								rs1			1	1	0			r	ď		0 0	1	0	0	1	1
											Re	g[rd] =	Reg[r	s1] 8	k sEx	kt(Im	m[1	11:0])												
			I	mm[11:5]					rs2					rs1				func	t3		I	mm	[4:0]		0	ococ	le		
S type	sh		I	mm[11:5]					rs2					rs1			0	0	1		- 1	mm	[4:0]	0 1	. 0	0	0	1	1
										Mem	[Re	g[rs1	<u>[]</u> +	sExt(lmm	[11:0	0])] =	= Re	g[rs2	2][15	:0]											
		Imm									rs2					rs1				func	t3			In	nm			0	ococ	e		
B type	BGE	GE imm[1 imm[10:5]				rs2					rs1			1	0	1	iı	mm[4:1]	imm 1]	1 1	. 0	0	0	1	1
										PC(t	arge	et) <	= se	ext12	to32	(imn	n[12	:0])	, if r	1>rs	2											

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			1	funct	4		rd	/rs1				rs	2			0	р
CR type	C.MV	1	0	0	0		rd	(≠ 0)			rs2 (≠ 0)			1	0
		Reg[rd] = Reg[rs2]															
		funct3 Imm[5] rd Imm[4:0]														0	р
CI type	C.LI	0	1	0	Imm[5]		rd	(≠ 0)			lmm[4:0]			0	1
					Reg[ro	d] = s	Ext(Ir	nm[5:0])							
		f	unct	3	lmm[5:3]			rs1		Imm	[2 6]		rd		0	р
CL type	C.LW														0	0	
			Re	g[rd]	= Mem[Re	g[rs1] + {1	.5'b(O,Im	m[6	5:2],2'k	00}]					

Question 26:

Cache Specific	eations
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Buffer
Replacement policy	Random
Cache Type	Way Prediction

Instructio n Type	Instructio n	3 1	3 0	2 9	2 8	2 7	2 6	2 5	2	2 3	2 2	2 1	2 0	1 9	1 8	1 7	1 6	1 5	1 4	1 3	1 2	L)	9	8	7	6	5	4	3	2	1	0
				f	unct	7				lm	[4:0)]				rs1			f	unct	3	r	rd	ı	ı			0	pcod	е		
	srli	0	0	0	0	0	0	0		shar	nt[4	:0]				rs1			1	0	1	r	rd			0	0	1	0	0	1	1
P type												Re	g[rd]	= Re	eg[rs	1] >>	shar	nt														
R type				f	unct	7					rs2					rs1			f	unct	3	r	r d					0	pcod	e		
	sltu	0	0	0	0	0	0	0			rs2					rs1			0	1	1	r	rd			0	1	1	0	0	1	1
									Re	g[rd]	= (u	nsigr	ned(F	Reg[r	s1])	< uns	igne	d(Re	g[rs2]))?1	:0											
						I	mm[11:0								rs1			f	unct	3	r	r d					0	pcod	е		
	addi						mm[11:0								rs1			0	0	0	r	rd			0	0	1	0	0	1	1
											Re	g[rd]] = R	eg[rs	1]+:	sExt(l	mm	[11:0)])													
I type	lbu						mm[11:0]								rs1			1	0	0	r	rd			0	0	0	0	0	1	1
									Reg[rd] =	{24'	b0,N	1em[[Reg	[rs1]	+ sEx	t(Im	m[1:	1:0])]	(8 b	its)}											
	xori						mm[11:0]								rs1			1	0	0	r	rd			0	0	1	0	0	1	1
											Re	g[rd]] = R	eg[rs	1] ^	sExt(mm	[11:0)])													
											lm	m										r	rd					0	pcod	е		
U type	AUIPC									in	nm[3	1:12	!]									r	rd			0	0	1	0	1	1	1
											R	eg[r	d] = I	PC + ·	{imn	n[31::	L2],1	2'd0	}													

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			fur	nct4			rd	/rs1				rs	2			0	р
CR type	C.JALR	1	0	0	1		rs1	(≠ C))		0	0	0	0	0	1	0
				Reg[1] = PC + 3	(new	PC),	PC =	= Re	g[rs	1]						
		Reg[1] = PC + 3 (new PC), PC = Reg[rs1] funct3													р		
CB type	C.BEQZ	1	1	0	Imm[8	[4:3]			rs1		lm	m[7:6	2:1	.[5]		0	1
				if(R	eg[rs1] == () PC	= PC	+ sE	xt(I	mm	1)						
		fun	ict3		Imm	5:3]			rs1		Imm	[2 6]		rs2		0	р
CS type	C.SW	1	1	0	Imm	5:3]			rs1		Imm	[2 6]		rs2		0	0
			Mem	[Reg[rs1] + {15'k	0,lm	m[6:	2],2	'b0}] = F	Reg[rs2	2]					

Question 27:

Cache Specific	eations
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Buffer
Replacement policy	FIFO
Cache Type	Way Halting

Instructio	Instructio	3	3	2	2	2	2	2	2	2	2	2		2	1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	1	0
n Type	n	1	0	9	8	7	6	5	4	3	2	1		0	9	8	7	6	5	4	3	2	1	0		0		U	,	7	,			
				f	unct	7					Im[4	:0]					rs1			f	unct	3			rd					op	cod	е		
	slli	0	0	0	0	0	0	0		sł	namt	[4:0]					rs1			0	0	1			rd			0	0	1	0	0	1	1
Datuma												F	Reg	[rd] :	= Re	g[rs	1] <<	shar	nt															
R type				f	unct	7					rs2	2					rs1			f	unct	3			rd					op	cod	е		
	or	0	0	0	0	0	0	0			rs2	2					rs1			1	1	0			rd			0	1	1	0	0	1	1
												R	eg[rd] =	= Re	g[rs1	L] R	eg[r	s2]															
						ı	mm[11:0]								rs1			f	unct	3			rd					op	cod	е		
	jalr					ı	lmm[11:0]								rs1			0	0	0			rd			1	1	0	0	1	1	1
I type								F	Reg[r	d] =	= PC -	+ 3 (r	next	t PC)), PC) = sE	xt({I	mm[11:0],0})	+ Re	g[rs1]]											
	sltiu					I	lmm[11:0]								rs1			0	1	1			rd			0	0	1	0	0	1	1
											Reg[rd] =	= (R	eg[rs	s1] <	<{20'	b0,In	nm[1	1:0]	})?1:)													
				lmı	m[11	.:5]					rs2	2					rs1			f	unct	3		lm	m[4:	0]				op	cod	е		
S type	sb			lmı	m[11	.:5]					rs2	2					rs1			0	0	0		lm	ո[4։	0]		0	1	0	0	0	1	l
										M	lem[F	leg[r	's1]	+ sE	xt(lı	mm[11:0)] =	Reg[ı	rs2][7	7:0]													
											lmn	ո[19։	:0]												rd					op	cod	е		
J type	JAL										imn	10:	:0]												rd			1	1	0	1	1	1	1
								Р	C(tar	rget	t) <= :	sext2	20tc	32(imm	1[20:	0]) +	PC, ı	rd = 1	PC+	3 (ne	w PC	C)											

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				funct	:4		rd	/rs1				rs	2			0	р
CR type	C.MV	1	0	0	0		rd	(≠ 0)			rs2 (≠ 0)			1	0
					Re	g[rd]	= Re	g[rs:	2]								
		Reg[rd] = Reg[rs2] funct3 Imm[5:3] rs1 Imm[2 6] rd o														p	
CL type	C.LW	0	1	0	lmm[[5:3]			rs1		Imm	[2 6]		rd		0	0
			Re	g[rd]	= Mem[Re	g[rs1] + {1	.5'b(O,Im	ım[6	5:2],2'l	o0}]					
		f	unct	3	Imm[5]		rd	/rs1				lmm[4:0			0	p
CI type	C.ADDI	0	0	0	Imm[5]		rs1/r	d (≠	0)			lmm[4:0]			0	1
				ı	Reg[rd] = Re	eg[rs	1] + s	Ext(lmr	n[5:	0])						

Question 28:

Cache Specific	eations
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Buffer
Replacement policy	FIFO
Cache Type	Way Prediction

Instructi on Type	Instructi on	31	3	2 9	2 8	2 7	2 6	2	2 4	2 3	2 2	2	2	1 9	1 8	1 7	1 6	1 5	1 4	1 3	1 2	1 1 0 9 8	7	6 5	3 4	3	2	1	0
				fun	ct7	ı				Im	[4:0)]				rs1			f	unct	:3	rd	•		C	рсос	le		
	srai	0	1	0	0	0	0	0		shar	nt[4	:0]				rs1			1	0	1	rd		0 0	1	0	0	1	1
D tuno												Re	g[rd]	= R	eg[rs	1] >>	>> sł	namt											
R type				fun	ct7						rs2					rs1			f	unct	:3	rd			C	рсос	le		
	or	0	0	0	0	0	0	0			rs2					rs1			1	1	0	rd		0 1	. 1	0	0	1	1
												Re	g[rd]] = R	eg[rs	3]	Reg	[rs2]											
						lmr	n[11	:0]								rs1			f	unct	:3	rd			C	рсос	le		
	jalr					lmr	n[11	:0]								rs1			0	0	0	rd		1 1	. C	0	1	1	1
I type								R	eg[rd	l] = P	C + 3	3 (ne	xt P	C), P	C = 9	Ext({lmn	n[11	:0],0	}) +	Reg[rs1]							
	lh					lmr	n[11	:0]								rs1			0	0	1	rd		0 0) (0	0	1	1
									Reg[rd] =	sExt	t(Me	m[[l	Reg[rs1] ·	+ sEx	t(Im	m[1	1:0]] (1	6 bits	5))		_					
										lı	mm											rd			C	рсос	le		
U type	AUIPC									imm	[31::	12]										rd		0 0) 1	0	1	1	1
											R	eg[r	d] =	PC+	· {imı	m[31	:12]	,12'c	(0t										
				lm	m						rs2					rs1			f	uncl	:3	Imm			C	рсос	le		
B type	BNE	imm[1 2]		i	mm[10:5]				rs2					rs1			0	0	1	imm[4:1]	imm[1 1]	1 1	. C	0	0	1	1
									- 1	PC(ta	rget	:) <=	sext	:12tc	32(i	mm[12:0)]) , i	f rs1	=/=r	s2								

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		fur	nct3		Imm[5]		rd	/rs1				lmm	4:0]			0	р
CR type	C.ADDI	0	0	0	Imm[5]		rs1/r	d (≠	0)			lmm[4:0]			0	1
		Reg[rd] = Reg[rs1] + sExt(Imm[5:0]) funct3															
		fur	nct3			lmm	[2 6]		rs2		0	р					
CS type	C.SW	1	1	0	lmm[5:3]			rs1		Imm	[2 6]		rs2		0	0
			Mem	[Reg	[rs1] + {15'k	o0,Im	m[6:	2],2	'b0	}] =	Reg[rs	2]					
		fur	nct3		Imm[5]		ı	rd				lmm	4:0			0	р
CI type	C.LI	0	1	0	Imm[5]		rd ((≠ 0)			lmm[4:0]			0	1
					Reg[rd] :	= sEx	t(Imn	ո[5:	0])								

Question 29:

Cache Specific	eations
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Buffer
Replacement policy	LRU counter
Cache Type	Way Halting

Instructio	Instructio	3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	1	0
n Type	n	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	0	′	0	3	4	3	_	1	۱,
				f	unct	7				In	ո[4:0)]				rs1			f	unct	3		ı	rd					op	cod	е		
	srli	0	0	0	0	0	0	0		shai	mt[4	:0]				rs1			1	0	1		ı	rd			0	0	1	0	0	1	1
Datum												Re	g[rd]	= Re	eg[rs	1] >>	shan	nt															
R type				f	unct	7					rs2					rs1			f	unct	3		ı	rd					op	cod	е		
	sra	0	1	0	0	0	0	0			rs2					rs1			1	0	1		ı	rd			0	1	1	0	0	1	1
											Re	eg[rd] = R	eg[rs	1] >:	>> Re	g[rs2	2][4:0	0]														
						ı	mm[11:0]								rs1			f	unct	3			rd					op	cod	е		
	lw					ı	mm[11:0]								rs1			0	1	0			rd			0	0	0	0	0	1	1
									R	eg[ro	l] = N	Mem	[[Re	g[rs1]] + s[xt(In	ոm[1	1:0])] (32	bits)												
I type	addi					I	mm[11:0]								rs1			0	0	0		I	rd			0	0	1	0	0	1	1
											Re	g[rd] = Re	eg[rs	1]+:	sExt(I	mm[11:0)])														
	andi					I	mm[11:0]								rs1			1	1	0		ı	rd			0	0	1	0	0	1	1
											Re	g[rd]	= Re	eg[rs:	1] &	sExt(Imm	[11:0)])														
											lm	m											ı	rd					op	cod	е		
U type	AUIPC									in	nm[3	31:12	.]										ı	rd			0	0	1	0	1	1	1
											R	leg[r	d] = F	PC +	(imm	[31:1	L2],1	2'd0	}														

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			fur	nct4			rd	/rs1				rs	2			0	р
CR type	C.MV	1 0 0 0 rd (≠ 0) rs2 (≠ 0)													1	0	
					Reg[r	d] = I	Reg[r	s2]									
		Reg[rd] = Reg[rs2] funct3 Imm[8 4:3] rs1 Imm[7:6 2:1 5] o													р		
CB type	C.BNEZ	1	1	1	Imm[8	[4:3]			rs1		lm	m[7:6	2:1	[[5]		0	1
				if(R	eg[rs1] != ()) PC	= PC	+ sE	xt(I	mm)						
		fur	ict3		Imm	5:3]			rs1		Imm	[2 6]		rs2		0	р
CS type	C.SW	1	1	0	Imm	5:3]			rs1		Imm	[2 6]		rs2		0	0
			Mem	[Reg[[rs1] + {15'k	0,lm	m[6:	2],2	'b0}] = [Reg[rs2	2]					

Question 30:

Cache Specific	eations
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Buffer
Replacement policy	LRU counter
Cache Type	Way Prediction

Instructi on Type	Instructi on	31	3	2 9	2 8	2 7	2	2 5	2 4	2	2 2	2	2	1 9	1 8	1 7	1 6	1 5	1 4	1	1 2	1	1 0	9 8	3	7	6	5	4	3	2 :	1 0
7.			1	fun	ct7	l	l			I	ո[4:0	0]				rs1				unct				rd	ı			II	op	cod	9	1
	srai	0	1	0	0	0	0	0		sha	mt[4	1:0]				rs1			1	0	1			rd			0	0	1	0	0 1	1 1
P type												Re	g[rd]] = R	eg[r	s1] >:	>> sł	namt														
R type				fun	ct7						rs2					rs1			f	unct	:3			rd					op	cod	2	_
	sub	0	1	0	0	0	0	0			rs2					rs1			0	0	0			rd			0	1	1	0	0 2	1 1
												Re	g[rd] = R	eg[r	s1] -	Reg	[rs2]														
						lmı	m[11	:0]								rs1			f	unct	:3			rd					op	cod	9	_
	jalr					lmı	n[11	:0]								rs1			0	0	0			rd			1	1	0	0	1 1	1 1
I type								R	eg[ro	[] = F	PC +	3 (ne	ext P	C), P	C =	sExt({Imr	n[11	:0],0	}) +	Reg[rs1]										
	lbu					lmı	m[11	:0]								rs1			1	0	0			rd			0	0	0	0	0 2	1 1
									Reg[r	d] =	{24'	b0,N	⁄lem	[[Re	g[rs1	L] + s	Ext(I	mm	[11:0)])](8 bit	s)}										
										I	mm													rd					op	cod	.	
U type	AUIPC									imm	[31:	12]												rd			0	0	1	0	1 1	1 1
											F	Reg[r	d] =	PC+	· {im	m[31	L:12]	,12'	{0b													
				lm	m						rs2					rs1			f	unct	:3			Imm	1				op	cod	.	
B type	BGEU	imm[1 2]		i	mm[10:5	[]				rs2					rs1			1	1	1	in	nm[4	l:1]	in	nm[1 1]	1	1	0	0	0 2	1 1
							PC	(tar	get) <	<= se	xt12	2to3	2(im	m[12	2:0])	, if r	s1>r	s 2 (u	ınsig	ned	com	parisi	ion)									

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		fur	nct3		Imm[5]		rd	/rs1				lmm[4:0]			0	р
CR type	C.JALR	1 0 0 1 $rs1 \neq 0$ 0 Reg[1] = PC + 3 (new PC), PC = Reg[rs1]											0	0	0	1	0
				Reg[1] = PC + 3	(new	PC),	PC:	= Re	g[rs	51]						
		fur	nct3		lmm[5:3]			rs1		Imm	[2 6]		rs2		0	р
CS type													0	0			
			Mem	[Reg	[rs1] + {15'k	o0,Im	m[6:	2],2	'b0]	}] =	Reg[rs	2]					
		fur	nct3					lm	ım[:	10:0)]					0	р
CJ type	C.JALR															0	1
			Reg	[x1] =	= PC + 3 (ne	ew PC	C), PC	= P	C +	sExt	(Imm)						

Question 31:

Cache Specific	eations
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Buffer
Replacement policy	Pseudo LRU
Cache Type	Way Halting

	structi	31	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	9 8	,	7	6	5	4	3	2 :	ιο			
on Type	on	31	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9 6	•	,	6	3	4	3	-	1 0			
				fun	ct7					In	ո[4:0)]				rs1			f	unct	3			rd					ор	code)				
	slli	0	0	0	0	0	0	0		shai	mt[4	:0]				rs1			0	0	1			rd			0	0	1	0	0 :	1 1			
Datama												Re	g[rd] = R	eg[rs	51] <	< sha	amt																	
R type				fun	ct7						rs2					rs1			f	unct	3			rd					ор	code	•				
9	sltu	0	0	0	0	0	0	0			rs2					rs1			0	1	1			rd			0	1	1	0	0 1	1 1			
									Reg	[rd]	= (uı	nsigr	ned(Reg[rs1])	< ur	nsign	ed(F	Reg[ı	rs2]))?1:0)													
						lmr	n[11	:0]								rs1			f	unct	3			rd					ор	code	•				
	lb					lmr	n[11	:0]								rs1			0	0	0			rd			0	0	0	0	0 1	1 1			
I type									Reg[rd] =	= sEx	t(Me	em[[Reg[rs1]	+ sEx	xt(Im	nm[1	1:0])] (8	bits)													
,	xori					lmr	n[11	:0]								rs1			1	0	0			rd			0	0	1	0	0 (1 1			
											Re	g[rd] = R	eg[r	s1] ^	sExt	(Imr	n[11	:0])																
			lr	nm[11:5]					rs2					rs1			f	unct	3		Ir	nm[4	:0]				ор	code	•				
S type	sh		lı	nm[11:5]					rs2					rs1			0	0	1		Ir	nm[4	:0]		0	1	0	0	0 2	1 1			
	<u> </u>								١	Иem	n[Reg	g[rs1] + s	Ext(I	mm[11:0])] =	Reg	[rs2][15:	0]														
		Imm									rs2					rs1			f	unct	3			lmn	1				ор	code	•				
B type E	BLT	imm[1 2]		iı	mm[10:5]				rs2					rs1			1	0	0	ir	nm[4	1:1]	ir	nm[1 1]	1	1 1 0 0 0 1							
										PC(t	targe	et) <=	= sex	t12t	o32(imm	[12:	0]),	if rs	1 <rs< th=""><th>2</th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th></rs<>	2														

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				funct	:4		rd	/rs1				rs	s 2			0	р
CR type	C.ADD														1	0	
					Reg[rd] =	Reg	[rs1]	+ Re	g[r	s2]							
		f	unct	3	Imm[5]		ı	ď				lmm	[4:0)]		0	р
CI type	C.LUI	0	1	1	Imm[5]		rd	(≠ 0)			lmm	[4:0)]		0	1
					Reg[rd] = s	Ext({	lmm{	5:0]	,12	'b0})						
		f	unct	3				lm	m[1	0:0]						0	р
CJ type	C.J														0	1	
					PC =	PC+	sExt(Imr	n)								

Question 32:

Cache Specific	eations
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Buffer
Replacement policy	Pseudo LRU
Cache Type	Way Prediction

Instructio n Type	Instructio n	3 1	3	2 9	2 8	2 7	2 6	2 5	2 4	2 3	2 2	2 1	2 0		1 8	1 7	1 6	1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	,	6 5	4	3	2	1	0
				f	unct	7				ı	Im[4:	0]				rs1			1	unct	3			rd					C	рсо	de		
	srli	0	0	0	0	0	0	0		sh	namt[4:0]				rs1			1	0	1			rd				0 0	1	0	0	1	1
D tuno												Re	eg[ro	d] = R	eg[rs	1] >>	sha	mt															
R type				f	unct	7					rs2					rs1			f	unct	:3			rd					(рсо	de		
	xor	0	0	0	0	0	0	0			rs2					rs1			1	0	0			rd				0 1	1	0	0	1	1
												Re	eg[rd	l] = Re	eg[rs:	1] ^ R	eg[r	s2]															
							lmm[11:0]							rs1			1	unct	:3			rd					(рсо	de		
	jalr						lmm[11:0]							rs1			0	0	0			rd				1 1	0	0	1	1	1
I type								F	Reg[r	d] =	PC +	3 (n	ext F	PC), P	C = s	Ext({I	mm[11:0],0})	+ Re	g[rs1]											
	addi						lmm[11:0]							rs1			0	0	0			rd				0 0	1	0	0	1	1
											R	eg[ro	1 = [k	Reg[rs	s1] +	sExt(lmm	[11:0)])														
				lm	m[11	L:5]					rs2					rs1			ſ	unct	:3	ı	lmr	n[4:	:0]				C	рсо	de		
S type	SW			lm	m[11	L:5]					rs2					rs1			0	0	1	ı	lmr	n[4:	0]			0 1	0	0	0	1	1
											Mem	[Reg	[rs1]] + sEx	kt(Im	m[11	:0])]	= Re	g[rs2	2]													
											Ir	nm												rd					(рсо	de		
U type	AUIPC									i	imm	31:1	2]				·							rd				0 0	1	0	1	1	1
												Reg[ı	rd] =	PC +	{imn	า[31::	12],1	2'd0	}														

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				funct	:4		rd	/rs1				rs	2			0	р
CR type	C.MV	1	0	0	0		rd	(≠ 0)			rs2 (≠ 0)			1	0
					Re	g[rd]	= Re	g[rs:	2]								
		f	unct	3	lmm[5:3]			rs1		Imm	[2 6]		rd		0	р
CL type	C.LW	0	1	0	lmm[5:3]			rs1		Imm	[2 6]		rd		0	0
			Re	g[rd]	= Mem[Re	g[rs1] + {1	.5'b(O,Im	m[6	5:2],2'l	00}]					
		f	unct	3	Imm[8	4:3			rs1		lm	m[7:6	2:1	L[5]		0	р
CB type	C.BEQZ	QZ 1 1 0 Imm[8 4:3] rs1 Imm[7:6 2:1 5] 0													0	1	
				if	(Reg[rs1] =	= 0) I	PC = I	PC +	sEx	t(In	nm)						