EE310
POWER SYSTEMS LAB

IEEE 14 BUS SYSTEM

Submitted by:

Group 5 (Batch 2)

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DECLARATION

We declare that this written submission represents our ideas in our own words and where others' ideas or words have been included, I have adequately cited and referenced the original sources. We also declare that we have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. We understand that any violation of the above will be cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

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OVERVIEW

The IEEE 14 Bus system is exemplar power system that is widely used for power system analysis and simulation. It is the illustration of the power system in real world that was created in the 1970s by the Institute of Electrical and Electronics Engineers (IEEE). The IEEE 14 Bus System serves as a standard system for researchers to gain a better understanding of concepts and implement new ideas in the power system. Sudden disturbances can occur in the network due to changes in load or line switching, which can be detrimental to the system and consumers. Fault analysis is crucial for stability analysis as insulation failure can lead to faults. Therefore, we have conducted a study on fault analysis of the IEEE 14 Bus System.

In this project, we have created a model of the IEEE 14 Bus system in PSCAD using Tline modeling. The main objective of this project is to observe the voltages and currents at all the buses and transmission lines under normal operating conditions and during a 3 phase LLL symmetrical fault between Bus 5 and Bus 4. We have also analyzed the breaker currents, active and reactive power at Bus 5 during all the scenarios.

COMPONENTS and EQUIPMENTS

COMPONENTS USED	
	Load
	Multimeter
	Generator
	Current label and Output channel
	Bergeon Model Transmission line

PROBLEM STATEMENT

1. Create an IEEE 14 Bus system in PSCAD (Use T-line modeling). The datasheet for the 14 Bus system has been attached along with it.
    a. Observe the voltages and currents at all the buses and transmission lines
2. Create a 3-phase LLL symmetrical fault between Bus 5 and Bus 4 in the middle at time 1=0.2 sec and clear the fault at t=0.4 sec.
    a. Observe voltages at all the buses
    b. Breaker Currents pre, post and during fault conditions
    c. Active and Reactive power at bus five during all the scenarios

Modeling of IEEE 14 Bus System

We built a model of the IEEE 14 Bus System in PSCAD using Tline modeling. Data sheet tp built the same was provided to us, and we have assumed data wherever required. The single-line diagram of the IEEE 14 Bus system is shown below

The following are the features of IEEE 14 Bus System:

1. There are 14 buses, 5 generators, and 11 loads in the IEEE 14 bus system
2. Buses 1, 2, 3, 6 and 8 are link to the generator
3. Buses 2, 3, 4, 5, 6, 9, 10, 11, 12, 13 and 14 are connect the load
4. The system has 20 transmission lines with various line heights and impedance

Loads are modelled as a constant PQ load and Transmission lines are modelled using the Bergeron model.

For building the model we first used the bus from the component panel, we created a new module (i.e. the black box) in which we created the bergeon model of transmission line from the given data to keep the circuit neat and clean. Further we used multimeter to measure the voltages and current at all the buses, since multimeter doesnt directly display the value of current hence we need data label and output channel to get the waveform of the current and check current.
For question 2 we further modified the circuit to create a 3-phase LLL fault from t= 0.2s to t=0.4sand studied the current behavious and voltage behavious during and after the fault is cleared.

CURCUIT DIAGRAM

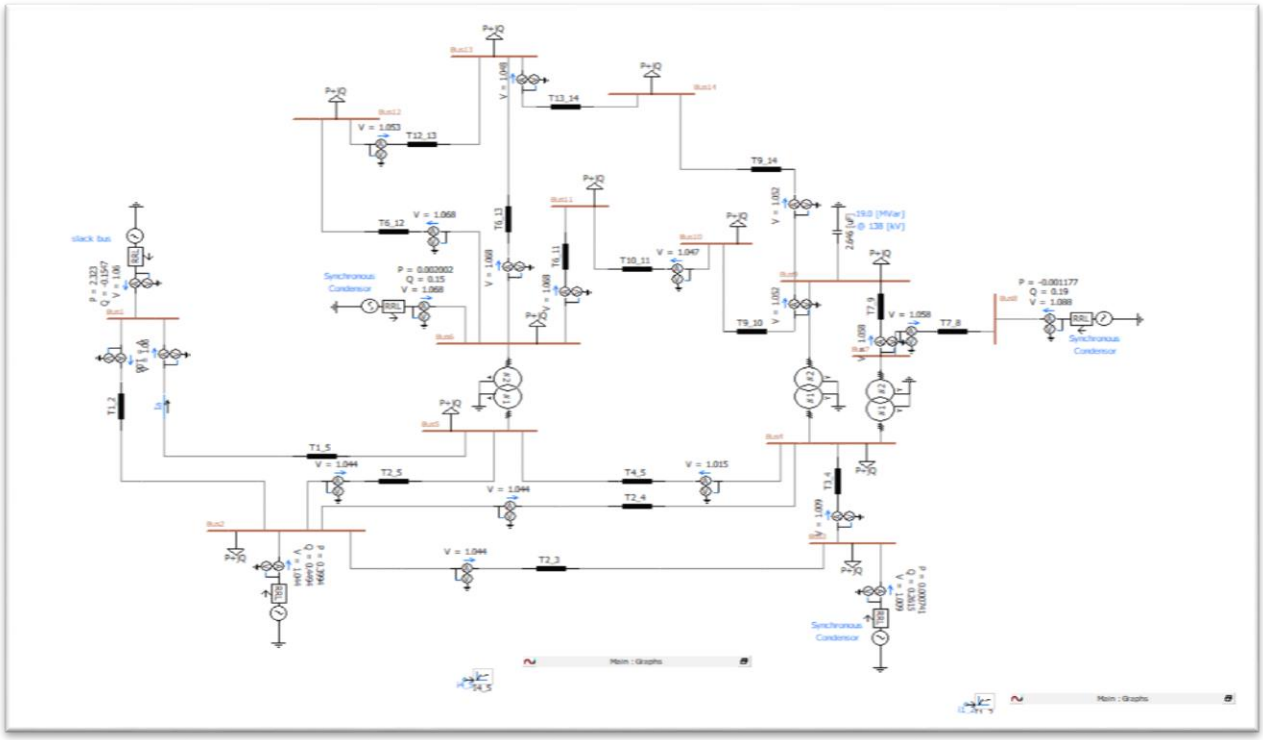


Fig 1. *Circuit Diagram (without fault)*

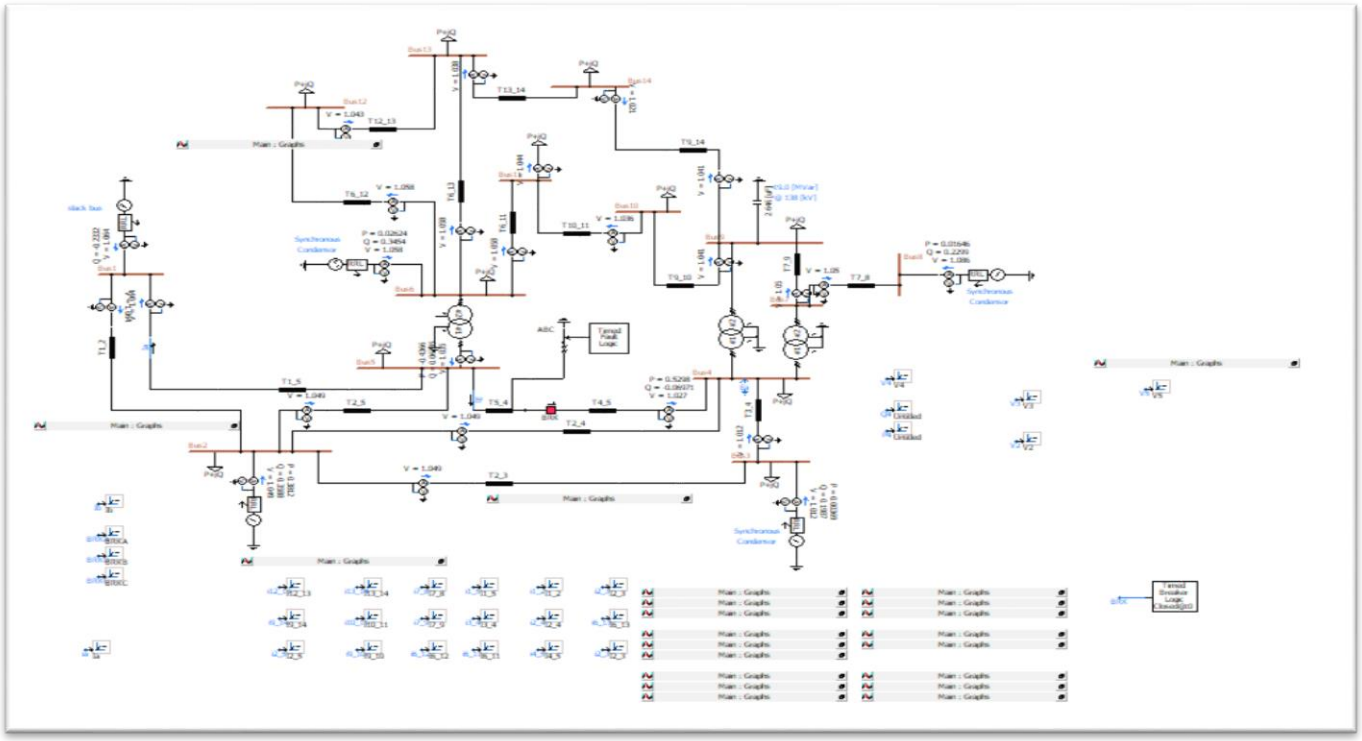


Fig 2. *Circuit Diagram (with fault)*

OBSERVATION

Parameters used:

Base MVA Taken: 100 MVA
Base Current: 1 A
Base Voltage (Bus, Three Phase): 138 kV
Base Voltage (Load): 76.66 kV
Run Time: 1 s
Step Time: 5 µs
Channel Plot Step: 50 µs
Circuit Breaker Resistance: 1e6 Ω

- *Bus voltages values tables are represented in below table:*

1. Under normal operating conditions, we have observed the voltages and currents at all the buses and transmission lines. The results are tabulated below

2. During the 3 phase LLL symmetrical fault between Bus 5 and Bus 4, we have observed the voltages at all the buses. The results are tabulated below.

Table 1: *Voltage values at various buses before the fault (till 0.2 sec)*

Bus Number	RMS Voltage (in KV)
1	140.898
2	138.828
3	134.0808
4	140.07
5	135.1434
6	142.002
7	140.346
8	144.762
9	139.104
10	138.552
11	139.656
12	139.794
13	138.966
14	136.4268

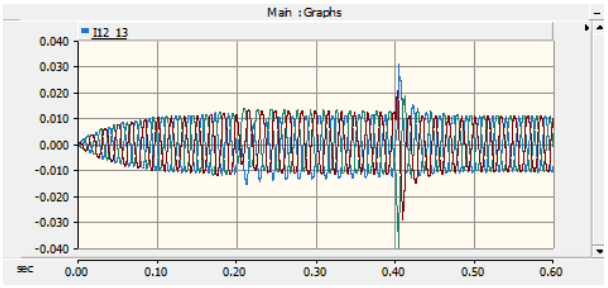
Table 2: *Voltage values at various buses during the fault (till 0.4 sec)*

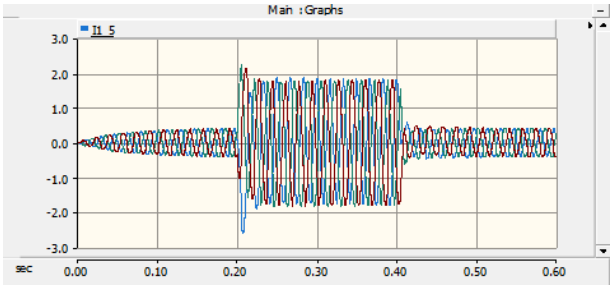
Bus Number	RMS Voltage (in KV)
1	125.6214
2	123.6618
3	133.9014
4	127.9398
5	29.0352
6	127.7742
7	136.1508
8	147.936
9	131.8728
10	129.9408
11	128.271
12	125.8974
13	125.4834
14	126.2286

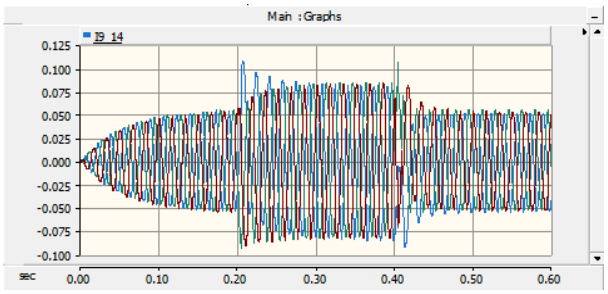
Table 3: *Voltage values at various buses after the fault (till 0.65 sec)*

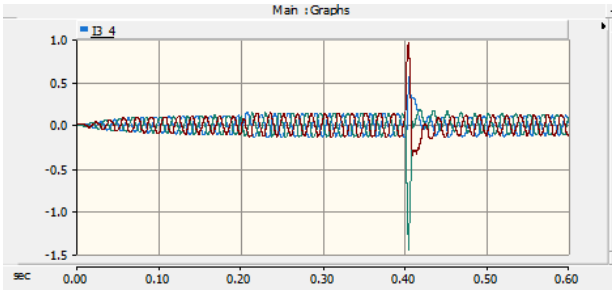
Bus Number	RMS Voltage (in KV)
1	146.28
2	144.072
3	139.242
4	139.932
5	140.346
6	147.384
7	145.866
8	150.144
9	145.038
10	144.348
11	145.452
12	145.314
13	144.624
14	142.278

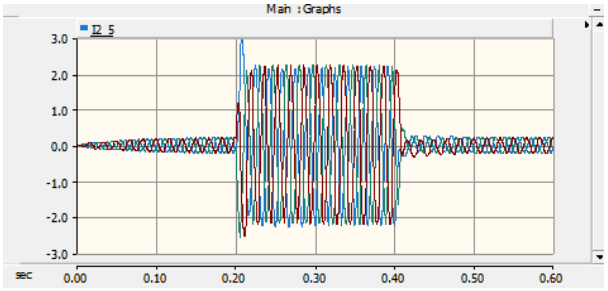
➢ *Transmission Line Current Values at various states in the system*

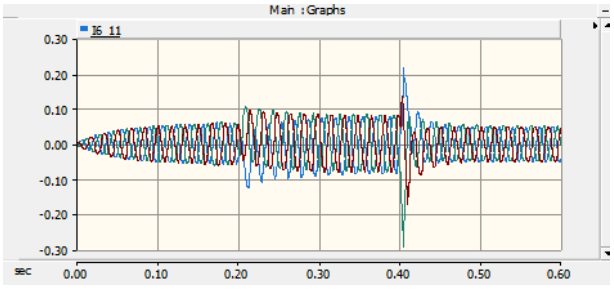


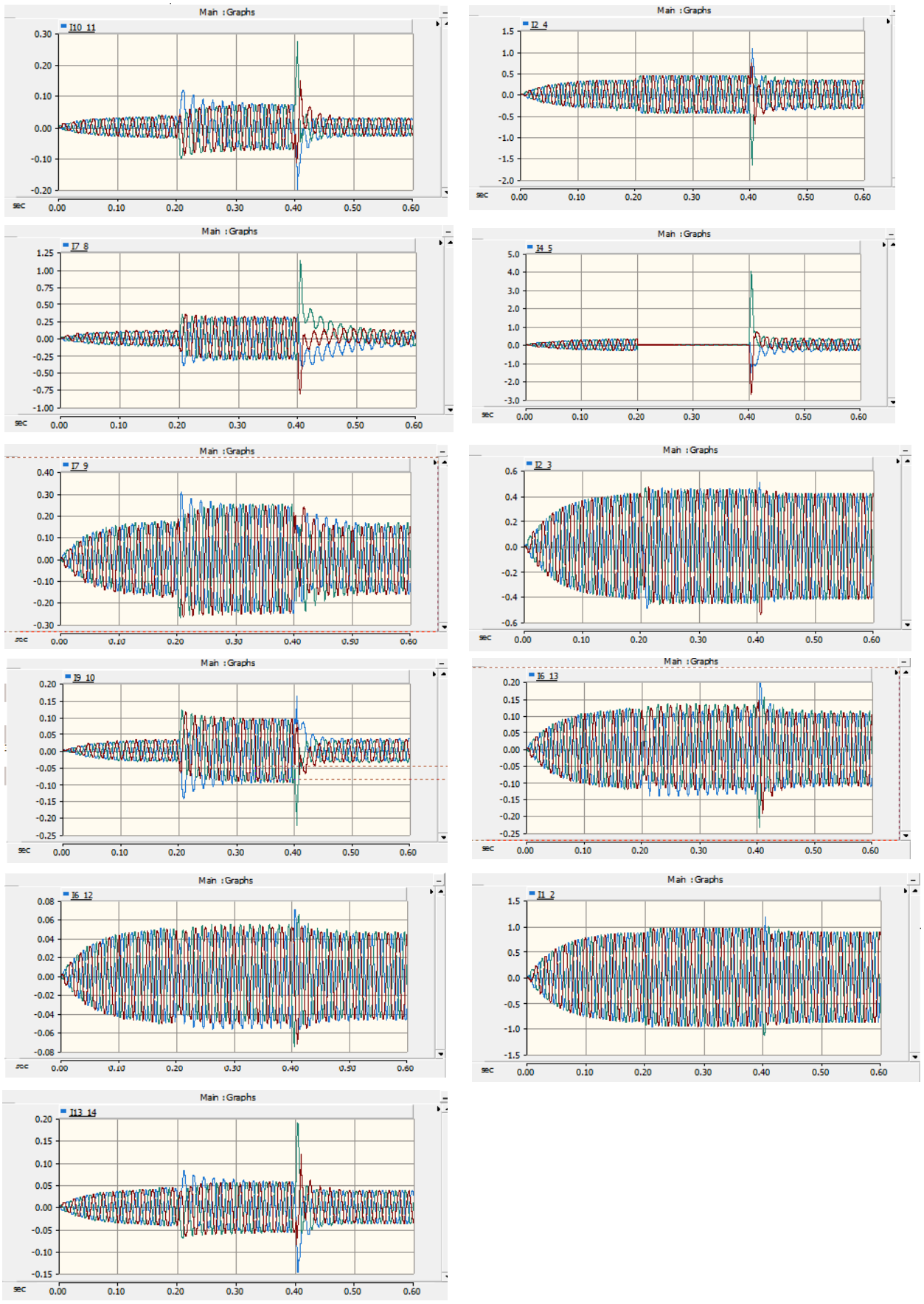












Showing Transmission Lines Current before the insertion of fault (0 - 0.2 sec) and during the fault (0.2 - 0.4 sec) and after clearing the fault (0.4-0.65 sec)

➢ *Breaker Current Values at pre, post and during fault conditions*

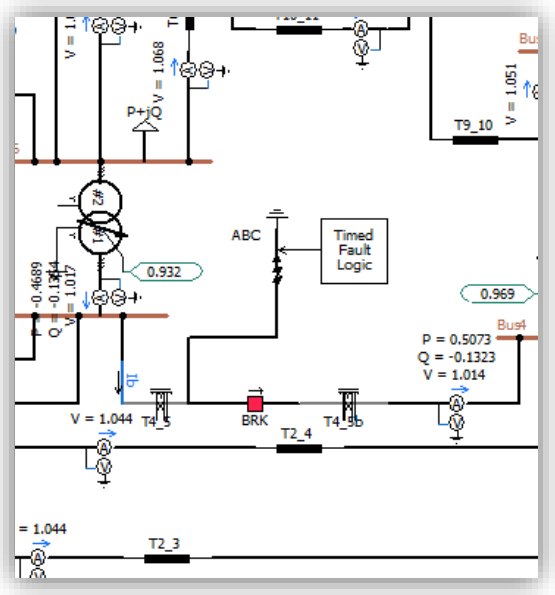


Fig 3. *Diagram Showing Circuit Breaker Current*

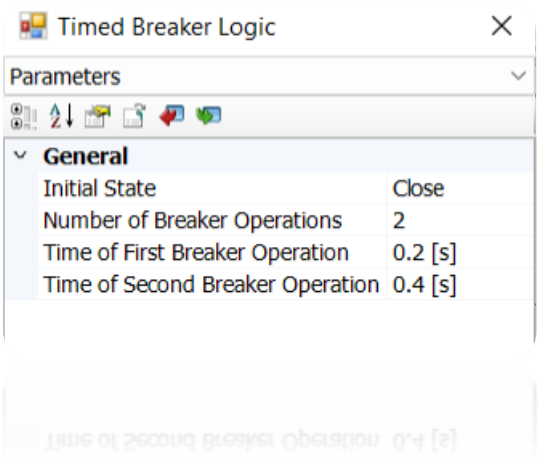


Fig 4. *Diagram Showing Circuit Breaker Logic*

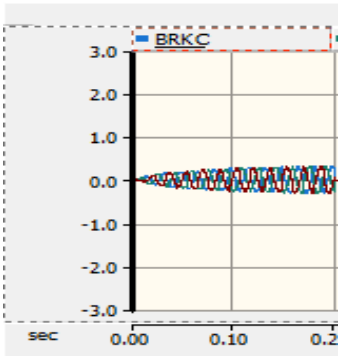


Fig 5. *Showing Breaker Current before fault (0 - 0.2 sec)*

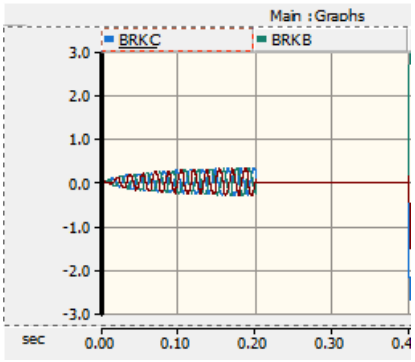


Fig 6. *Showing Breaker Current before fault (0 - 0.2 sec) and during fault (0.2 - 0.4 sec)*

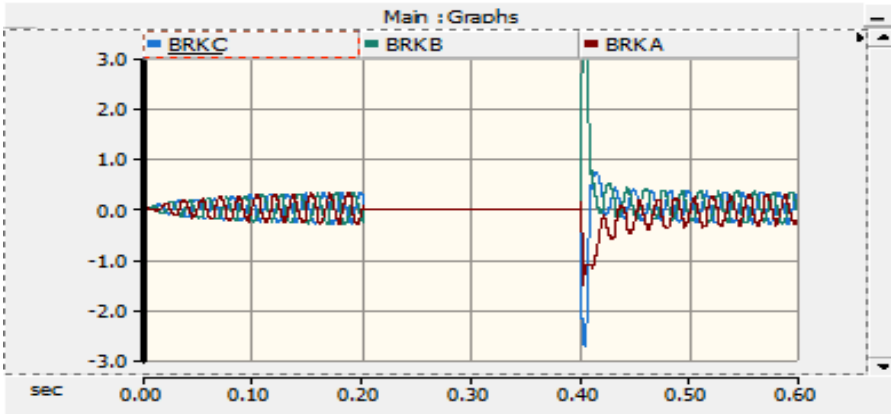


Fig 7. *Showing Breaker Current before fault (0 - 0.2 sec), during the fault (0.2 - 0.4 sec) and after clearing the fault (0.4-0.6 sec)*

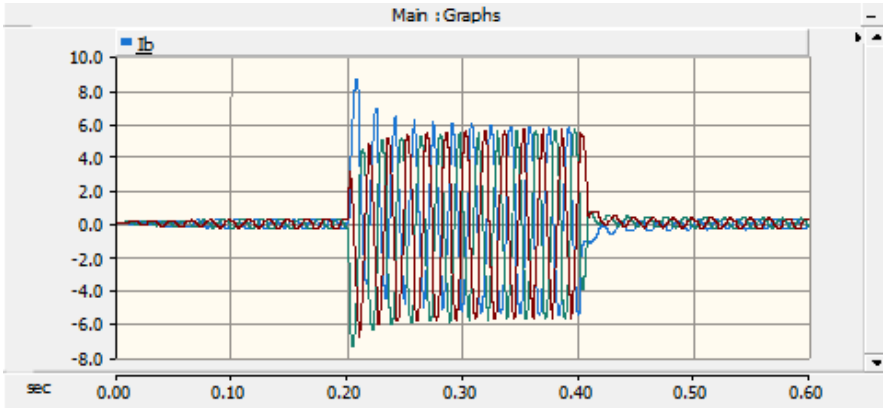


Fig 8. *Showing Line Current before fault (0 - 0.2 sec), during the fault (0.2 - 0.4 sec) and after clearing the fault (0.4-0.6 sec)*

➢ *Active and Reactive Power at Bus 5 at various stages*

State	***Active Power (Base – 100 MVA)***	***Reactive Power (Base - 100 MVA)***
Pre Fault (0.2 Sec)	*0.4818*	*0.1211*
During Fault (0.4 sec)	*0.0001266*	*6.16e-6*
After Clearing the Fault (0.65 sec)	*0.501*	*0.1323*

INFERENCES AND RESULTS

- During the fault, the voltage at Bus 4 and Bus 5 drops sharply and increases after clearing the fault
- A large current flow through transmission line 4 and 5 during the fault. After clearing the fault, a significant drop in current is observed
- The breaker current found is not exactly 0 after clearing the fault (when the breaker is open) because of the finite large value resistance ($10^6\Omega$) given instead of an ideal open circuit
- Active and Reactive Powers at Bus 5 drop significantly in the fault condition

CONCLUSION

In this project, we have created a model of the IEEE 14 Bus system in PSCAD using Tline modeling. We have observed the voltages and currents at all the buses and transmission lines under normal operating conditions and during a 3 phase LLL symmetrical fault between Bus 5 and Bus 4. We have also analyzed the breaker currents, active and reactive power at Bus 5 during all the scenarios. Time logic blocks were used to control the initiation of fault and opening - closing of circuit breakers. The results show that the system is stable under normal operating conditions but experiences voltage drops and current surges during fault conditions. The breaker currents and power analysis at Bus 5 provide valuable information for the protection and control of the power system.