Name:..... Entry No.: .....

INDIAN INSTITUTE OF TECHNOLOGY ROPAR

EE 301 Analog Circuits

Academic Year 2022 - 2023

Course Project

Duration: 28 Days | Max. Marks: 20 | October 14, 2022

Instruction:

1. Discussion among the students is allowed. However, each of the students needs to prepare a report separately.
2. Plagiarism in the report leads to "F" grade.
3. The final Submission deadline is on 10^{th} **November 2022**. Students must submit the report with all the simulation results and executable schematic files.
4. Request of deadline extension and acceptance of delayed submission will not be entertained.
5. It is the student's responsibility to check the files on different PCs before submitting them.
6. The evaluation will be done in 20 Marks (On time submission+report +VIVA=5+5+10).
7. The marks for the report will be awarded after viva and verification of the circuits.

Design of cascode amplifier and cascode current mirror in schematic and layout using LTspice and Magic tools in 180 nm (supply 1.8 V) technology and only schematic of cascode amplifier, beta multiplier and cascode current mirror in 22 nm (supply 0.8 V) technology node to see the effect of lowering the technology node.

1 Introduction

The block diagram for the single-stage cascode amplifier with required biasing network is shown Fig 1. The cascode amplifier requires a biasing circuit which includes the beta multiplier and cascode current mirror circuits. The beta multiplier circuit provides the input to the cascode current mirror and cascode amplifier. One capacitor as a load is added at the output of the cascode amplifier. The characteristics due to the cascoding of amplifiers are: the impedances at input and output are high. The signals amplification undergoes under high bandwidths possessed by the system. The isolation amid input and the output is high. A brief description of every block is given below:

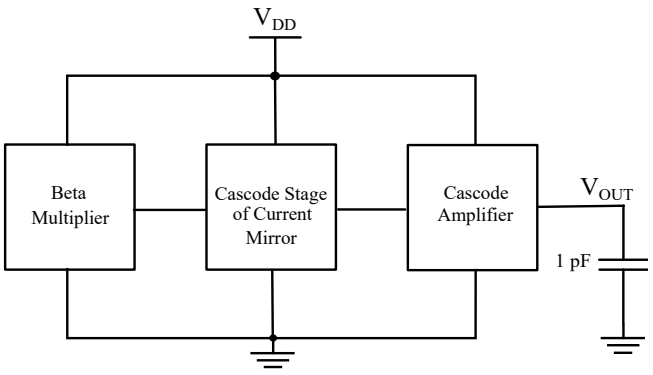

Figure 1: Block diagram of cascode amplifier with other blocks

1.1 Design of beta multiplier circuit

The beta multiplier circuit is an example of positive feedback shown in Fig 2. The beta multiplier circuit is an example of positive feedback. The resistor is added to stabilize the close loop gain of the circuit by requiring higher V_{GS}. The beta multiplier current reference circuit is an alternative method for (potentially) getting a PTAT-like current without utilizing bipolar transistors.

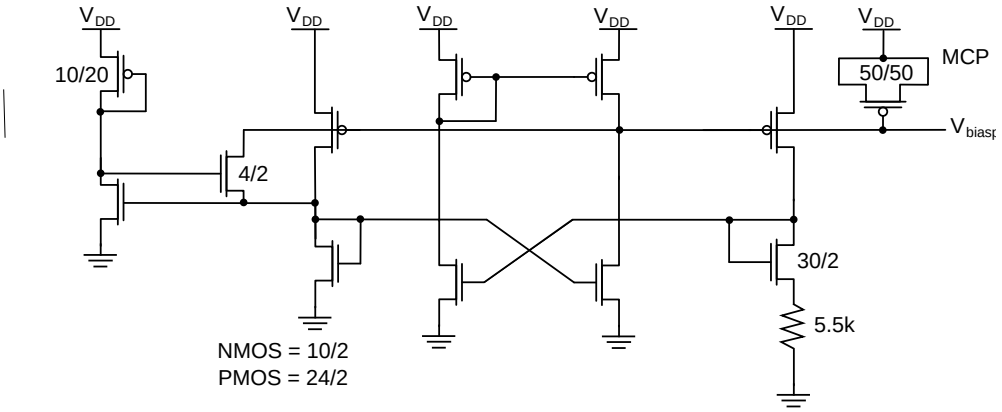

Figure 2: Circuit for beta multiplier circuit

1.2 Design of cascode stage of current mirror

The cascode current mirror with reference biasing circuit is shown in Fig 3. The output (V_{biasp}) of the beta multiplier circuit is fed to the input of the current mirror. The outputs of the circuit are V_{bias1}, V_{bias2}, and V_{bias3}, which are used in the cascode amplifier stage for biasing of the circuit.

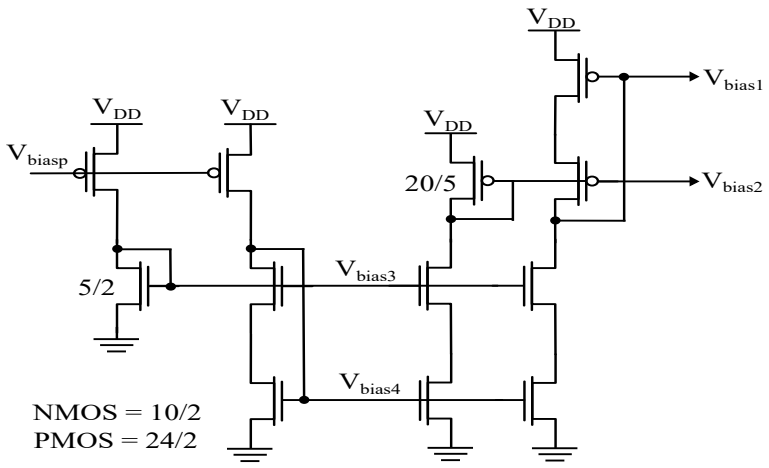

Figure 3: Circuit for cascode current mirror

1.3 Cascode amplifier

A cascode amplifier is also named the "telescopic" cascode. It consists of a common source stage (CS) with a common gate stage (CG), as shown in Fig 4. Compared to a single amplifier stage, this combination may have one or more characteristics: higher input-output isolation, higher input impedance, high output impedance, and higher bandwidth. The stability of the cascode amplifier is another essential aspect that has to be covered. The cascode design is a stable configuration itself. The bottom transistor's source and drain terminals have virtually constant voltage levels, and there is nothing to provide gate feedback. Whereas the higher transistor likewise keeps the source and gate terminal voltages constant. There are only output and input nodes with the appropriate voltage values.

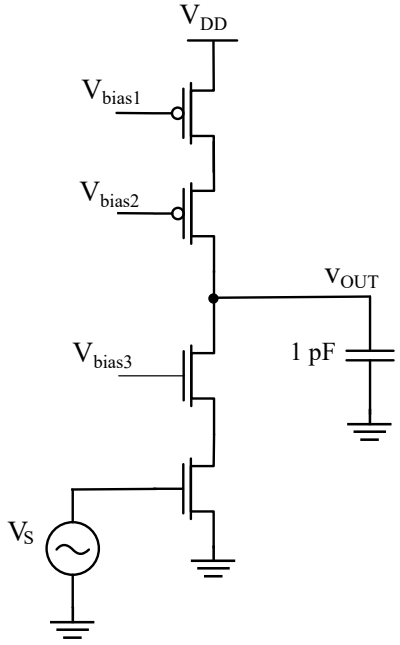

Figure 4: Circuit for cascode amplifier

The target specifications for designing the cascode amplifier are as follows:

- $V_{DD} = 1.8$V
- $A_V = 20$V/V
- Power dissipation (P_D) < 5mW
- Load Capacitance (C_L) $= 1$pF
- Unity Gain Bandwidth(UGB) > 500KHz.

Note: The following steps are needed to be followed:

- Assume suitable data, where ever it is required.
- Do hand calculations for every parameter required for designing the circuit and include in the report.
- Students must submit the report, including the circuits (LTspice and Magic simulation file) and simulation results along with the detailed calculation of every parameter.

References

1. R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation (second ed.)", *Wiley Interscience. Microelectronics Reliability*, 2005.