The two classes defined in the code are Directory class and Core class. Directory class interacts with multiple cores created with the help of core class.

Directory class

dataMemory class has been defined to keep track of directory information and the memory value associated. Directory information comprises 2 bits about the state of the block, 2 bits for owner, and 4 bits for sharer list.
We have then defined a hashmap *dir* whose key value is a string indicating the directory address and value indicating the dataMemory for storing memory blocks indexed by the address of the directory.
The constructor initializes the directory with a maximum size of 64 with a memory value of 0 for each address.
Finally, we have the *directoryLog* for printing the final state of directory entries after processing the entire program.
Directory has access to all the cores.

Core class

Each core class has a cache controller a l1 cache. L1 cache is a 2 way set associative cache with LRU implementation.
Class *Cache_Schema* represents a cache block in the L1 cache of a particular core. It keeps track of memory address, read/write bit, memory value associated, and valid bit.
Core will be initialized with the constructor with the attributes core Id, L1 cache, cache controller and a set of addresses to be used in L1 cache.
Cache_Controller is a nested class that contains the following methods for cache-related instructions:

- instrLS - executes LS instruction - initiates getShared() transaction
- instrLM - executes LM instruction - initiates getModified() and put() transactions
- instrIN - executes IN instruction - initiates put() transaction
- instrADD - executes ADD instruction - initiates getModified() and put() transactions

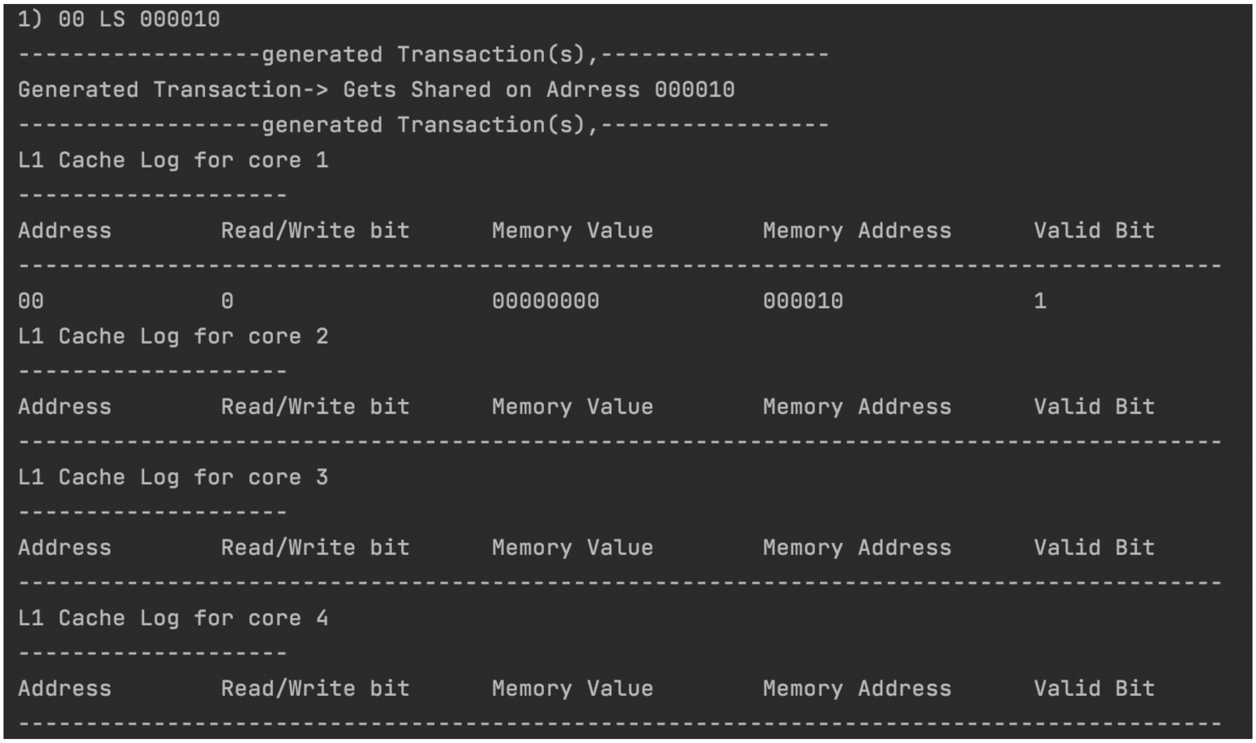
This class handles the cache's working and cache coherence transactions in the quad-core architecture with directory-based coherence protocol. The cache controller interacts with the main memory and updates the cache based on the cache coherence protocol.

Main.py

A new directory and four cores are initialized with an instance of Directory class and Core class respectively.
each instruction is decoded from the instruction.txt and sent to appropriate cores by interconnect(assumed). The cache and directory are updated accordingly.
cacheMemoryDump showcases the status of L1 cache of each core after processing an instruction.
Finally, directoryLog is called for printing the final state of directory entries.

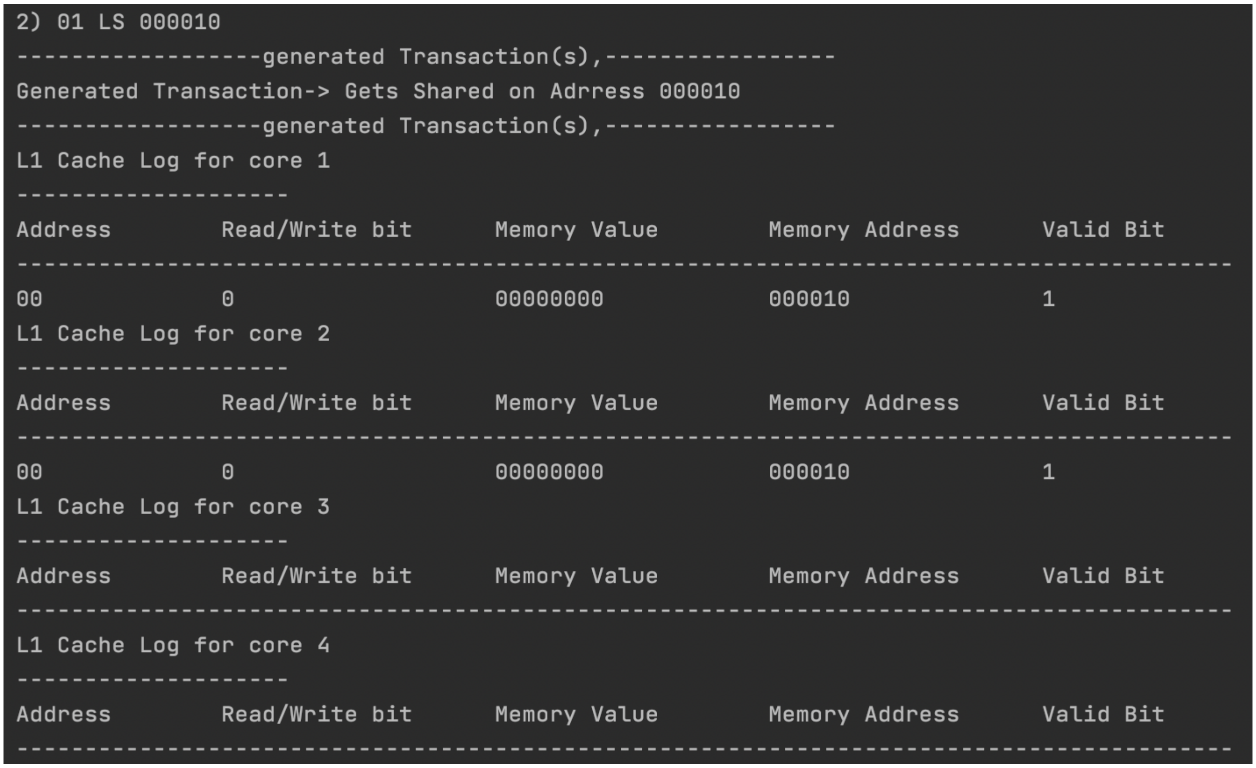
Working and Instruction semantic

- Load Shared Instruction
- 00 LS 000010 -> <2-bit core id><whitespace>LS<whitespace><6-bit memory address>



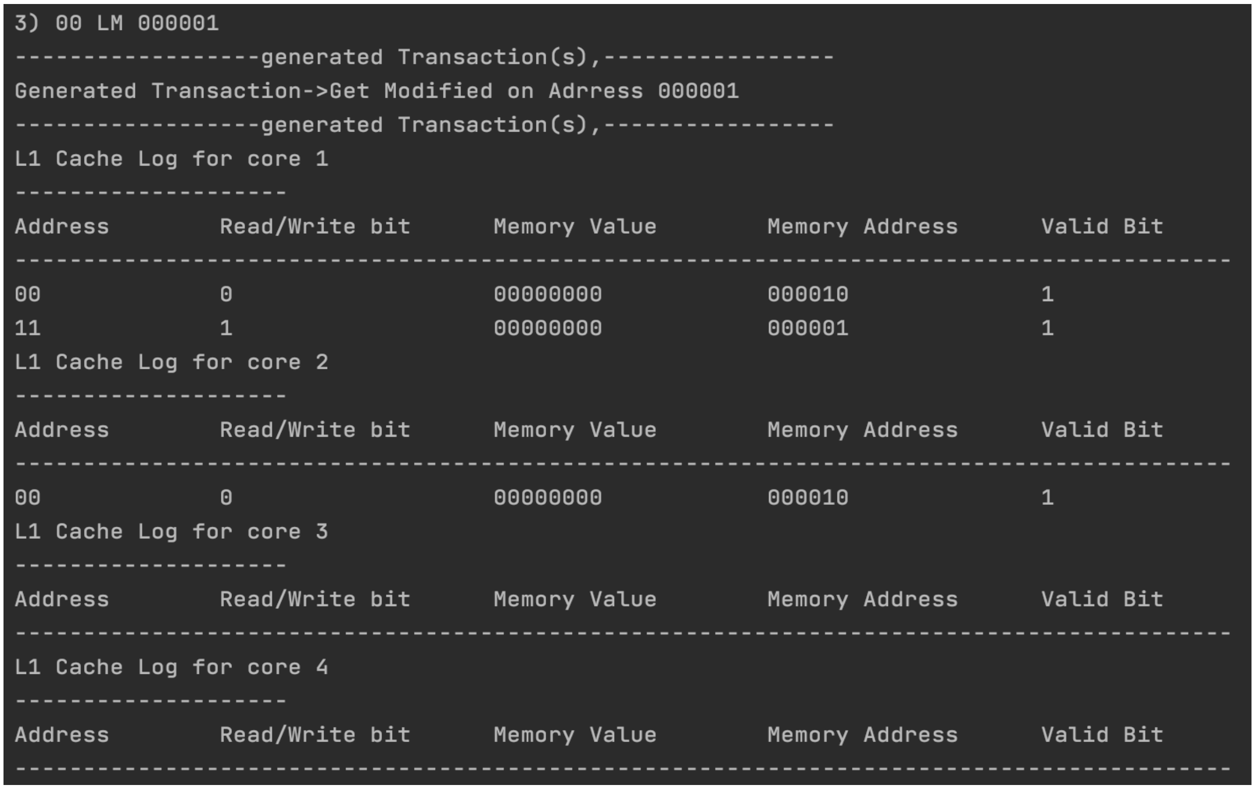
```
1) 00 LS 000010
------------------generated Transaction(s),-----------------
Generated Transaction-> Gets Shared on Adrress 000010
------------------generated Transaction(s),-----------------
L1 Cache Log for core 1
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
-----------------------------------------------------------------------------------------
00             0                   00000000            000010              1
L1 Cache Log for core 2
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
-----------------------------------------------------------------------------------------
L1 Cache Log for core 3
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
-----------------------------------------------------------------------------------------
L1 Cache Log for core 4
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
-----------------------------------------------------------------------------------------
```

- 01 LS 000010



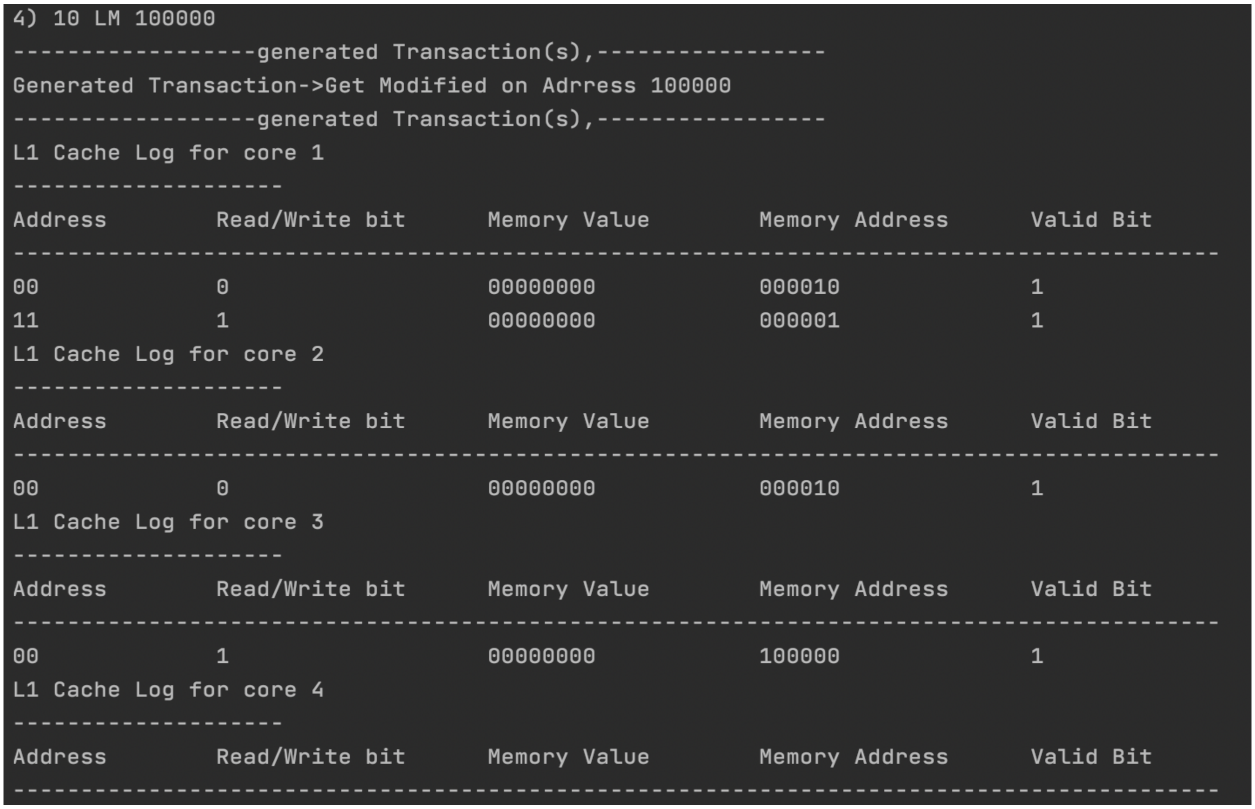
```
2) 01 LS 000010
------------------generated Transaction(s),-----------------
Generated Transaction-> Gets Shared on Adrress 000010
------------------generated Transaction(s),-----------------
L1 Cache Log for core 1
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
-----------------------------------------------------------------------------------------
00             0                   00000000            000010              1
L1 Cache Log for core 2
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
-----------------------------------------------------------------------------------------
00             0                   00000000            000010              1
L1 Cache Log for core 3
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
-----------------------------------------------------------------------------------------
L1 Cache Log for core 4
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
-----------------------------------------------------------------------------------------
```

- Modify Instruction
- 00 LM 000001 -> <2-bit core id><whitespace>LM<whitespace><6-bit memory address>



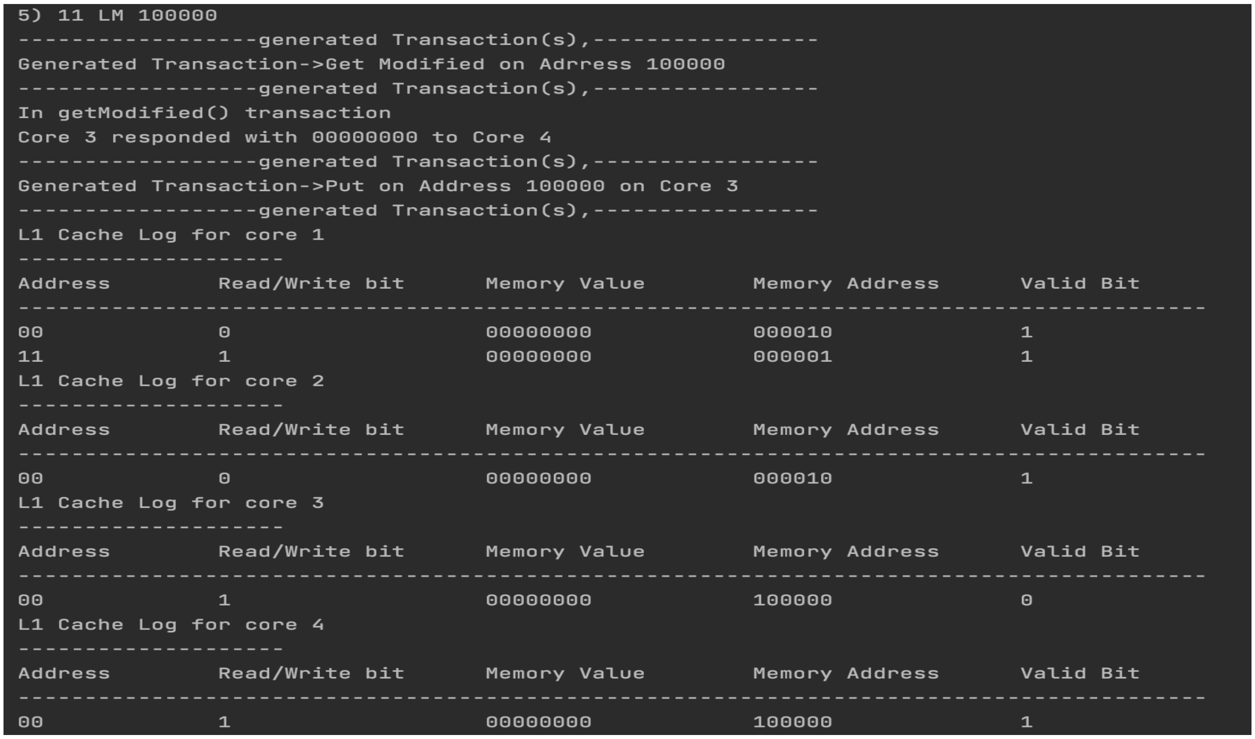
```
3) 00 LM 000001
------------------generated Transaction(s),-----------------
Generated Transaction->Get Modified on Adrress 000001
------------------generated Transaction(s),-----------------
L1 Cache Log for core 1
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
-----------------------------------------------------------------------------------------
00             0                   00000000            000010              1
11             1                   00000000            000001              1
L1 Cache Log for core 2
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
-----------------------------------------------------------------------------------------
00             0                   00000000            000010              1
L1 Cache Log for core 3
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
-----------------------------------------------------------------------------------------
L1 Cache Log for core 4
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
-----------------------------------------------------------------------------------------
```

- 10 LM 100000



```
4) 10 LM 100000
------------------generated Transaction(s),-----------------
Generated Transaction->Get Modified on Adrress 100000
------------------generated Transaction(s),-----------------
L1 Cache Log for core 1
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
-----------------------------------------------------------------------------------------
00             0                   00000000            000010              1
11             1                   00000000            000001              1
L1 Cache Log for core 2
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
-----------------------------------------------------------------------------------------
00             0                   00000000            000010              1
L1 Cache Log for core 3
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
-----------------------------------------------------------------------------------------
00             1                   00000000            100000              1
L1 Cache Log for core 4
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
-----------------------------------------------------------------------------------------
```

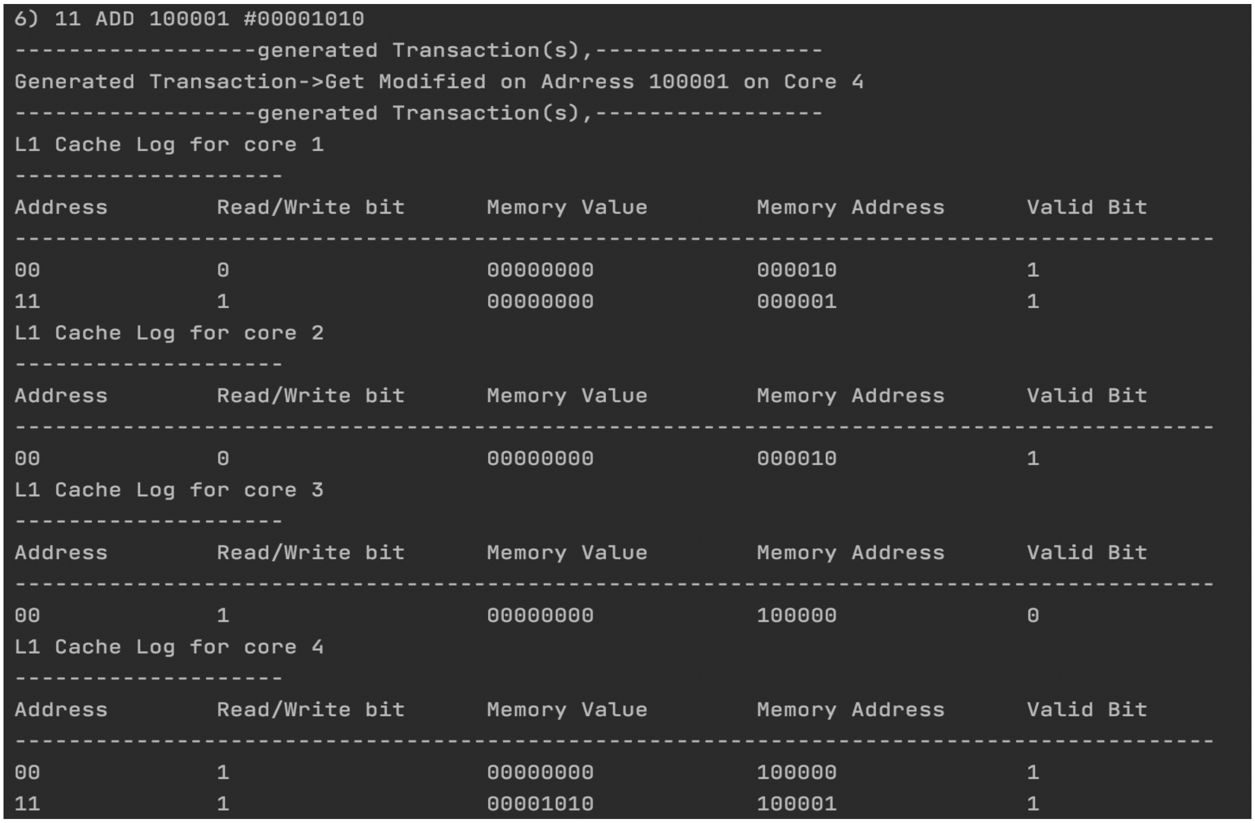
- 11 LM 100000



```
5) 11 LM 100000
------------------generated Transaction(s),-----------------
Generated Transaction->Get Modified on Adrress 100000
------------------generated Transaction(s),-----------------
In getModified() transaction
Core 3 responded with 00000000 to Core 4
------------------generated Transaction(s),-----------------
Generated Transaction->Put on Address 100000 on Core 3
------------------generated Transaction(s),-----------------
L1 Cache Log for core 1
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
-----------------------------------------------------------------------------------------
00             0                   00000000            000010              1
11             1                   00000000            000001              1
L1 Cache Log for core 2
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
-----------------------------------------------------------------------------------------
00             0                   00000000            000010              1
L1 Cache Log for core 3
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
-----------------------------------------------------------------------------------------
00             1                   00000000            100000              0
L1 Cache Log for core 4
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
-----------------------------------------------------------------------------------------
00             1                   00000000            100000              1
```

-

-
- Add Instruction
- 11 ADD 100001 #00001010 - -> <2-bit core id><whitespace>ADD<whitespace><6-bit memory address><whitespace>#<8-bit immediate value>

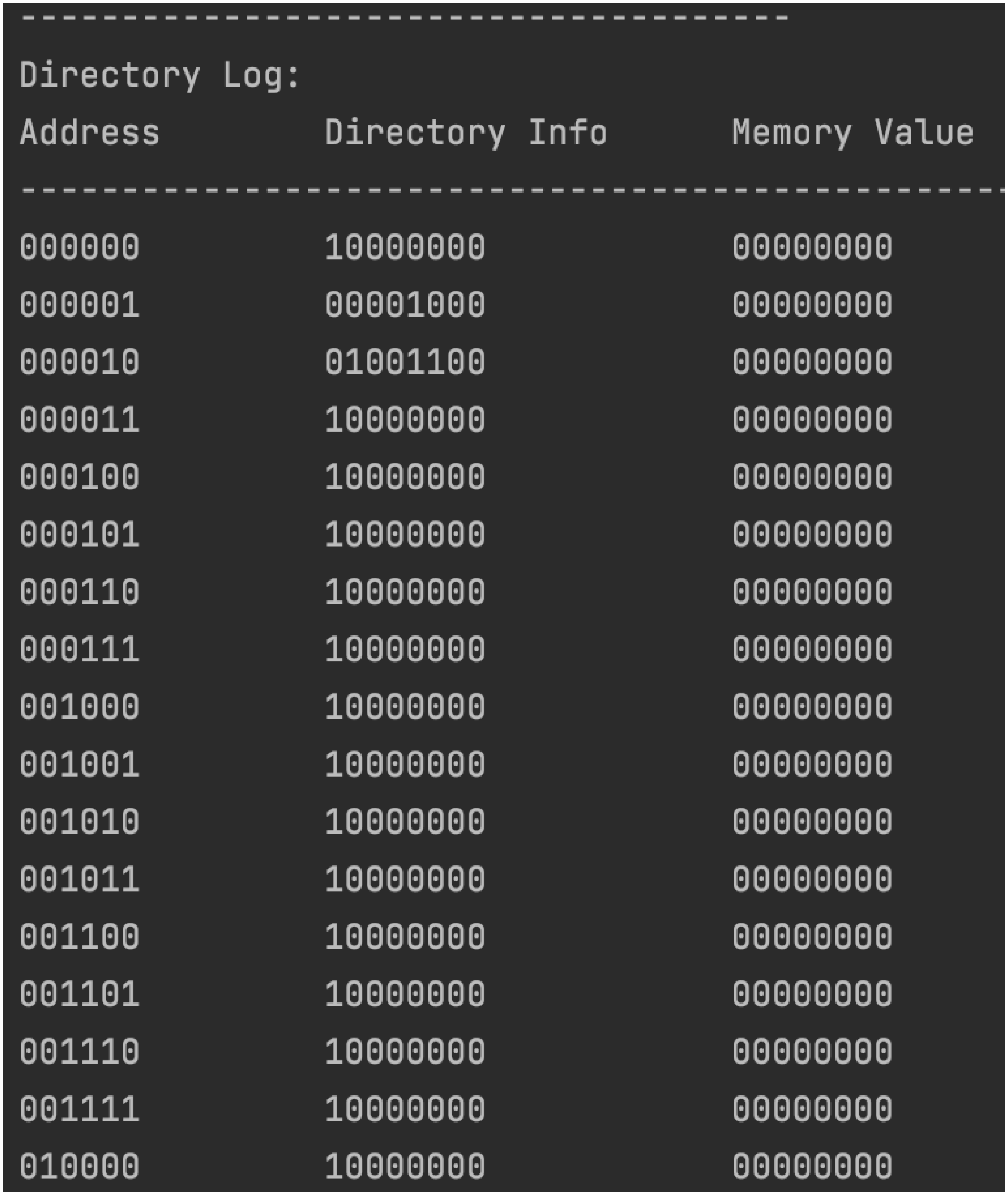


```
6) 11 ADD 100001 #00001010
------------------generated Transaction(s),-----------------
Generated Transaction->Get Modified on Adrress 100001 on Core 4
------------------generated Transaction(s),-----------------
L1 Cache Log for core 1
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
------------------------------------------------------------------------------------------
00             0                   00000000            000010              1
11             1                   00000000            000001              1
L1 Cache Log for core 2
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
------------------------------------------------------------------------------------------
00             0                   00000000            000010              1
L1 Cache Log for core 3
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
------------------------------------------------------------------------------------------
00             1                   00000000            100000              0
L1 Cache Log for core 4
--------------------
Address        Read/Write bit      Memory Value        Memory Address      Valid Bit
------------------------------------------------------------------------------------------
00             1                   00000000            100000              1
11             1                   00001010            100001              1
```

Invalidate Instruction

00 IN 000001 - -> <2-bit core id><whitespace>IN<whitespace><6-bit memory address>

Display of directory entries at the end of execution of program



```
--------------------------------------
Directory Log:
Address        Directory Info      Memory Value
-------------------------------------------------
000000         10000000            00000000
000001         00001000            00000000
000010         01001100            00000000
000011         10000000            00000000
000100         10000000            00000000
000101         10000000            00000000
000110         10000000            00000000
000111         10000000            00000000
001000         10000000            00000000
001001         10000000            00000000
001010         10000000            00000000
001011         10000000            00000000
001100         10000000            00000000
001101         10000000            00000000
001110         10000000            00000000
001111         10000000            00000000
010000         10000000            00000000
```