EC302 – VLSI DESIGN

LAB PROJECT REPORT

TITLE: Design and Analysis of various Oscillators using CMOS transistor

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Candidate's Declaration

We, Sarthak Aggarwal (2K22/EC/206), Sahil Kumar Sakshi (2K22/EC/194) & Satyam Rahi (2K22/EC/208) as 3rd year students in the B.Tech. program for VLSI Design, declare that the project dissertation titled **" Design and Analysis of various Oscillators using CMOS transistor"** submitted to the Department of Electronics and Communication Engineering at Delhi Technological University, Delhi, fulfils partial requirements for the Bachelor of Technology degree. We affirm that this work is original, has not been copied from any source without appropriate citation, and has not been previously used to obtain any degree, diploma, associateship, fellowship, or other similar titles.

Place: New Delhi

Names: Sarthak Aggarwal, Sahil Kumar Sakshi, Satyam Rahi

Roll Nos: 2K22/EC/206, 2K22/EC/194, 2K22/EC/208

Date: 24th April 2025

Certificate

I, **Professor Sumit Kale**, certify that the project dissertation titled **"Design and Analysis of various Oscillators using CMOS transistor"** submitted by **Sahil Kumar Sakshi (2K22/EC/194), Sarthak Aggarwal (2K22/EC/206) and Satyam Rahi (2K22/EC/208)** of the Department of Electronics and Communication Engineering, fulfils partial requirements for the Bachelor of Technology degree at Delhi Technological University, Delhi. This project has been carried out under my supervision and to the best of my knowledge, it has not been submitted either partially or fully for any degree or diploma at this university or elsewhere.

Place: New Delhi

Professor: Sumit Kale

Date: 24th April 2025

Abstract

This project presents the design, simulation, and comparative analysis of five oscillator topologies—3-stage and 5-stage CMOS Ring Oscillators, and Colpitts, Hartley, and Wien Bridge Oscillators—implemented using standard integrated circuit technologies. Oscillators are critical components in VLSI and analog systems for timing and signal generation, each offering distinct advantages in terms of frequency, power, and noise performance.

The 3-stage and 5-stage Ring Oscillators, built from cascaded CMOS inverters, are evaluated for their compactness, ease of integration, and on-chip clocking capabilities. The 3-stage oscillator provides higher frequencies, while the 5-stage offers more phase outputs with better frequency stability. Simulations show Ring Oscillators are ideal for digital integration, though they suffer from higher phase noise and process sensitivity.

In contrast, the Colpitts, Hartley, and Wien Bridge oscillators, based on LC or RC feedback networks, are suited for analog and RF applications. Colpitts and Hartley use LC tanks to deliver stable, low phase-noise signals, while the Wien Bridge oscillator offers low distortion and tuneable frequencies for audio and instrumentation.

A comparison of oscillation frequency, power consumption, phase noise, and complexity reveal that Ring oscillators excel in integration and tunability, while LC-based designs offer better spectral purity, and the Wien bridge oscillator balances simplicity with signal quality. This study provides practical guidance for selecting oscillators in various VLSI and analog system applications.

Acknowledgement

We express our sincere gratitude to the Almighty for His divine blessings and for granting us the opportunity to pursue our academic journey at Delhi Technological University.

We are deeply thankful to our families, particularly our parents, for their unconditional love, constant support, and encouragement throughout the course of this project. Their continued faith in us has been a vital source of strength and motivation.

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1. Introduction

Oscillators are essential components in electronic systems, providing periodic signals required for timing, communication, and signal processing applications. In the field of Very Large-Scale Integration (VLSI), the design and implementation of efficient, reliable oscillators are critical for clock generation, synchronization, and frequency synthesis. Different oscillator topologies offer various trade-offs in terms of integration complexity, frequency range, power consumption, phase noise, and signal purity.

Among the simplest and most widely used oscillators in digital integrated circuits are Ring oscillators, which consist of an odd number of inverter stages connected in a feedback loop. The oscillation frequency of a ring oscillator is primarily determined by the number of stages and the propagation delay of each inverter. The 3-stageRing oscillator is popular for its high oscillation frequency and minimal area, while the 5-stage variant provides additional phase outputs and improved frequency stability at the cost of increased delay and area. Ring oscillators are highly suitable for on-chip clock generation and process monitoring due to their compactness and ease of integration, but they typically suffer from higher phase noise and sensitivity to supply voltage and temperature variations.

In contrast, sinusoidal oscillators such as the Colpitts, Hartley, and Wien bridge oscillators are commonly used in analog and RF circuits, where signal purity and frequency stability are paramount. The Colpitts and Hartley oscillators utilize LC tank circuits to generate stable sinusoidal waveforms with low phase noise, making them ideal for radio frequency applications. The Wien bridge oscillator employs an RC feedback network and is renowned for producing low-distortion sine waves at audio and low-frequency ranges, often used in instrumentation and signal generation.

This project aims to design, simulate, and analyse these five oscillator topologies—3-stage and 5-stageRing oscillators, Colpitts, Hartley, and Wien bridge oscillators—to understand their operating principles, performance characteristics, and practical trade-offs. By comparing their frequency ranges, power consumption, phase noise, and implementation complexity, this study provides valuable insights for selecting appropriate oscillator architectures tailored to specific VLSI and analog system requirements.

2. Theory and Design

2.1 Ring oscillators

2.1.1 Principle of Operation

A Ring oscillator is composed of an odd number of inverter stages connected in a closed loop. The odd number of inversions ensures that the circuit cannot settle at a stable logic state, causing the output to oscillate continuously. Each inverter introduces a propagation delay, and the total delay around the loop determines the oscillation period.

The oscillation frequency $\boldsymbol{f}$ is given by:

$$\boldsymbol{f = \frac{1}{2NT}}$$

where:

- **N** = number of inverter stages (odd number, e.g., 3 or 5)
- $\boldsymbol{T}$ = oscillation period of one inverter stage

2.1.2 Design Considerations

- **Number of Stages:** A 3-stage ring oscillator offers higher frequency due to fewer stages but provides fewer phase outputs. A 5-stage Ring oscillator has lower frequency but better phase resolution and stability.
- **Inverter Sizing:** Transistor sizing affects the delay and power consumption. Larger transistors reduce delay but increase power.
- **Supply Voltage:** The frequency is sensitive to supply voltage variations; thus, stable power supply is crucial.
- **Load Capacitance:** Parasitic and load capacitances increase delay, reducing frequency.

2.1.3 Circuit Implementation

Each inverter stage is implemented using CMOS technology with an NMOS and PMOS transistor. The stages are cascaded, and the output of the last inverter is fed back to the input of the first.

2.2 Colpitts Oscillator

2.2.1 Principle of Operation

The Colpitts oscillator is an LC tank oscillator where the feedback network consists of a capacitive voltage divider. The tank circuit, made of an inductor (L) and capacitors (C1 and C2), determines the oscillation frequency.

The oscillation frequency f_0 is given by:

$$f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

where,

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

2.2.2 Design Considerations

- The capacitive divider provides the necessary feedback for sustained oscillations.
- The quality factor (Q) of the tank circuit affects phase noise and frequency stability.
- The active device (transistor or op-amp) compensates for losses in the tank circuit.

2.2.3 Circuit Implementation

Typically implemented with a bipolar junction transistor (BJT) or MOSFET, the Colpitts oscillator uses an LC tank and capacitive feedback to generate a sinusoidal output.

2.3 Hartley Oscillator

2.3.1 Principle of Operation

The Hartley oscillator is another LC tank oscillator where the feedback is taken from a tapped inductor or two inductors in series. The tank circuit consists of an inductor (split into L1 and L2) and a capacitor (C).

The oscillation frequency f_0 is:

$$f_0 = \frac{1}{2\pi\sqrt{L_{eq}C}}$$

where,

$$L_{eq} = L_1 + L_2$$

2.3.2 Design Considerations

- The inductive divider provides feedback.
- High Q inductors improve frequency stability and reduce phase noise.
- The active device compensates for tank losses.

2.3.3 Circuit Implementation

Implemented using BJTs or MOSFETs, the Hartley oscillator uses the inductive feedback to maintain oscillations with a sinusoidal output.

2.4 Wien Bridge Oscillator

2.4.1 Principle of Operation

It has a selective feedback network consisting of resistors and capacitors arranged in a bridge configuration The Wien bridge oscillator is an RC oscillator that uses a frequency-. It produces low-distortion sine waves at audio and low-frequency ranges.

The oscillation frequency f_0 is:

$$f_0 = \frac{1}{2\pi\sqrt{RC}}$$

where R and C are the resistor and capacitor values in the feedback network.

2.4.2 Design Considerations

- The gain of the amplifier must be precisely controlled to sustain oscillations without distortion.
- Automatic gain control (AGC) circuits are often used to stabilize amplitude.
- The RC network determines frequency accuracy and stability.

2.4.3 Circuit Implementation

Typically implemented with an operational amplifier and RC feedback network. The design emphasizes low distortion and stable amplitude output.

2.5 Comparative Design Summary

Oscillator Type	Frequency Range	Key Components	Advantages	Limitations
3-Stage Ring	High (GHz range)	CMOS Inverters	Compact, easy integration	High phase noise, supply sensitive
5-Stage Ring	Moderate (Lower GHz)	CMOS Inverters	Better phase stability	Larger area, lower frequency
Colpitts	RF (GHz to MHz)	LC Tank, Capacitors	Low phase noise, stable frequency	Requires inductors, larger area
Hartley	RF (GHz to MHz)	LC Tank, Inductors	Tuneable frequency, low noise	Inductor size and losses
Wien Bridge	Audio to low KHz	RC Network, Op-Amp	Low distortion, simple design	Limited high-frequency operation

Table 2.1 Comparison between various Oscillators

3. Methodology and Simulation Results

3.1 3-Stage Ring Oscillator

- Composed of **3 CMOS inverters** in a closed loop.
- Feedback path connects the last inverter's output to the first inverter's input.
- Simplified symbol includes inverter triangles and feedback wiring.

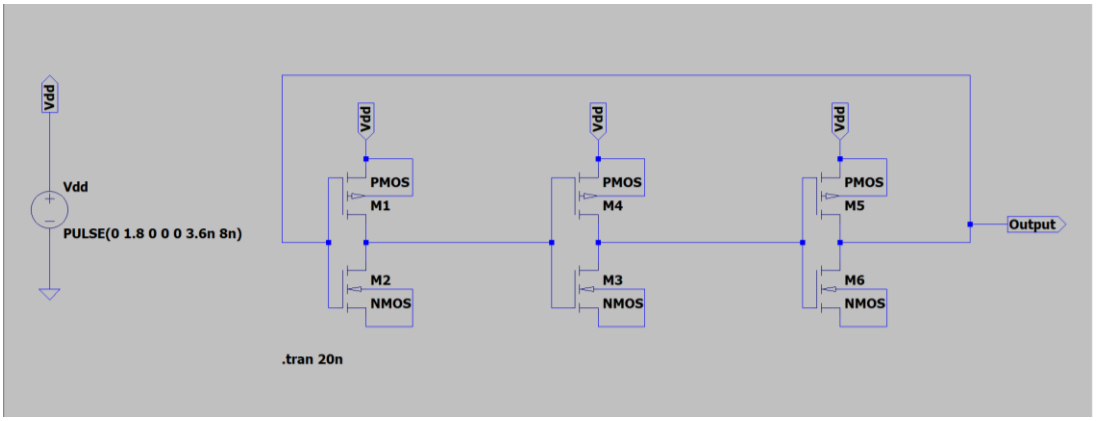

Fig 3.1 Schematic of 3 Stage Ring Oscillator

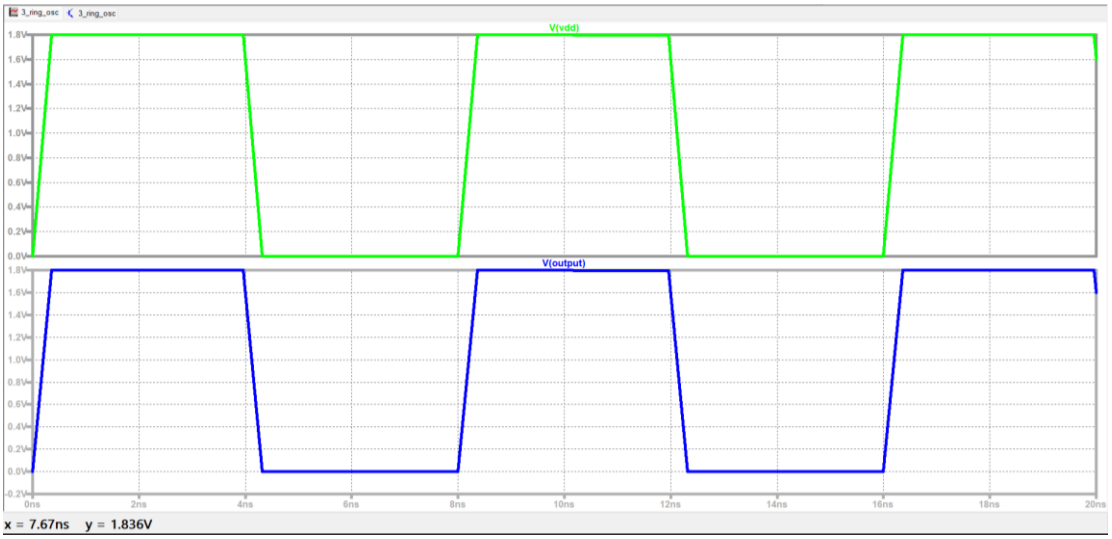

Fig 3.2 Simulation graph of 3 Stage Ring Oscillator

Result: The oscillation period of each inverter is 8 ns (125 GHz) so:

$$f = \frac{1}{2*3*8ns} = 20.833\ GHz$$

3.2 5-Stage Ring Oscillator

- Similar structure like **3-Stage CMOS inverter** but with **5 CMOS inverters**.
- Longer feedback path reduces frequency but improves phase resolution.

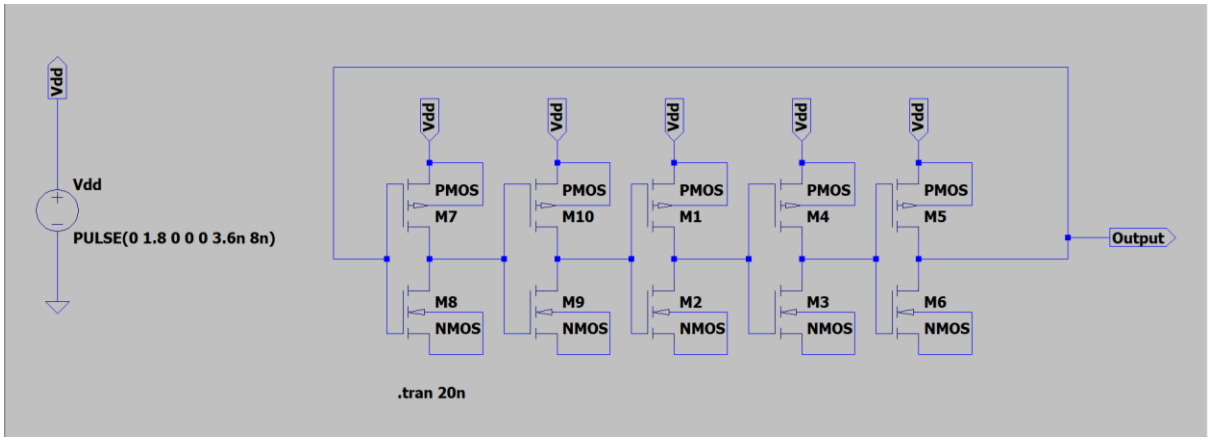

Fig 3.3 Schematic of 5 Stage Ring Oscillator

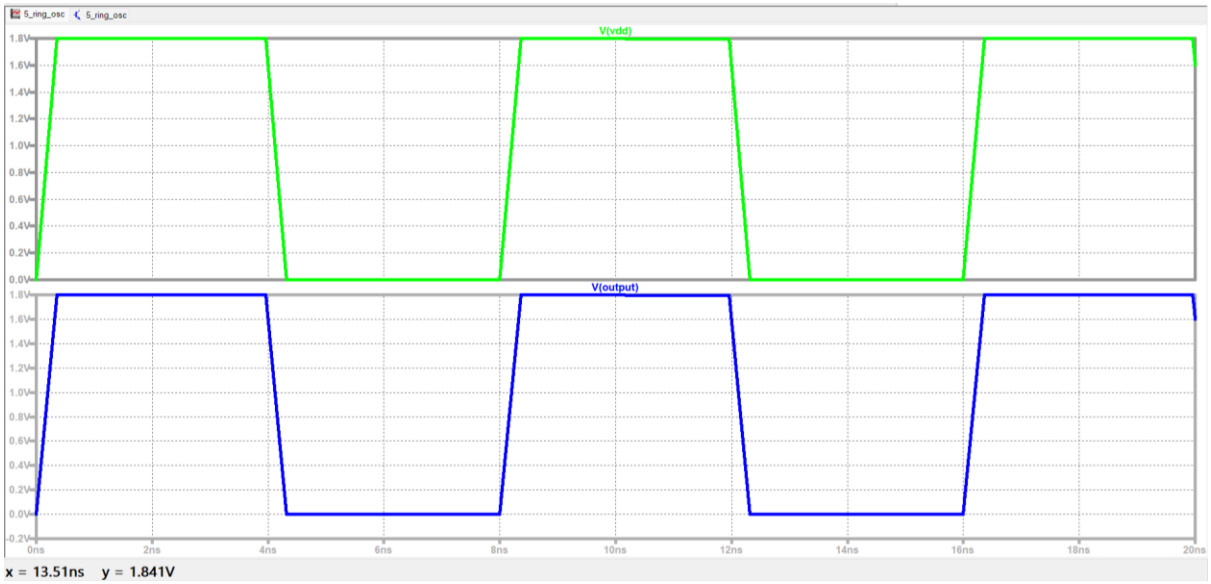

Fig 3.4 Simulation graph of 3 Stage Ring Oscillator

Result: The oscillation period of each inverter is 8 ns (125 GHz) so:

$$f = \frac{1}{2*5*8ns} = 12.5\ GHz$$

3.3 Colpitts Oscillator

- LC tank circuit with capacitive divider (C1, C2) and inductor (L).
- Active device (transistor Q) compensates for losses.
- Output taken from the collector/drain terminal.

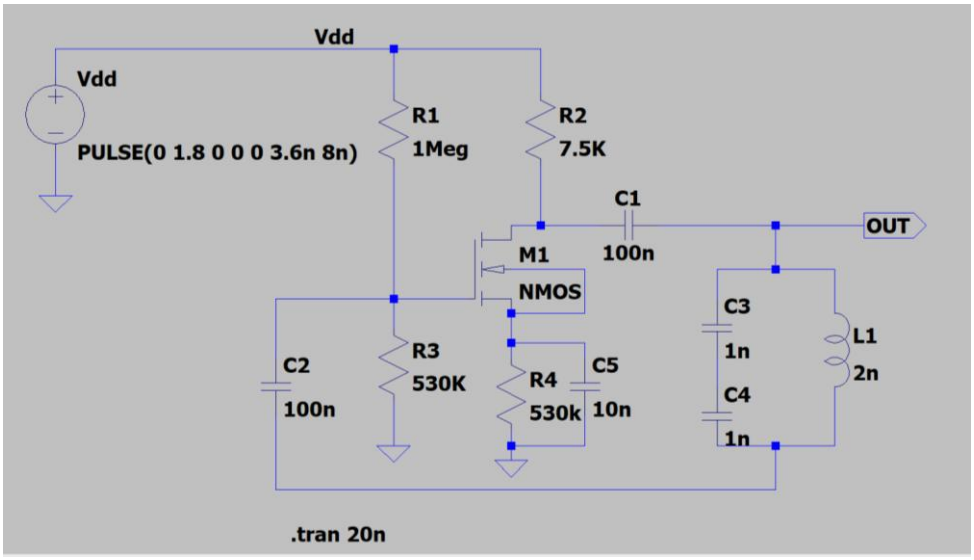

Fig 3.5 Schematic of Colpitts Oscillator

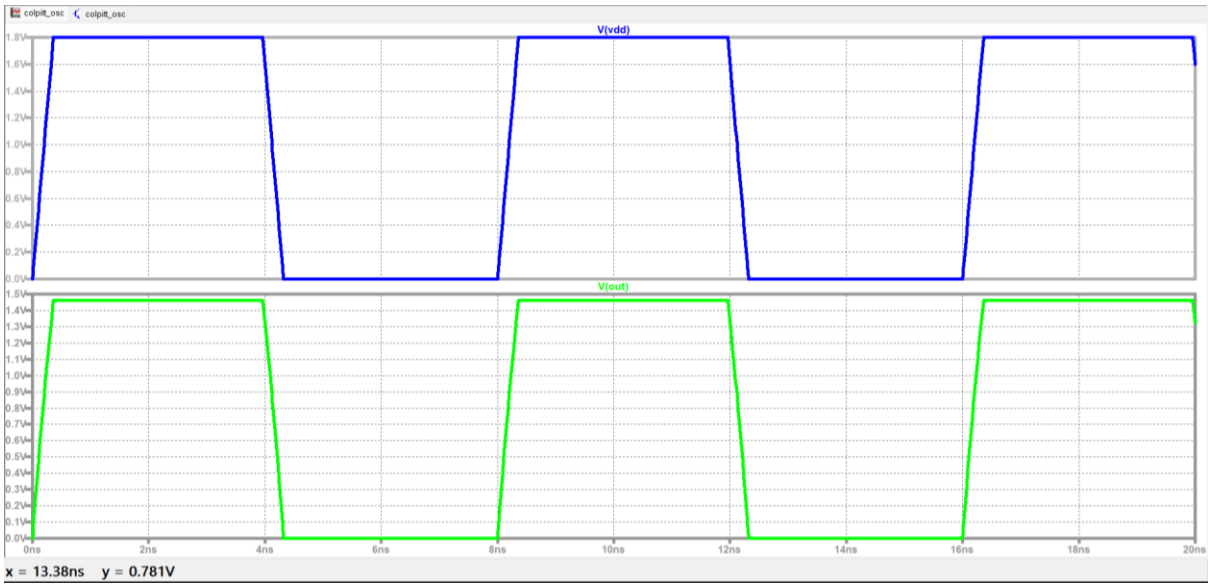

Fig 3.6 Simulation graph of Colpitts Oscillator

Result: If each capacitor is 1nF and inductor is 2nH so:

$$f = \frac{1}{2*\pi*\sqrt{2nH*0.5nF}} = 159.15\ MHz$$

3.4 Hartley Oscillator

- Tapped inductor (L1, L2) with capacitor (C) in the tank circuit.
- Feedback through inductive voltage division.
- Transistor (Q) maintains oscillations.

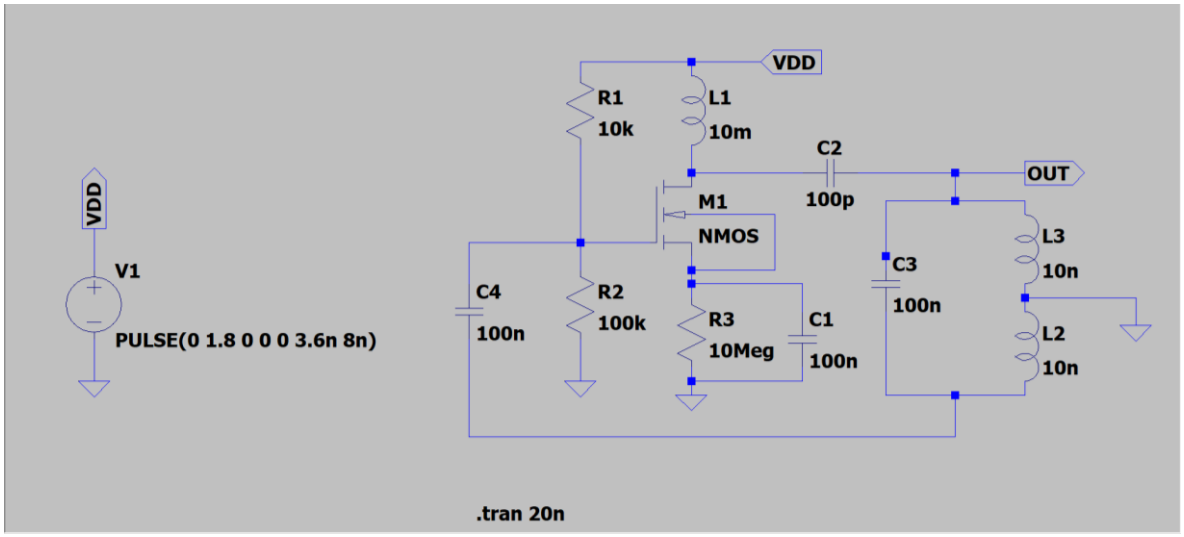

Fig 3.7 Schematic of Hartley Oscillator

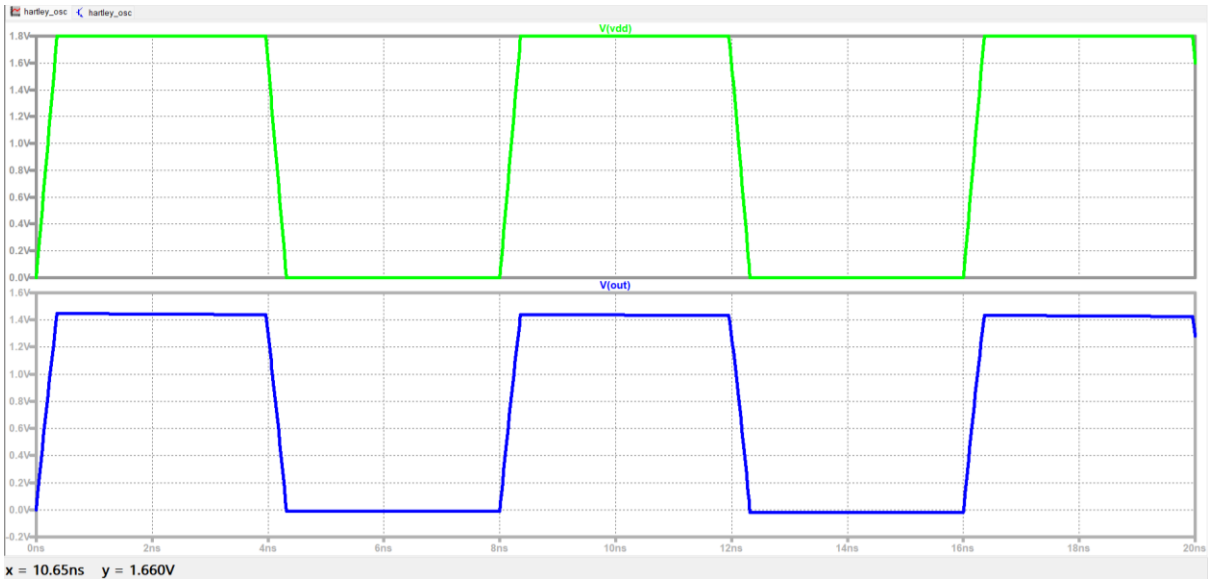

Fig 3.8 Simulation graph of Hartley Oscillator

Result: If each inductor is 10nH and the capacitor is 100nF, so:

$$f = \frac{1}{2 * \pi * \sqrt{20nH * 100nF}} = 11.25\ MHz$$

3.5 Wien Bridge Oscillator

- RC feedback network (R1, R2, C1, C2) with operational amplifier.
- Balanced bridge configuration for low-distortion sine waves.

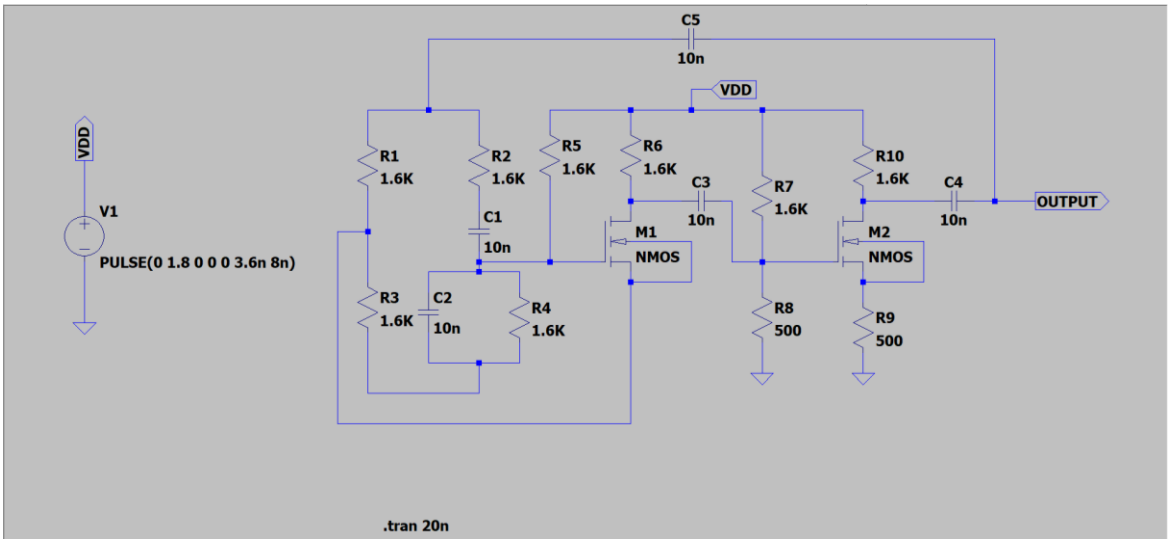

Fig 3.9 Schematic of Wein Bridge Oscillator

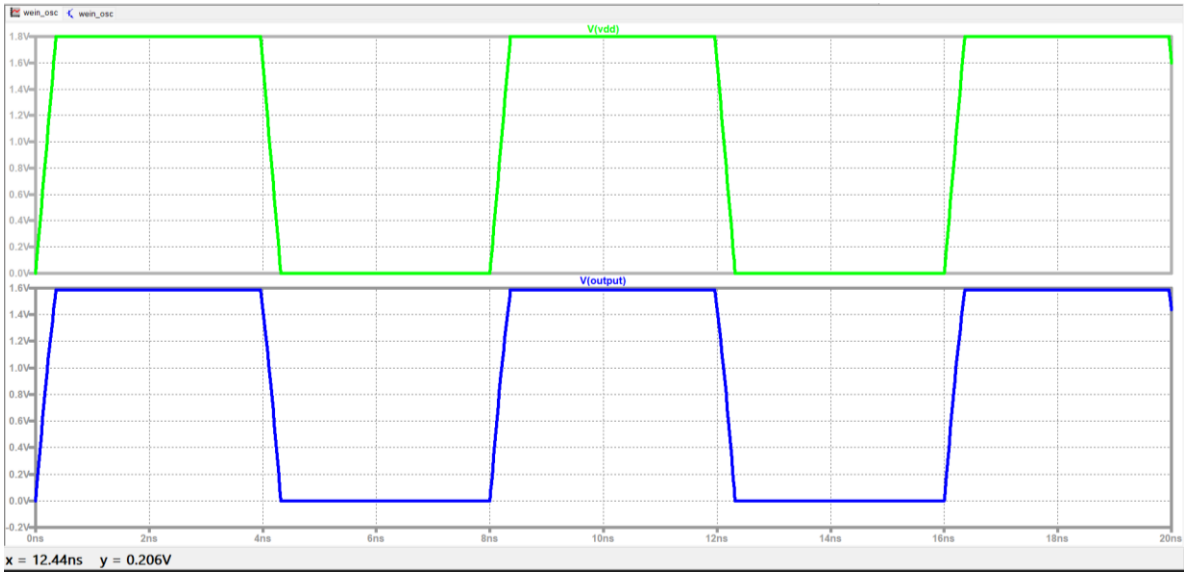

Fig 3.10 Simulation graph of Wein Bridge Oscillator

Result: If each inductor is 10nH and the capacitor is 100nF, so:

$$f = \frac{1}{2 * \pi * 1.6K\Omega * 10nF} = 9.95\ KHz$$

4. Conclusion

In this project, we have designed, simulated, and analysed five prominent oscillator topologies: 3-stage and 5-stage Ring oscillators, Colpitts, Hartley, and Wien Bridge oscillators. Through theoretical study, schematic design, layout, and post-layout verification, we have demonstrated the unique operational principles, advantages, and limitations of each architecture.

The **Ring oscillators**—both 3-stage and 5-stage—exhibit remarkable simplicity, compactness, and ease of integration, making them highly suitable for digital VLSI applications such as on-chip clock generation and process monitoring. However, their frequency stability and phase noise performance are inherently limited by sensitivity to supply voltage, temperature, and process variations.

The **Colpitts** and **Hartley oscillators**, with their LC tank circuits, achieve excellent frequency stability and low phase noise, which are critical for RF and precision analog systems. Their integration in standard CMOS processes is challenged by the need for high-quality inductors, but they remain indispensable in applications demanding spectral purity.

The **Wien bridge oscillator** offers a straightforward approach to generating low-distortion sine waves at audio and low RF frequencies, with the added benefit of easy frequency tuning through RC components.

Post-layout analysis highlighted the significance of parasitic effects and careful layout practices, especially for high-frequency designs. The comparative study underscores that no single oscillator topology is universally optimal; instead, the choice must be guided by application-specific requirements such as frequency range, integration constraints, phase noise, and power consumption.

Overall, this work provides practical guidelines and a foundational understanding for selecting and implementing oscillators in modern VLSI and analog systems. Future enhancements may include adaptive compensation techniques and further optimization for on-chip integration of LC-based designs.

5. References

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These references cover the theory, design, and practical considerations for ring, Colpitts, Hartley, and Wien bridge oscillators, as well as general oscillator design resources.