1. Given the contents of registers:
   R2=0x12345678
   R5=0x3498765B
   R8=0xFFBBCC19
   What is the content of stack pointer after the execution of the following block of code?
   LDR R13, =0x1000002C
   STMDB R13!, {R2, R5, R8}
   LDM R13!, {R3, R6, R7}

   *
   (0.5/0.5 Points)

   - 0x10000038
   - 0x10000020
   - 0x1000002C ✓
   - 0x10000000

2. Assume that the content of R1 is 2 and the content of N flag is 0. After the execution of the instruction RSB R1, #0, the N flag will be set to 1. The statement is *
   (0/0.5 Points)

   - True
   - False ✓

3. Given the contents of registers:
R4=0x12345678
R5=0x3498765B
R6=0xFFBBCC19
What is the content of stack pointer after the execution of the following block of code?
LDR R13, =0x10000020
STM R13!, {R4-R6}

*
(0/0.5 Points)

- 0x10000020
- 0x10000014
- 0x10000032
- 0x1000002C ✓

4. Which of the following statements will send logic ZERO to P0.7 and P0.6 without affecting the values on the remaining pins of the Port-0? *
(0/0.5 Points)

- LPC_GPIO0->FIOCLR0 = 0x3F
- LPC_GPIO0->FIOPIN = 0xFFFFFF3F
- LPC_GPIO0->FIOPIN = 0x000000C0
- LPC_GPIO0->FIOCLR0 = 0xC0 ✓

5. Assume that content of R1 register is 6. What is the content of R1 after the execution of:
MLA R1, R1, R1, R1
LSR R1, #2 *
(0.5/0.5 Points)

- 0x15
- 0x05
- 0x0A ✓
- 0x21

6. Given the contents of registers:
R4=0x12345678
R5=0x3498765B
R6=0xFFBBCC19
What is the content of stack pointer after the execution of the following block of code?
LDR R13, =0x10000010
STMDB R13, {R4-R6}
*
(0/0.5 Points)

- 0x10000004
- 0x10000010 ✓
- 0x1000001C
- 0x10000012

7. Which of the following flag is not tested by BGT instruction? *
(0.5/0.5 Points)

- Sign Flag
- Overflow Flag
- Zero Flag
- Carry Flag ✓

8. Assume that
R1 = 0x10000020, R2 = 0x12345678
Value at the address 0x1000001C is 0x3976ABCD`
Value at the address 0x10000020 is 0xF45EC98A
What is the content of the register R2 after the execution of the following instruction?
LDR R2, [R1], #-4 *
(0.5/0.5 Points)

- 0xF45EC98A ✓
- 0x12345678
- 0x3976ABCD
- 0x1000000C

9. Given the contents of registers:
R2=0x12345678
R5=0x3498765B
R8=0xFFBBCC19
What is the content of R3 after the execution of the following block of code?
LDR R13, =0x1000002C
STMDB R13!, {R2, R5, R8}
LDM R13!, {R3, R6, R7}

*
(0/0.5 Points)

- 0x12345678 ✓
- 0x3498765B
- 0xFFBBCC19
- 0x10000020

10. What are the contents of Z and C flags after the execution of the following statements?
LDR R1, =0xE3D469FF
MSR xPSR, R1
LDR R4,=0x398F4CDE
RSB R1, R4 *
(0/0.5 Points)

- Z = 1, C=1 ✓
- Z=1, C=0
- Z=0, C=0
- Z=0, C=1

11. Complete the following instruction by filling the blank, to configure P2.28 with Function-02.
LPC_PINCON->PINSEL3 = _____; *
(0.5/0.5 Points)

- 2<<8
- 2<<12
- 2<<24 ✓
- 2<<56

12. Assume that
R1 = 0x1000000C
What is the content of the register R1 after the execution of the following block of code?
LDR R4, [R1], #4
LDR R4,[R1, #4]
LDR R3, [R1,#8]! *
(0/0.5 Points)

- 0x10000016
- 0x1000001C
- 0x10000018 ✓
- 0x10000014

13. Assume that content of R13 is 0x10000020 and the content of R14 is 0x10000040. What is the content of Stack Pointer after the execution of the instruction PUSH {R2, R6, R7} ? *
(0.5/0.5 Points)

- 0x10000003
- 0x10000014 ✓
- 0x1000002C
- 0x10000030

14. Assume that
R1=0xFFFFFFFE
R2=0xFFFFFFFF
R3=5
R4=-7
What is the content of R1 after the execution of instruction
SMLAL R1,R2,R3,R4? *
(0/0.5 Points)

- 0xFFFFFFFB
- 0xFFFFFFFF
- 0xFFFFFFDB ✓
- 0xFFFFFFFC

15. Assume that
R1=0x10000030
R2=0x12A96B3C
R3=0xFECD49EA
What is the byte stored in the address 0x1000002E after the execution of the following instructions?
STR R2, [R1, #-4]!
STR R3, [R1], #4
*
(0.5/0.5 Points)

- 0x6B
- 0xCD ✓
- 0xA9
- 0x49

16. Assume that the content of R4 register is 0x12345678. What is its content after rotating it right by 240 bits? *
(0.5/0.5 Points)

- 0x81234567
- 0x12345678
- 0x56781234 ✓

17. Which of the following instructions is invalid in LPC 1768? *
(0/0.5 Points)

- ADCLS R1, R2, #4
- ROL R3, #4 ✓
- RRX R3, R4
- CMN R2, #-4

18. Assume that value at the address 0x10000020 is 0x3456789A, value at 0x10000024 is 0xF34A6987, value at 0x10000028 is 0xFFEEAABB, and value at 0x1000002C is 0xABCDEF01. Given the content of Stack Pointer as 0x10000028: What is the content of register R4 after the execution of the instruction POP {R3, R4, R1, R5} ? *
(0/0.5 Points)

- 0x3456789A
- 0xF34A6987 ✓
- 0xFFEEAABB
- 0xABCDEF01

19. Assume that the following block of code is executed:
LDR R1, = 0x10000000
LDR R2, =0xABCDEF12
LDR R3, =0x39BC139F
STR R2, [R1], #4
STR R3, [R1]
What is the value of a byte stored in the address 0x10000005? *
(0.5/0.5 Points)

- 0xAB
- 0x13 ✓
- 0xBC
- 0x00

20. Given the contents of registers:
R4=0x12345678
R5=0x3498765B
R6=0xFFBBCC19
What is the content of memory location 0x10000027 after the execution of the following block of code?
LDR R13, =0x10000020
STM R13!, {R4-R6}

*
(0/0.5 Points)

- 0x12
- 0x34 ✓
- 0x5B
- 0x19

1. Assume that TCR is loaded with 0x03; PR is loaded with 0x01 ; CTCR is loaded with 0; Which of the following statement is TRUE?
(0/1 Point)

- The TC counts at each positive edge of PCLK
- The TC counts at each positive edge of CAP input
- The TC counts for every 2 positive edges of PCLK
- The TC is cleared and the Timer will not count ✓

2. Given PCLK = 12 MHz and the PR is loaded with 1999. The value to be loaded to MR register to get 500 milliseconds delay ----------
(0/1 Point)

- 1999
- 2999 ✓
- 5999
- 8999

1. The EM2 bit of Timer-1 can be pinned out on ----------
(1/1 Point)

- MAT 1.1
- MAT 1.2 ✓
- MAT 2.1
- MAT 2.2

2. Type- 5 interrupt vector is stored at an offset of ---------- in the Interrupt Vector Table.
(0/1 Point)

- 0x08
- 0x10
- 0x14 ✓
- 0x20

1. How many SFR's are there in Input/output interrupts (Port0, Port2)
(0/1 Point)

- 6
- 10 ✓
- 11
- 12

2. To have a level one external interrupt values to be loaded into the EXTPOLARx and EXTMODEx are
(0/1 Point)

- 0, 0
- 0, 1
- 1, 0 ✓
- 1, 1

1. To have a Falling Edge Interrupt, values to be loaded into the EXTPOLARx and EXTMODEx SFR's are *
(1/1 Point)

- 1, 1
- 0, 1 ✓
- 1, 0
- 0, 0

2. _____ is the interrupt handler for IO Interrupt *
(1/1 Point)

- External Interrupt handler 0
- External Interrupt handler 2
- External Interrupt handler 3 ✓
- External Interrupt handler 1

3. Io Interrupt Supports both +ve and -ve Edge, level Triggering *
(1/1 Point)

- YES
- NO ✓

4. Port 0 and Port 2 pins support External Interrupts *
(1/1 Point)

- YES
- NO ✓

1. What is the input analog voltage required to produce the digital output of 0x064 in LPC 1768?
(1/1 Point)

- 5.152 mV
- 51.52 mV
- 8.05 mV
- 80.5 mV ✓

2. How many analog channels could be simultaneously converted into digital in LPC 1768?
(1/1 Point)

- 4
- 8 ✓
- 12
- 16

1. In software controlled mode of ADC, only one of the SEL bits to be 1 in the ADCR register so that the selected channel gets converted into digital. TRUE/FALSE
(1/1 Point)

- TRUE ✓
- FALSE

2. How many data registers are there in LPC 1768 ADC module?
(0/1 Point)

- 6
- 8
- 9 ✓
- 12

1. Resolution of DAC in LPC1768 *
(1/1 Point)

- 8
- 12
- 14
- 10 ✓

2. DAC Register used to hold the digital value to convert into Analog *
(1/1 Point)

- DACAR
- DACCTRL
- DACCNTVAL
- DACR ✓

1. LPC 1768 PWM module supports up to ---------- double edge PWM lines
(1/1 Point)

- 2
- 3
- 5 ✓
- 6

2. To generate the double edge PWM output waveform on PWM4 line, following Match Registers are to be used.
(1/1 Point)

- MR0, MR4
- MR0, MR3, MR4 ✓
- MR0, MR3
- MR0, MR4, MR5

1. SFR's associated with DAC in LPC1768 *
(1/1 Point)

- [x] DACR ✓
- [x] DACCTRL ✓
- [ ] DACCNTAL
- [ ] All of the Above

2. Name the SFR used to enable double buffering option *
(1/1 Point)

- ( ) DACR
- (•) DACCTRL ✓
- ( ) Both DACR and DACCTRL
- ( ) None of the above

1. Value to be loaded on to LCR to configure UART for 8-bit word length, parity disable, enable divisor latch *
(1/1 Point)

- ( ) 0x00000081
- ( ) 0x00000082
- (•) 0x00000083 ✓
- ( ) 0x00000084

2. Value to be loaded into FCR register to enable both Tx and Rx FIFO buffer *
(1/1 Point)

- ( ) 0x00000008
- (•) 0x00000007 ✓
- ( ) 0x00000006
- ( ) 0x00000004

1. When a PWM Match 0 event occurs, the contents of match register will be transferred to the ----- if the corresponding bit in the ---------- has been ----------.
(1/1 Point)

- latch enable register, shadow register, set
- shandow register, latch enable register , set ✓
- latch enable register, shadow register, reset
- shandow register, latch enable register , reset

2. Given MR0 =200, MR2 =40, MR3 = 130.
The width of the double edge PWM pulse on PWM1.3 is ---------
(1/1 Point)

- 40
- 70
- 90 ✓
- 160