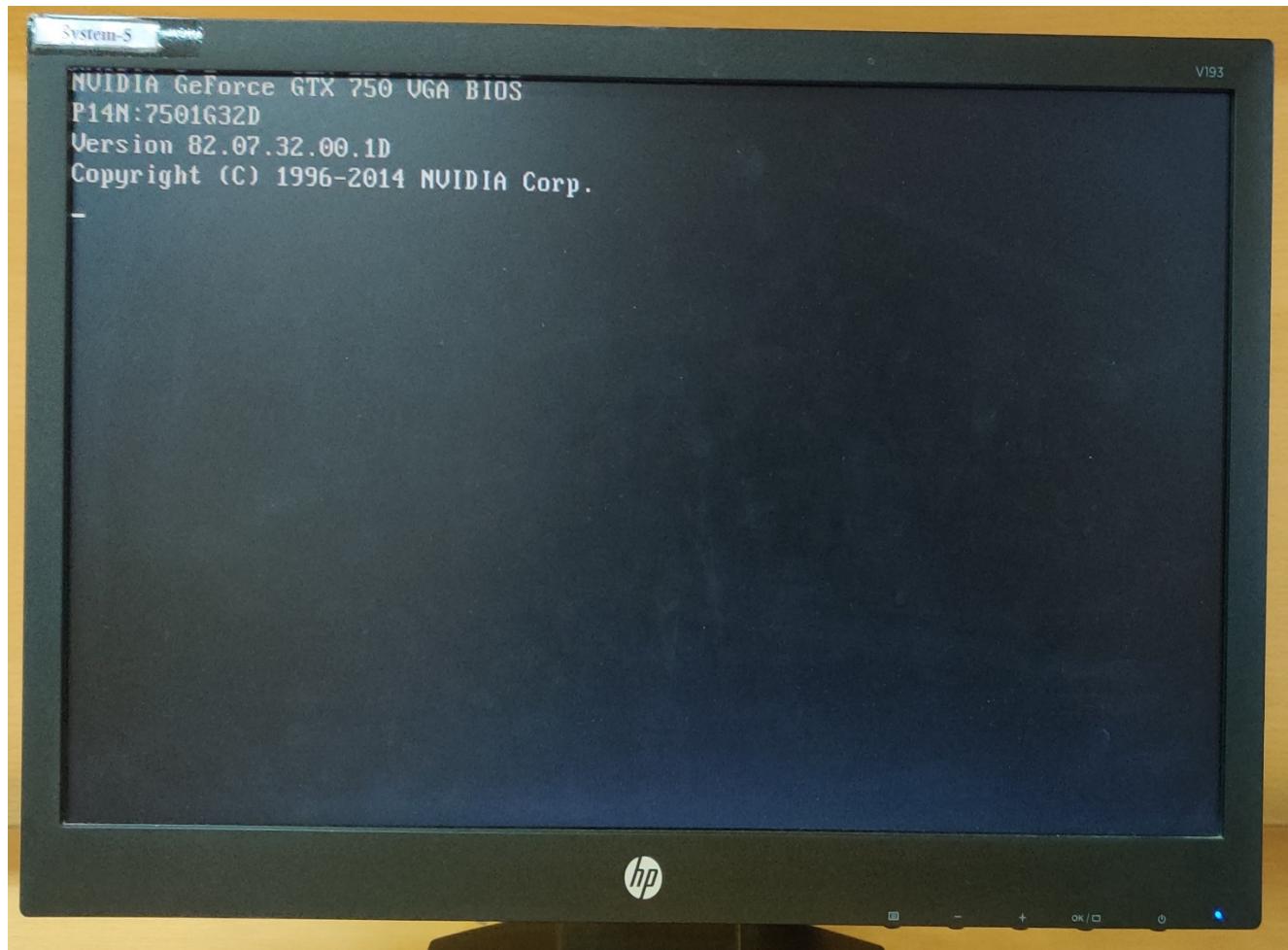


# HOW TO START SYSTEM

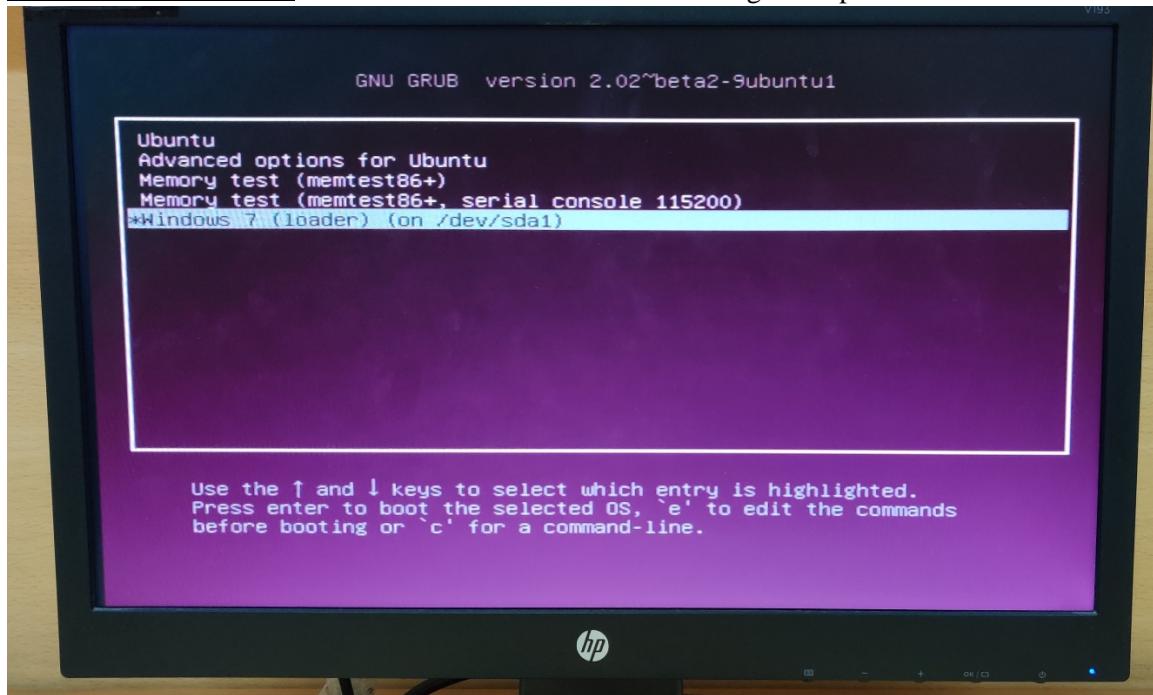
Dear students in the ECAD & DSP lab all desktops have dual operating system (OS) (WINDOS + UBUNTU/RED HAT) therefore I am sharing the some screen shots to let you know how to choose the desired OS.

1. When you will press the power button of the CPU, the given below screen/interface will appear on the Monitor/LCD Screen. **As soon as this screen comes on the screen you need to trigger the down arrow key** ( available on the keyboard in the arrow keys panel)

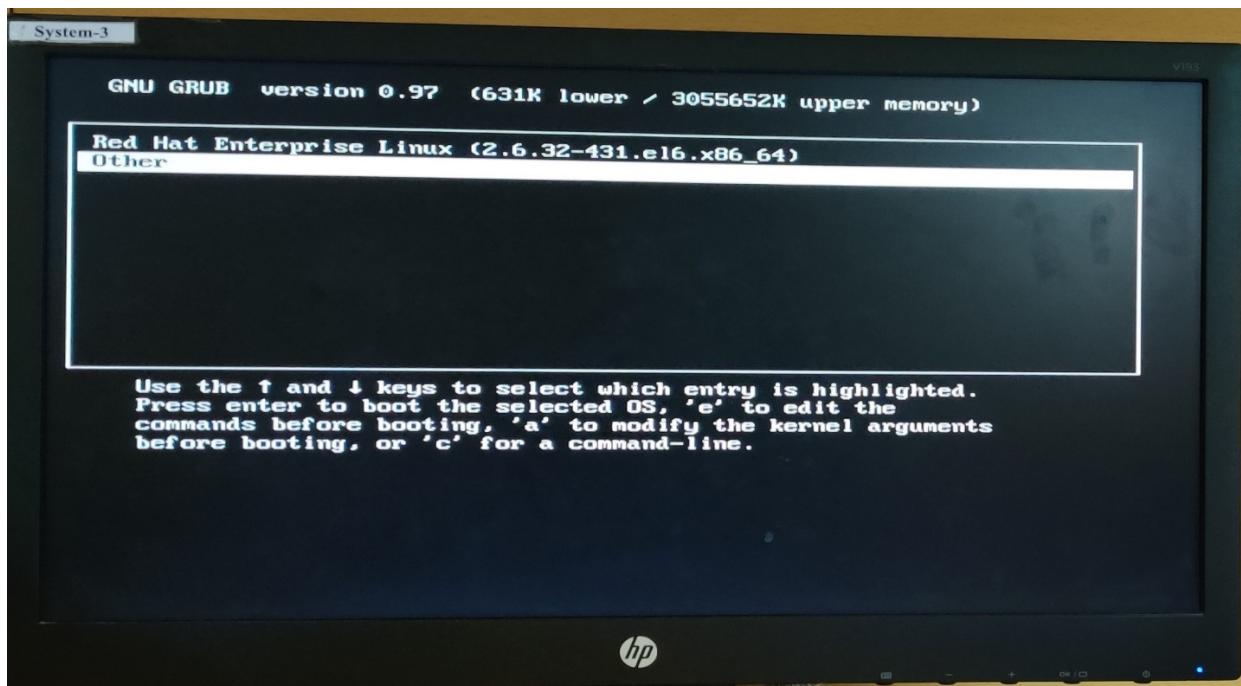


- When you trigger the down arrow key, the given below interface will come on the screen to choose the OS.

Ubuntu based interface: select the windows 7/ windows manager setup from the OS menu.



Red Hat based interface: From this interface you have to choose “Other” to get into the windows OS.



If you fail to choose the desired OS (windows OS) then UBUNTU/RED HAT OS will automatically boot itself. To get again same OS selection menu/ interface you will need to restart your system to select the windows OS.

# A Brief Introduction To Vivado® Design Suite



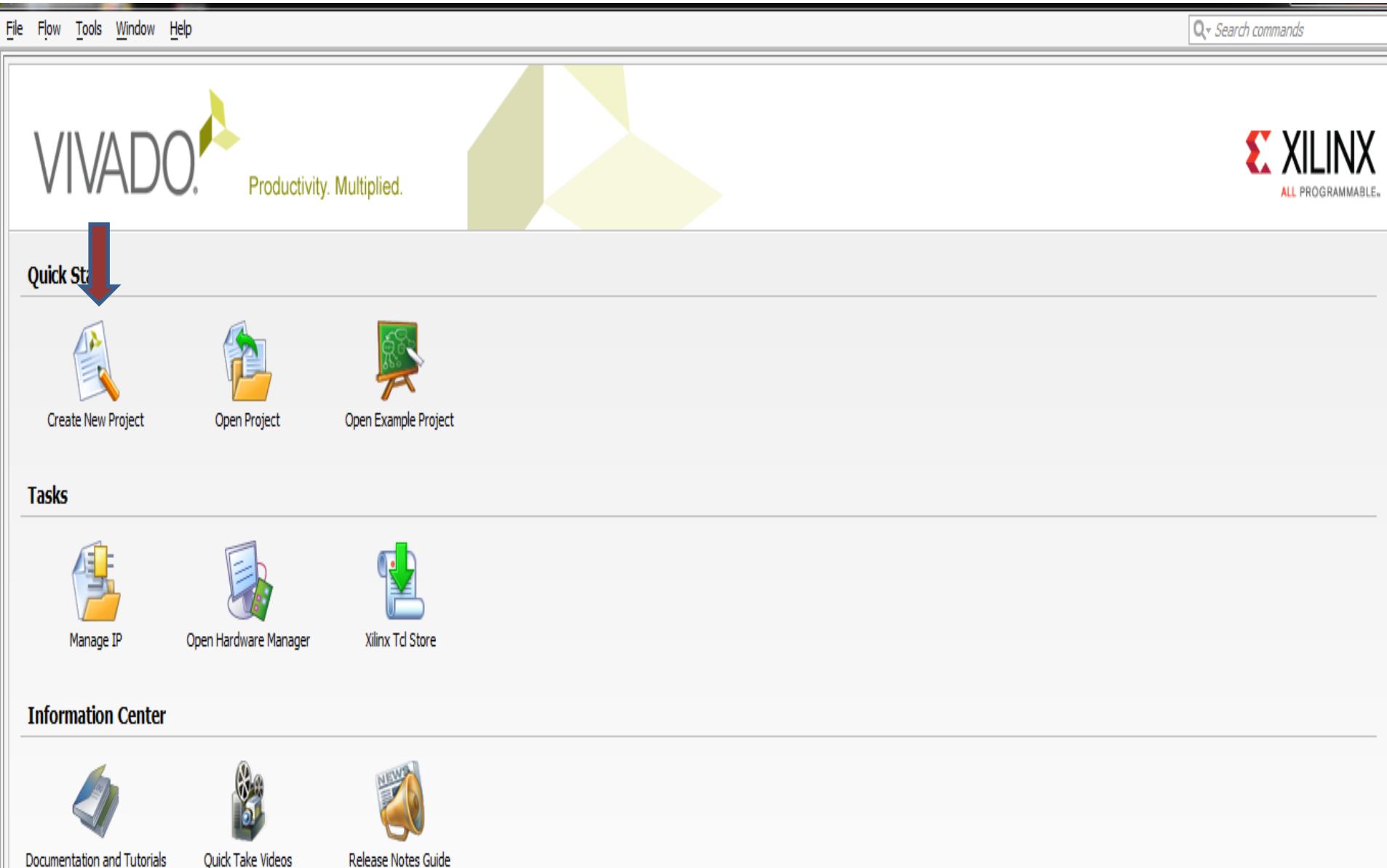
In this ‘Cheat Sheet’ the use of Vivado  
to Simulate , Synthesize and  
implementation ‘Digital Design’  
using VHDL is explained

# Agenda

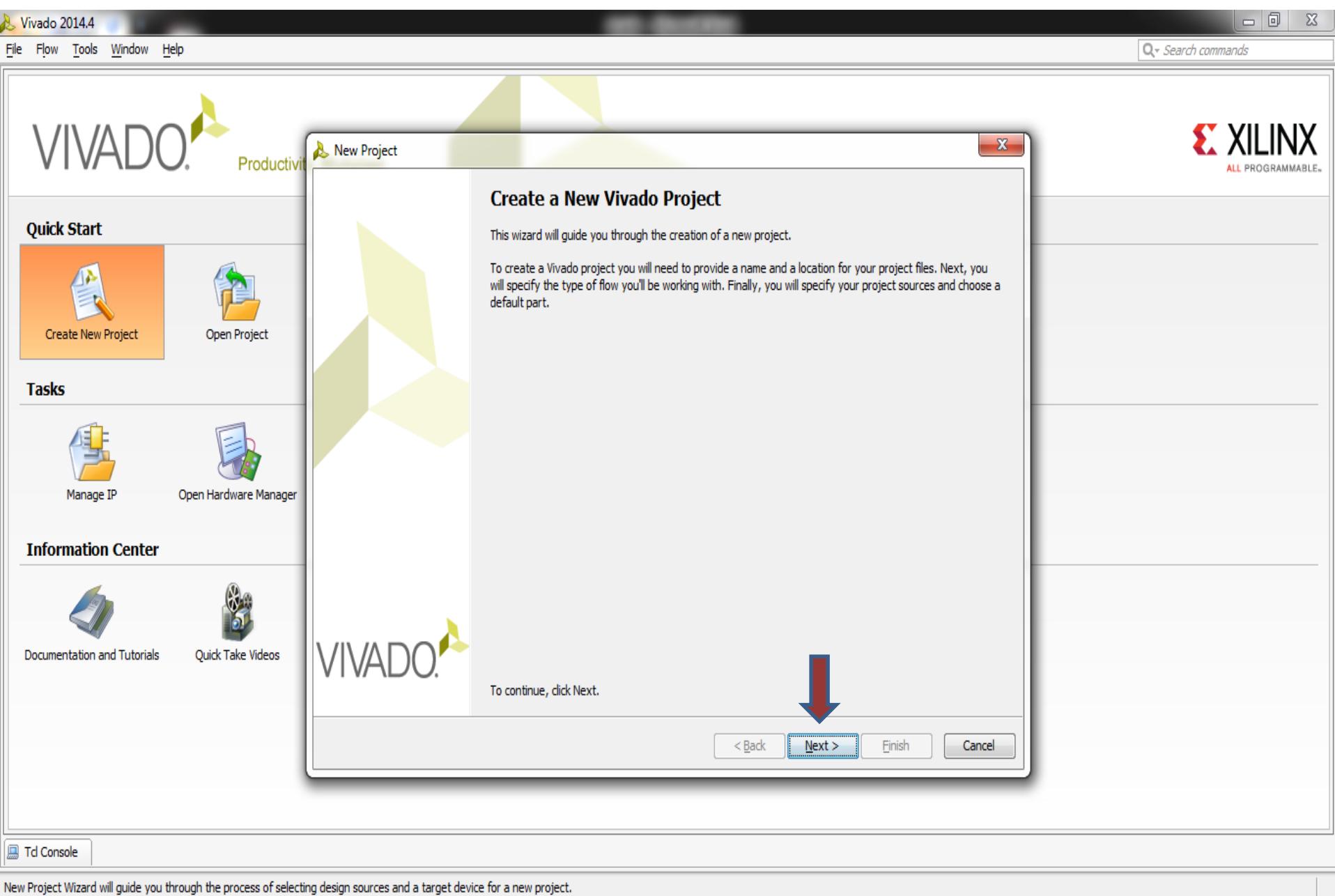
- How to create a new project.
- Execution of .vhd file without test bench.
- Execution of .vhd file with test bench.
- Power Calculation.

# 1. Creating New Project

0)Select Create New Project under the Quick Start

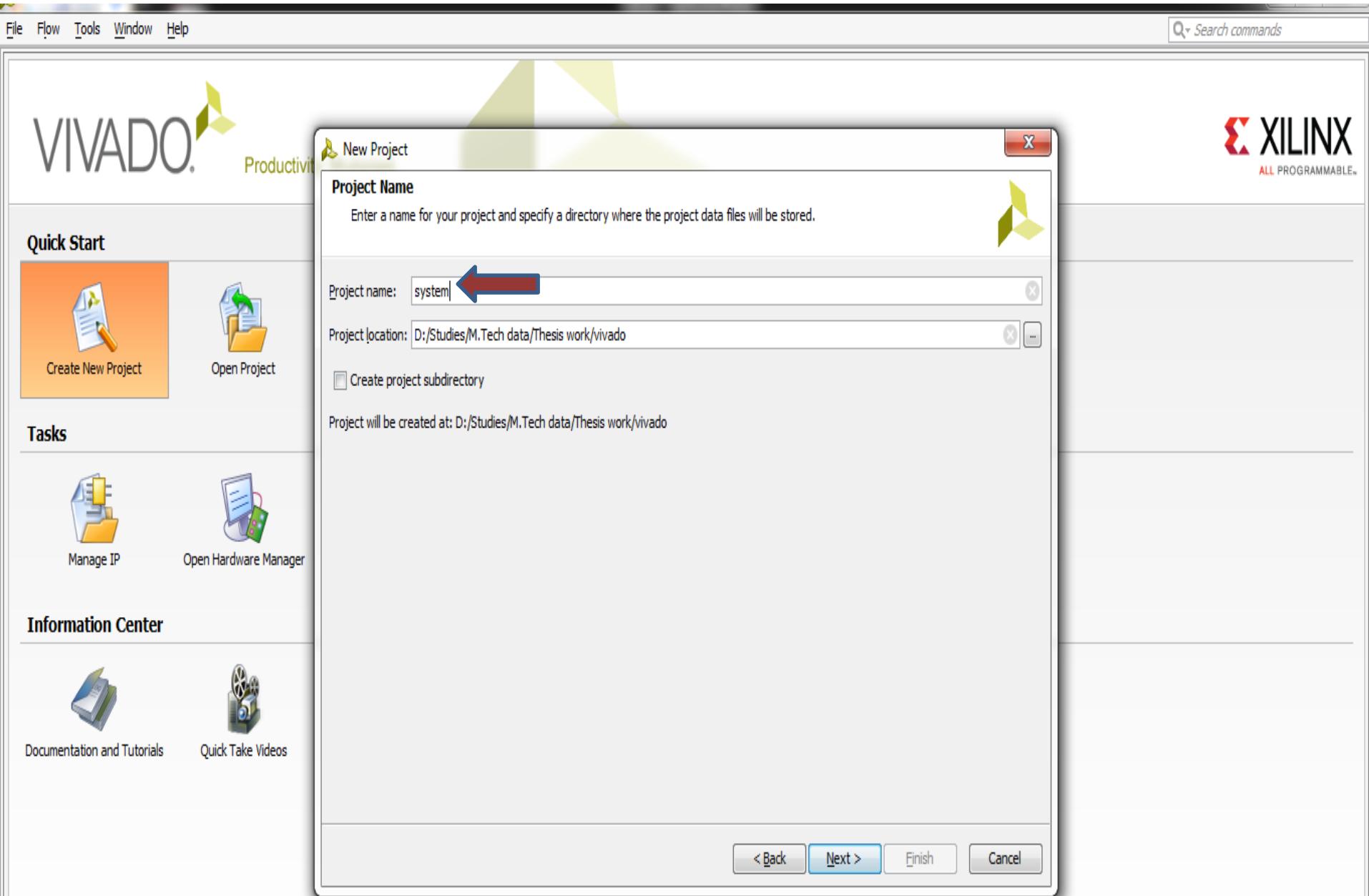


# i) Click on Next

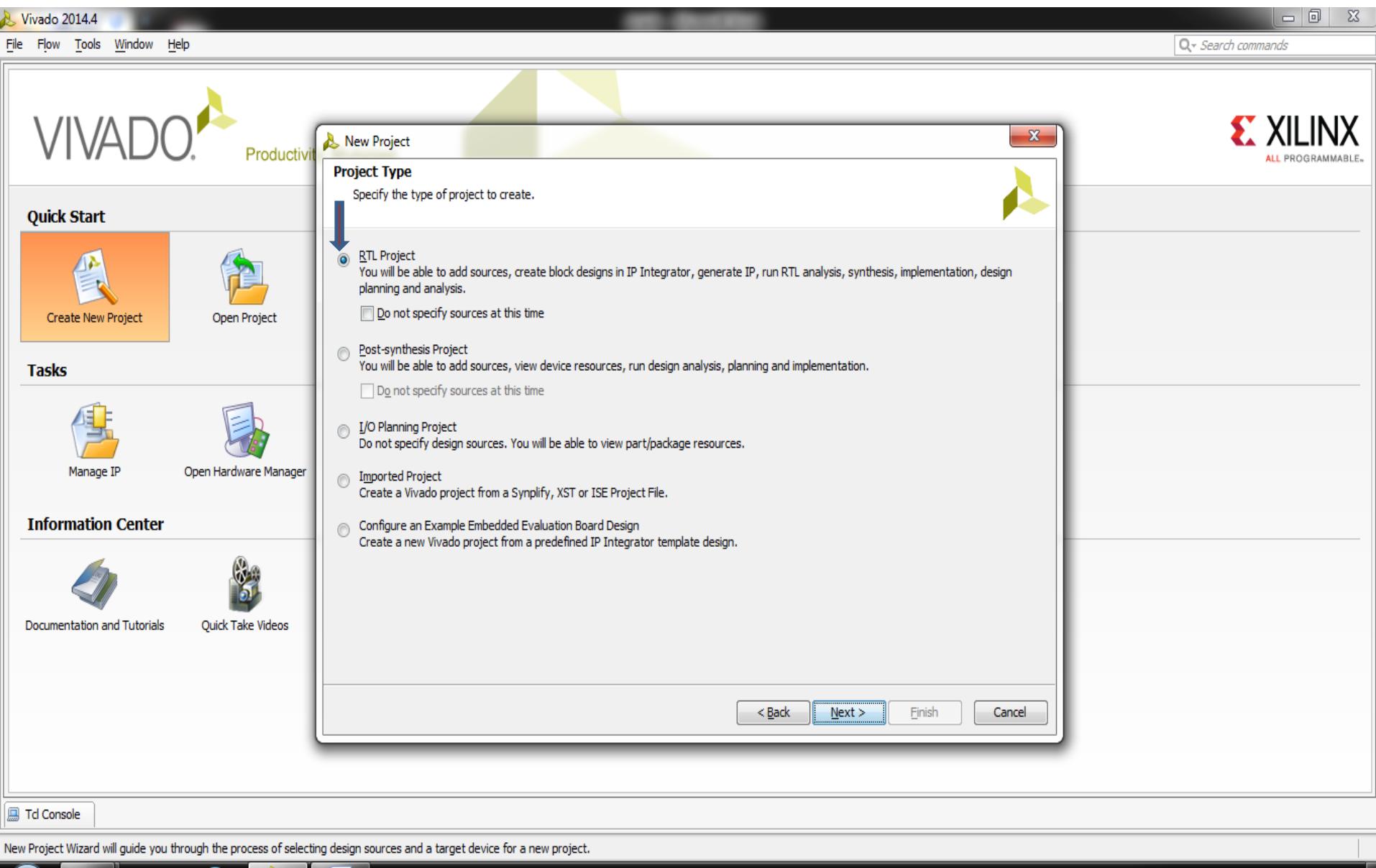


New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

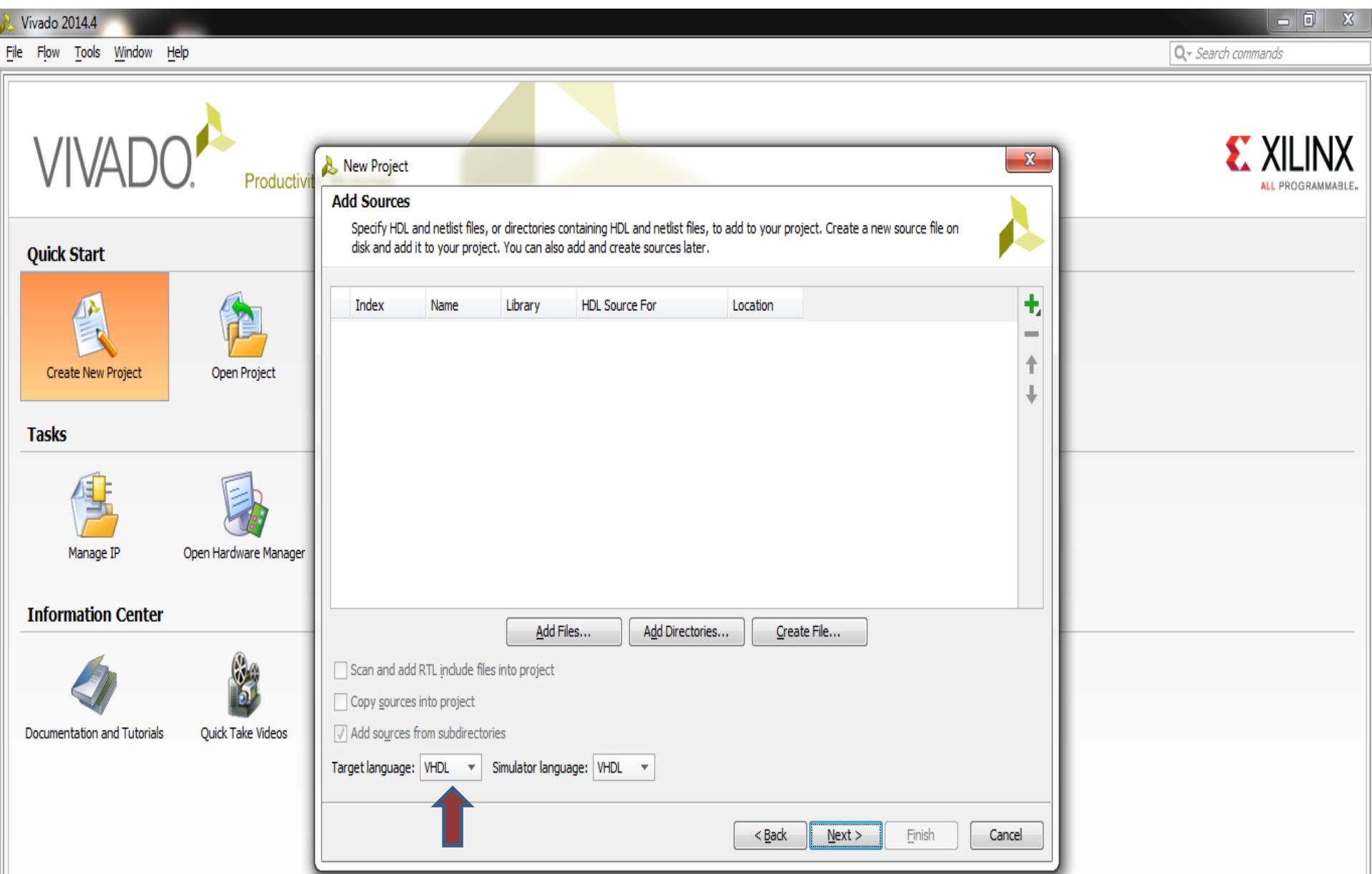
## ii)Specify the Project Name



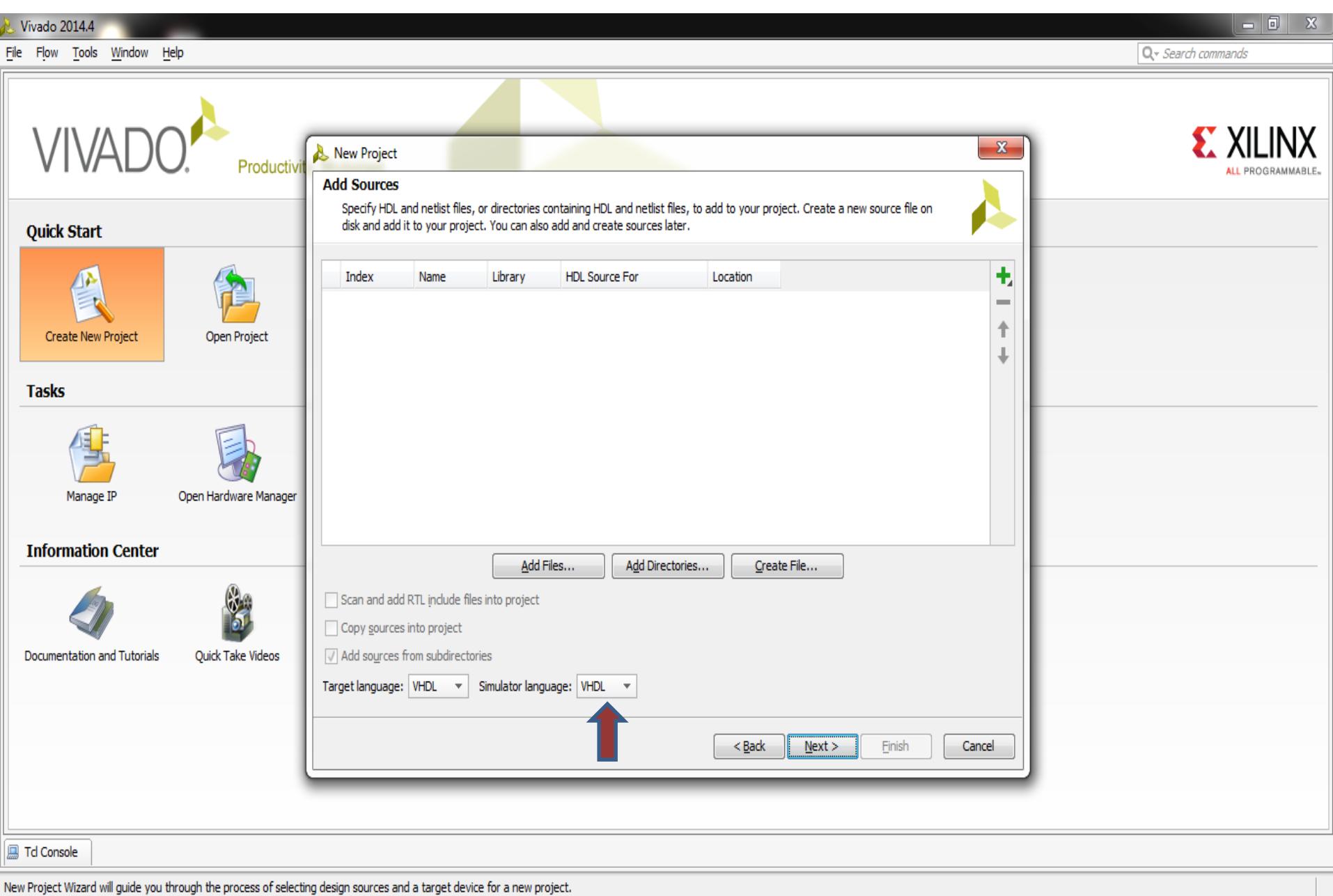
### iii)Select the Project type



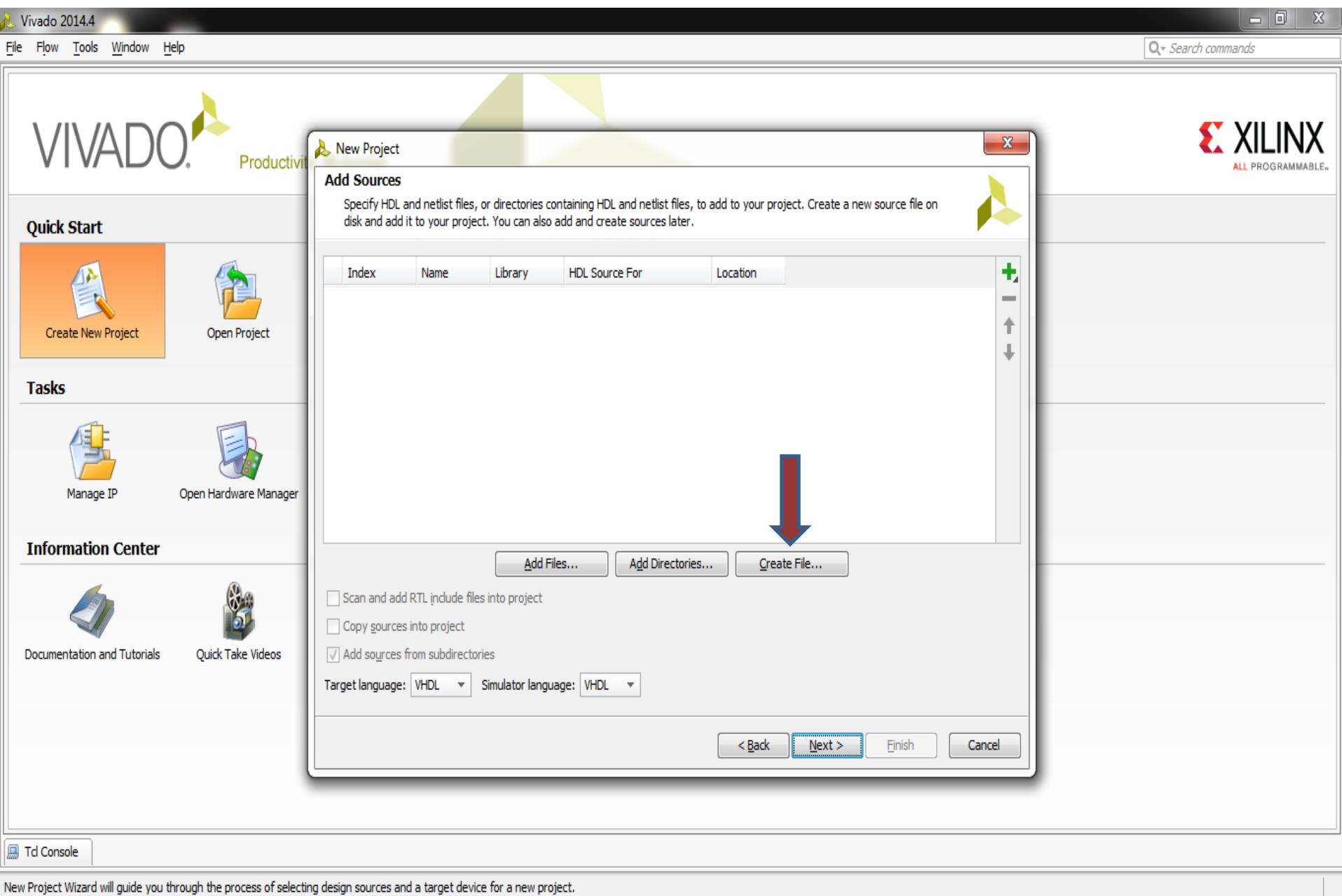
#### iv) Select The target language as VHDL



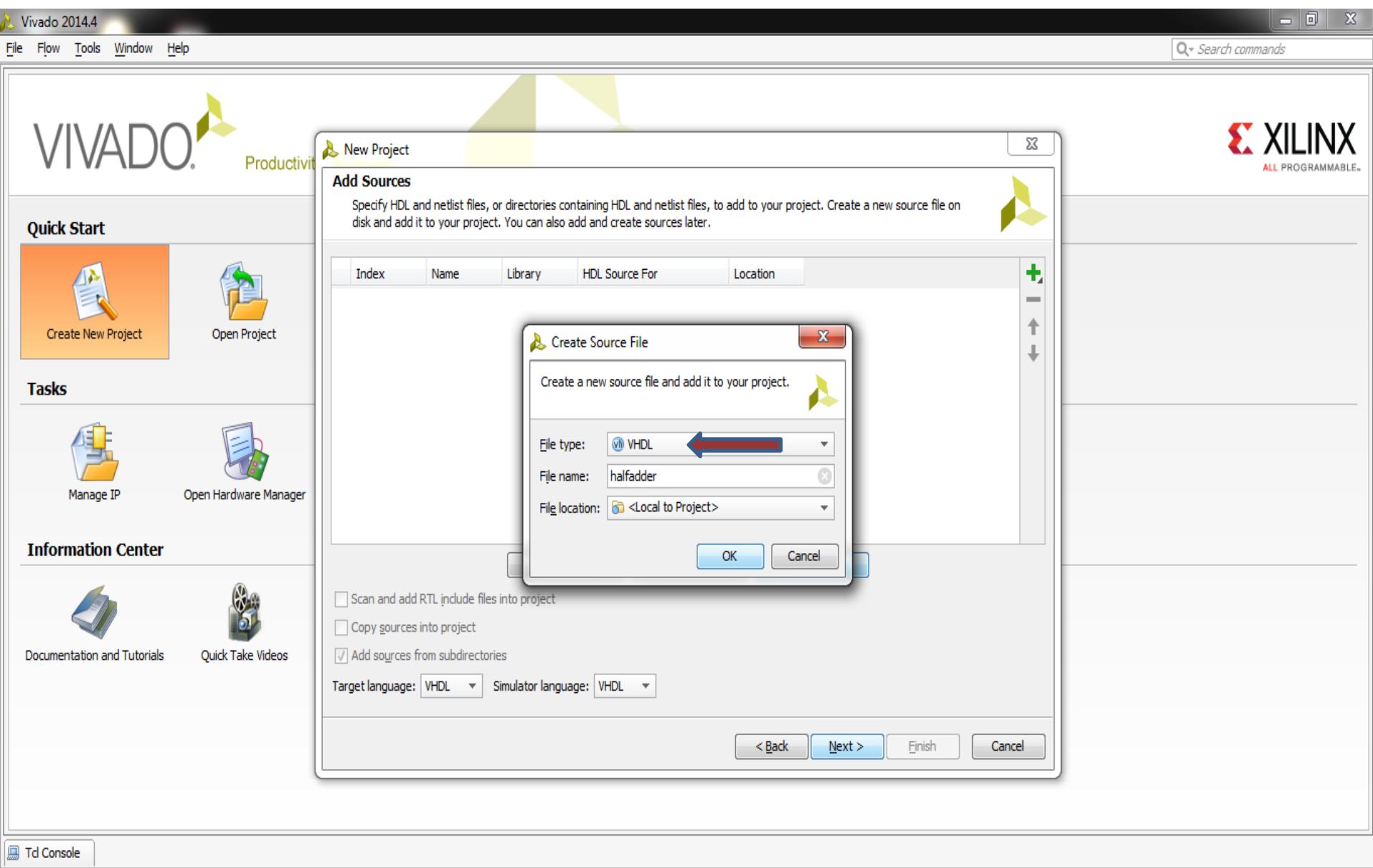
## v) Select the simulator language as VHDL



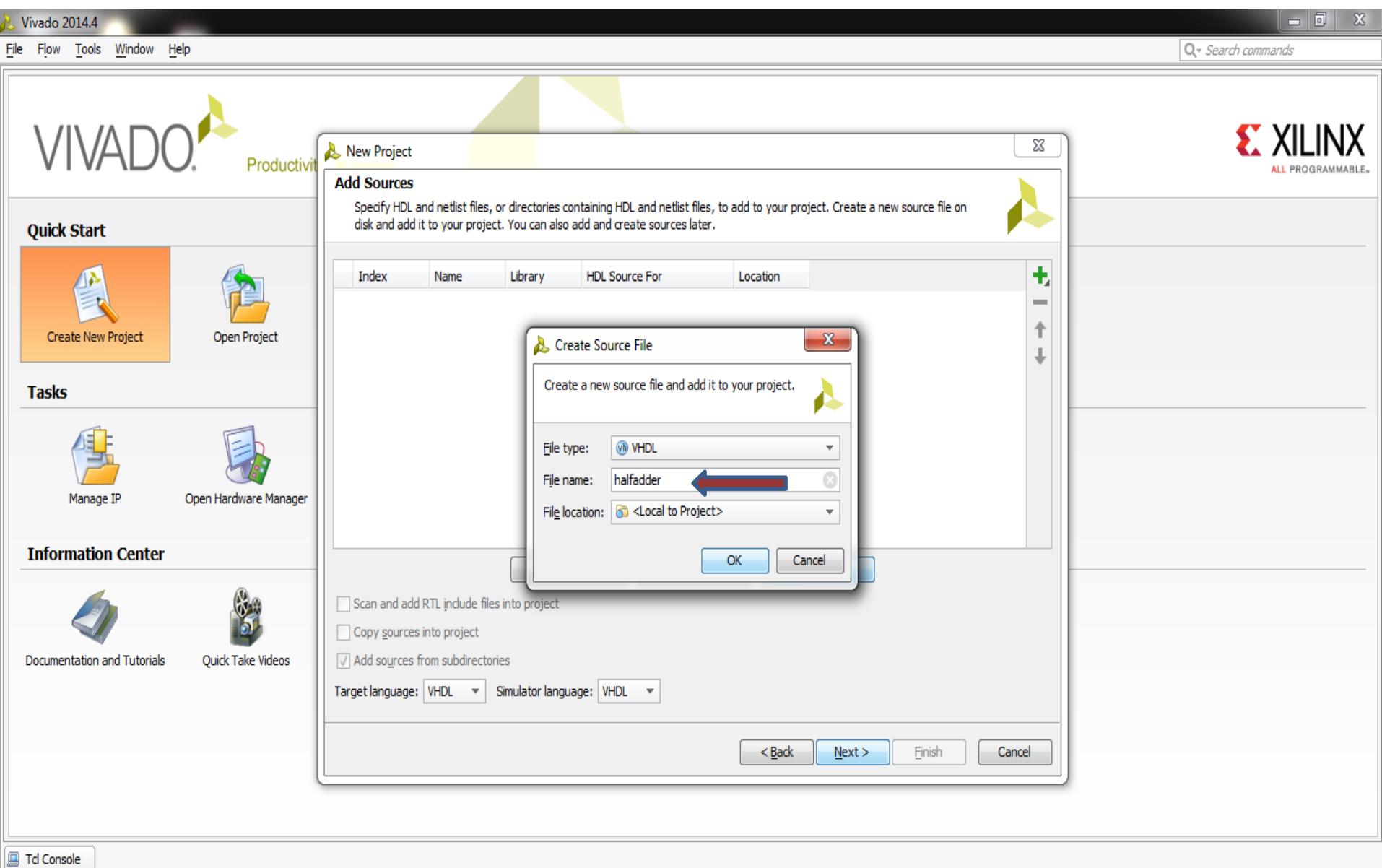
## vi) Click on Create File



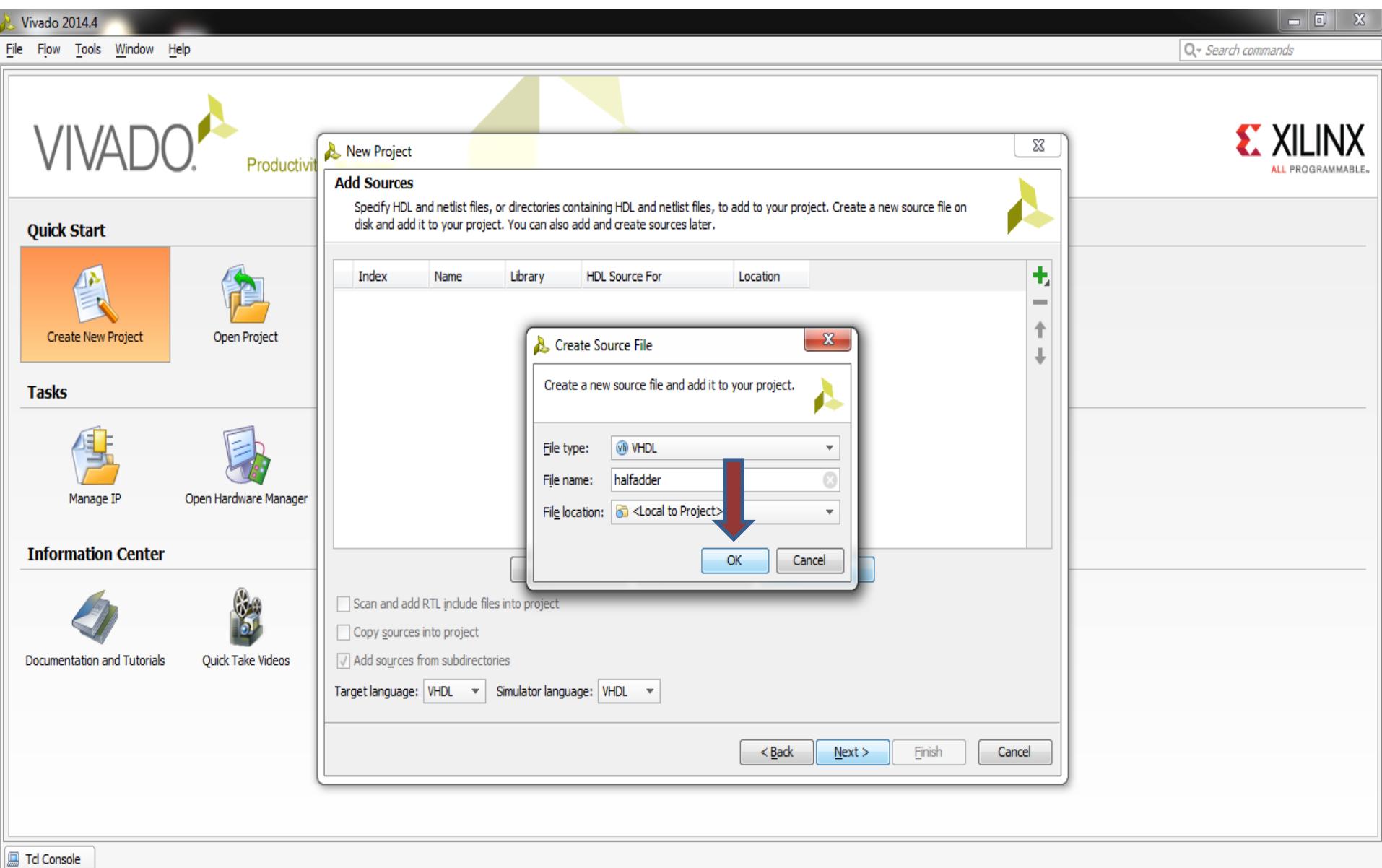
## vii) Select File Type



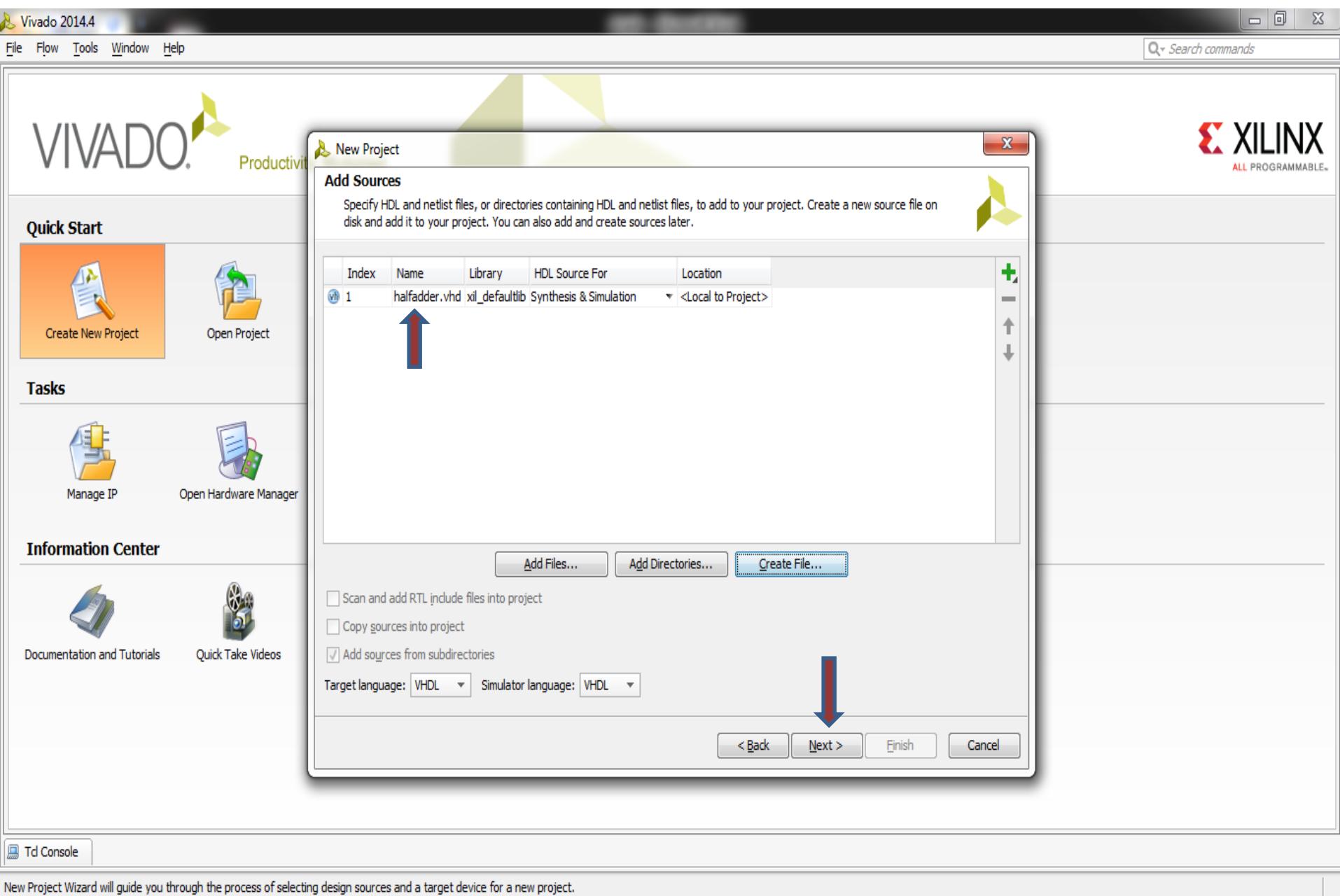
## viii) Specify the File name



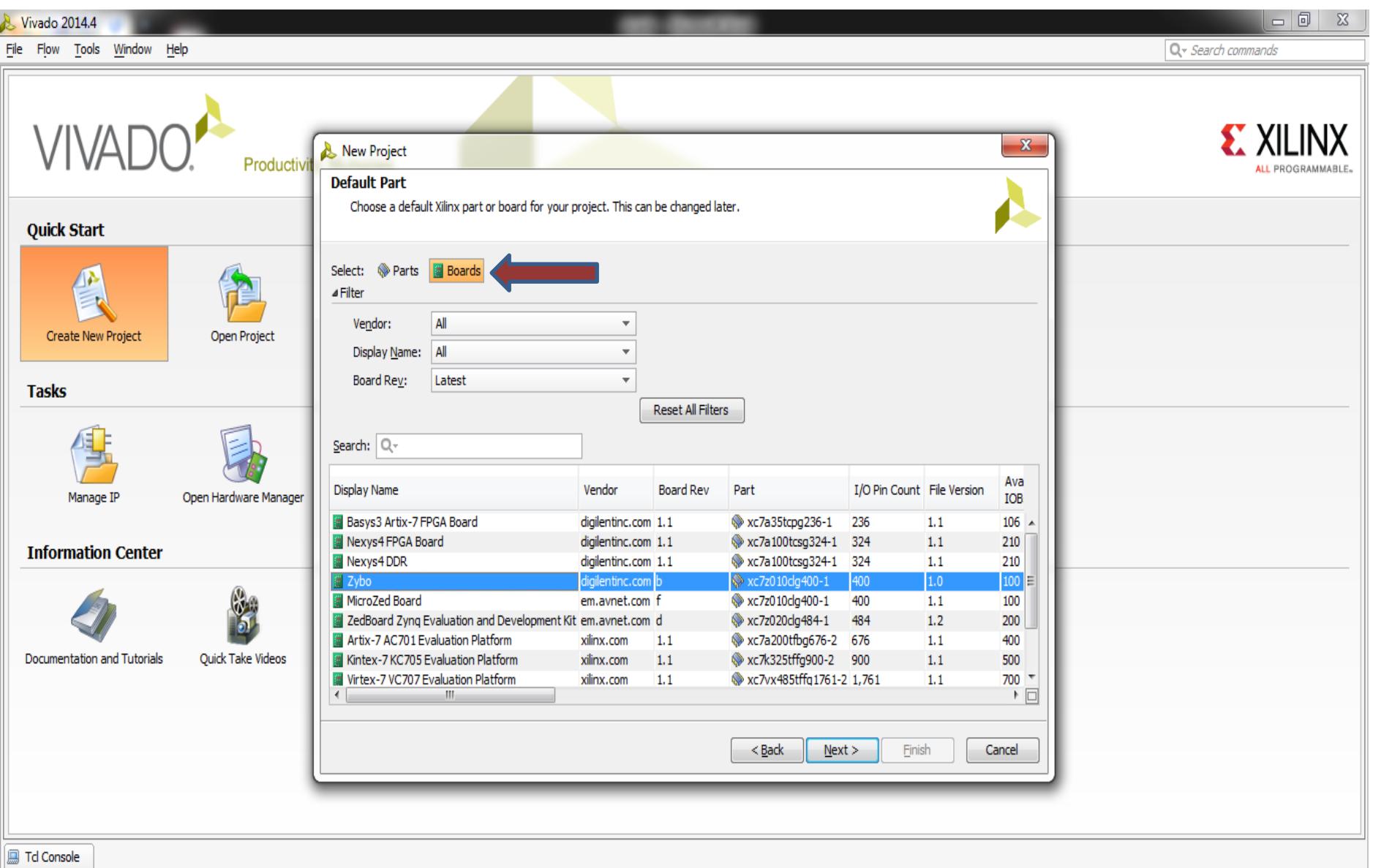
ix) Click on ok



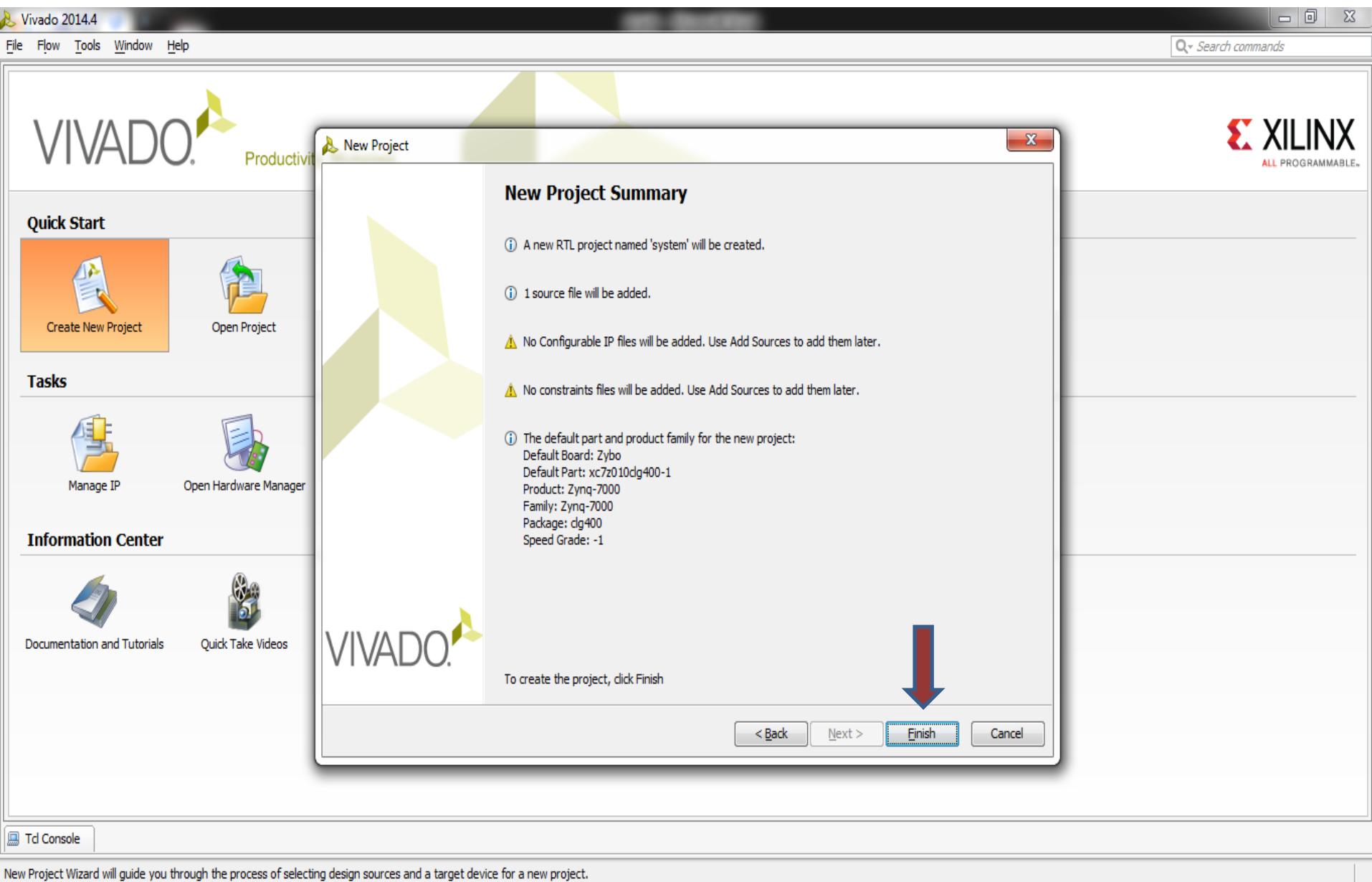
xi) Now Can see the specified file name and then click on Next



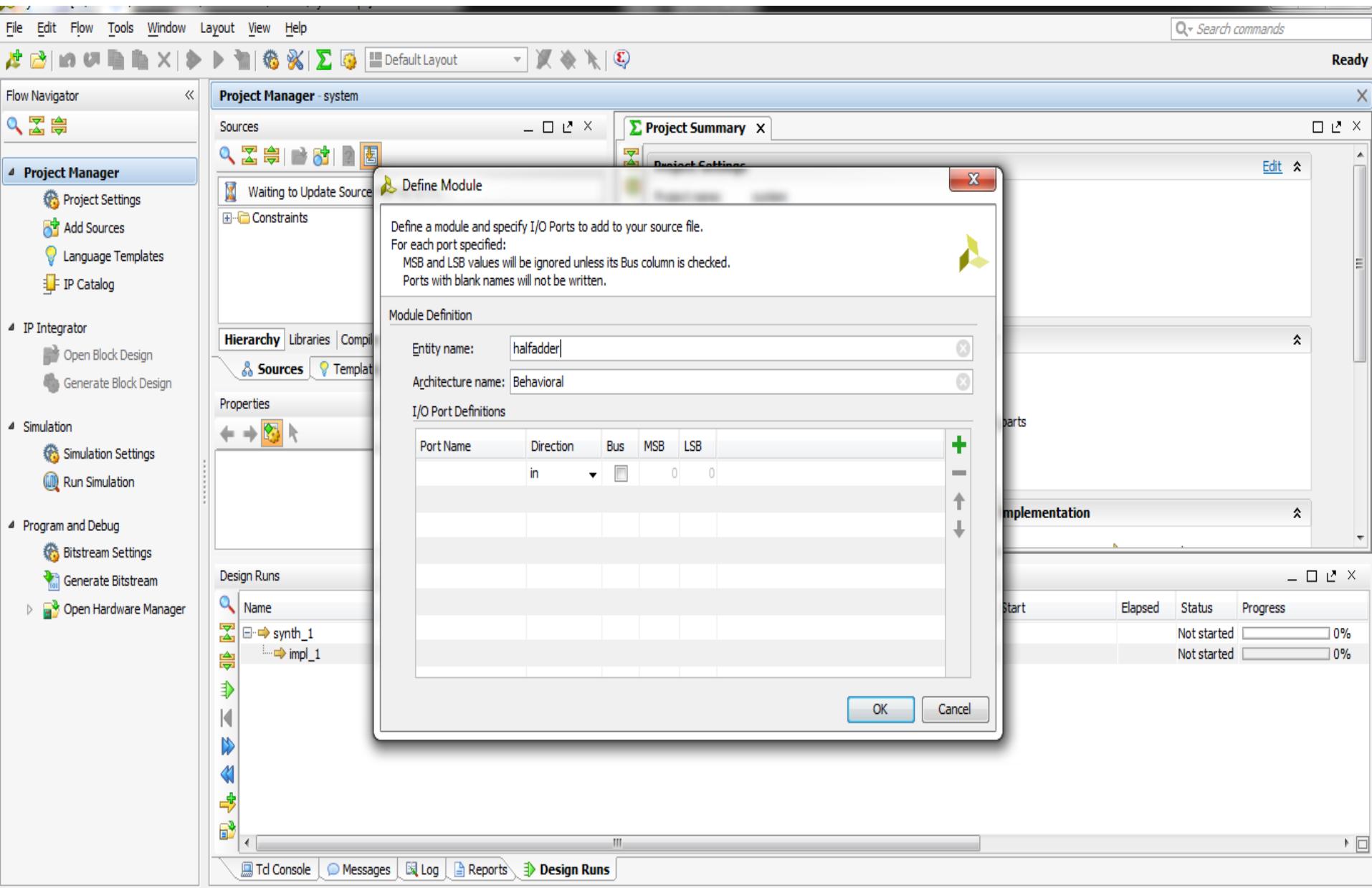
## xii) Select the tab Boards here



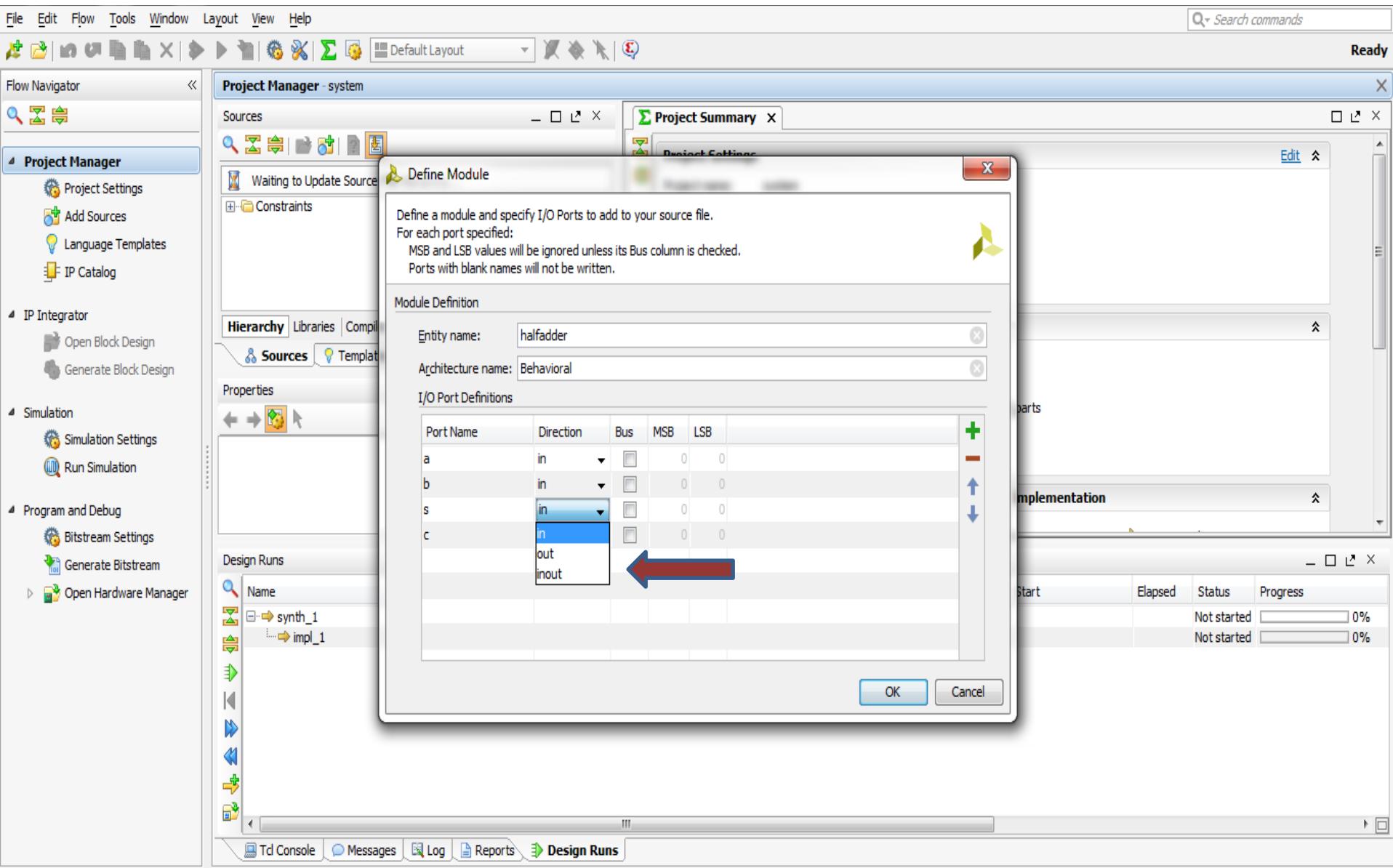
### xiii) Click on finish



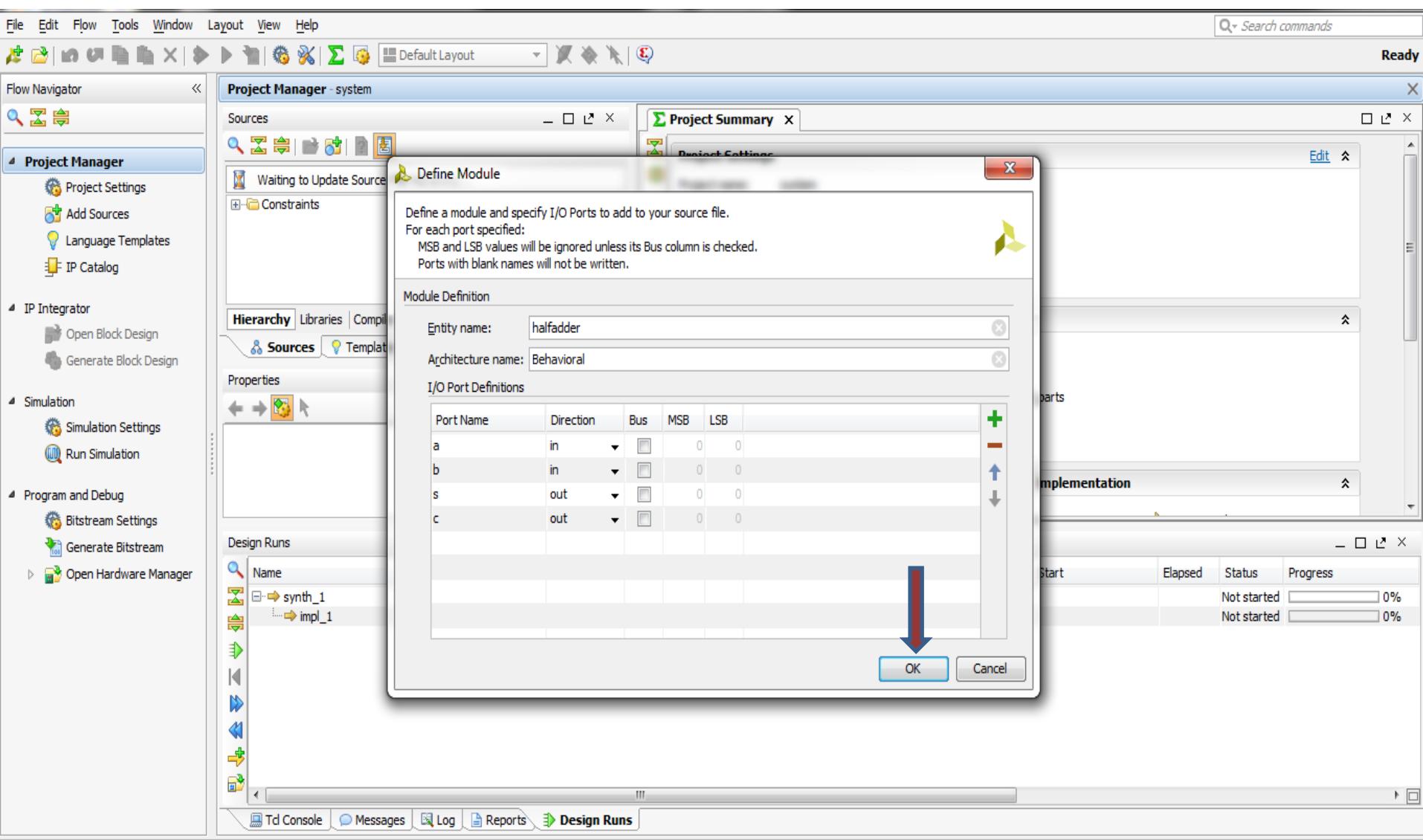
#### xiv) Now we can specify the input and output variables here.



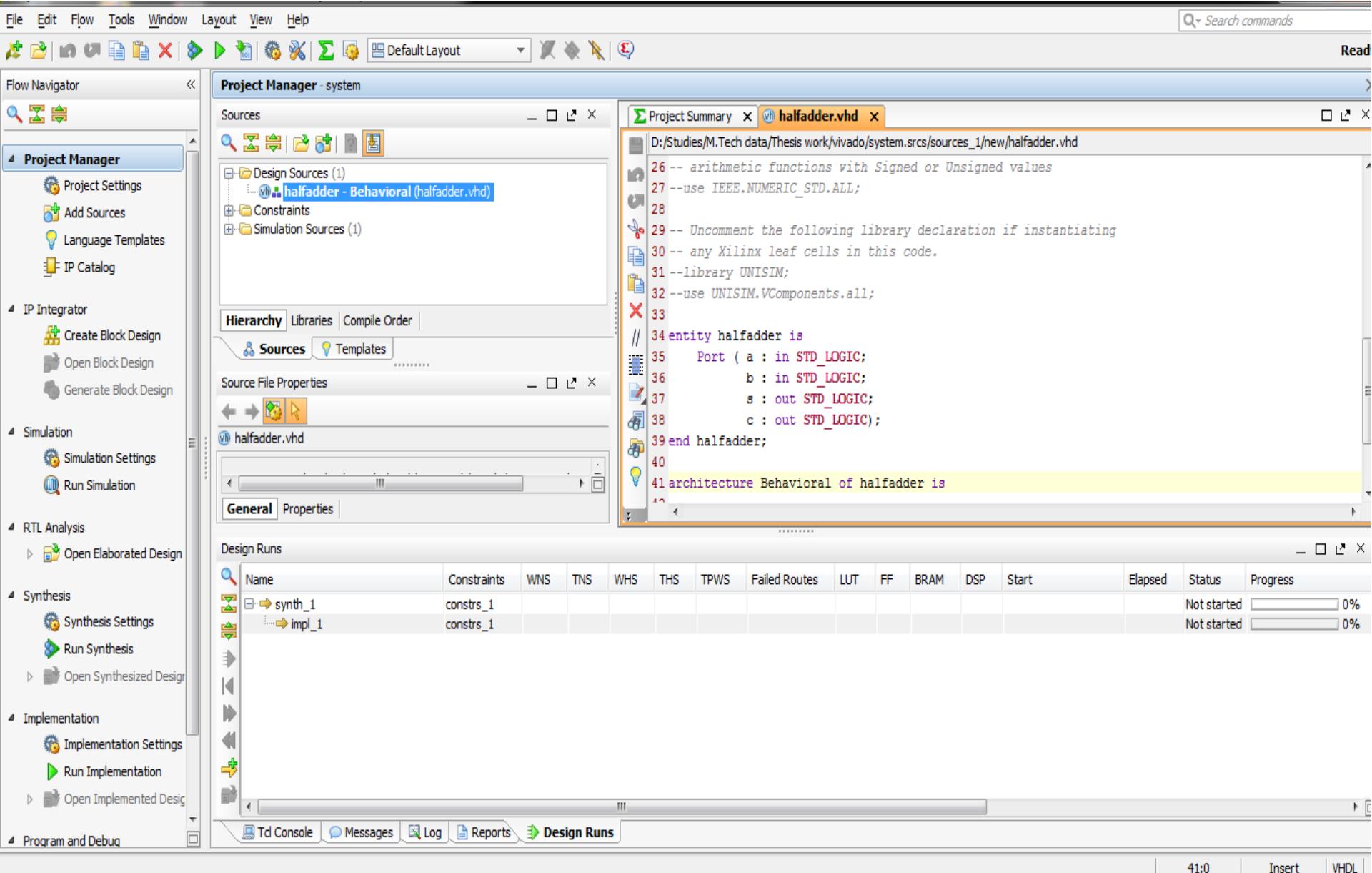
xv) For output variables we need to select out as a type like as shown



xvi) Click on ok then it will automatically generate the entity part.



xvii) Double Click on the file name then the file will open.



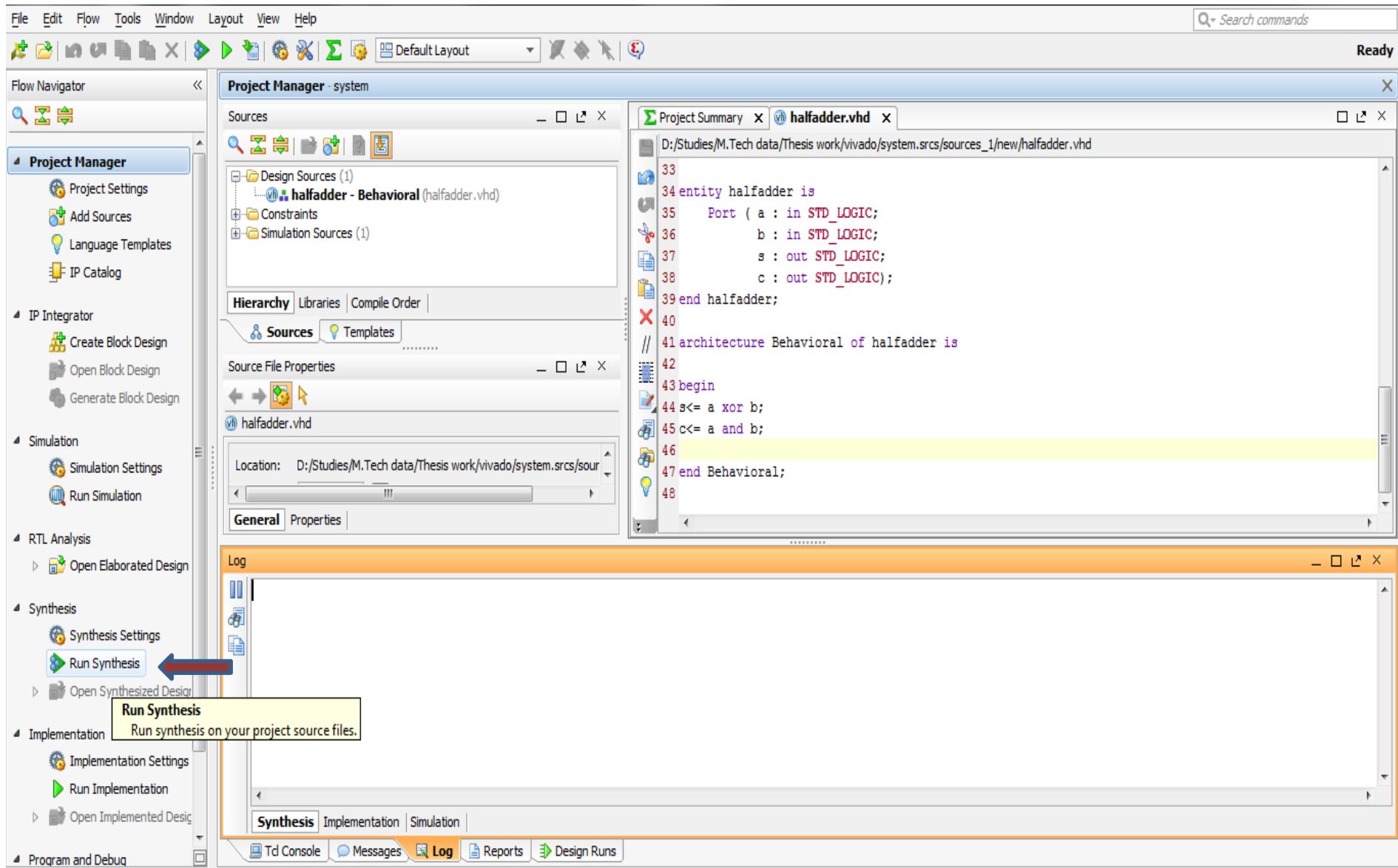
xviii) Now we have to write the operation of the circuit and then save it.

The screenshot shows the Vivado IDE interface with the Project Manager open. The code editor displays a VHDL file named `halfadder.vhd`. The code defines a half adder entity and architecture. A callout box highlights the assignment statements for the sum and carry outputs.

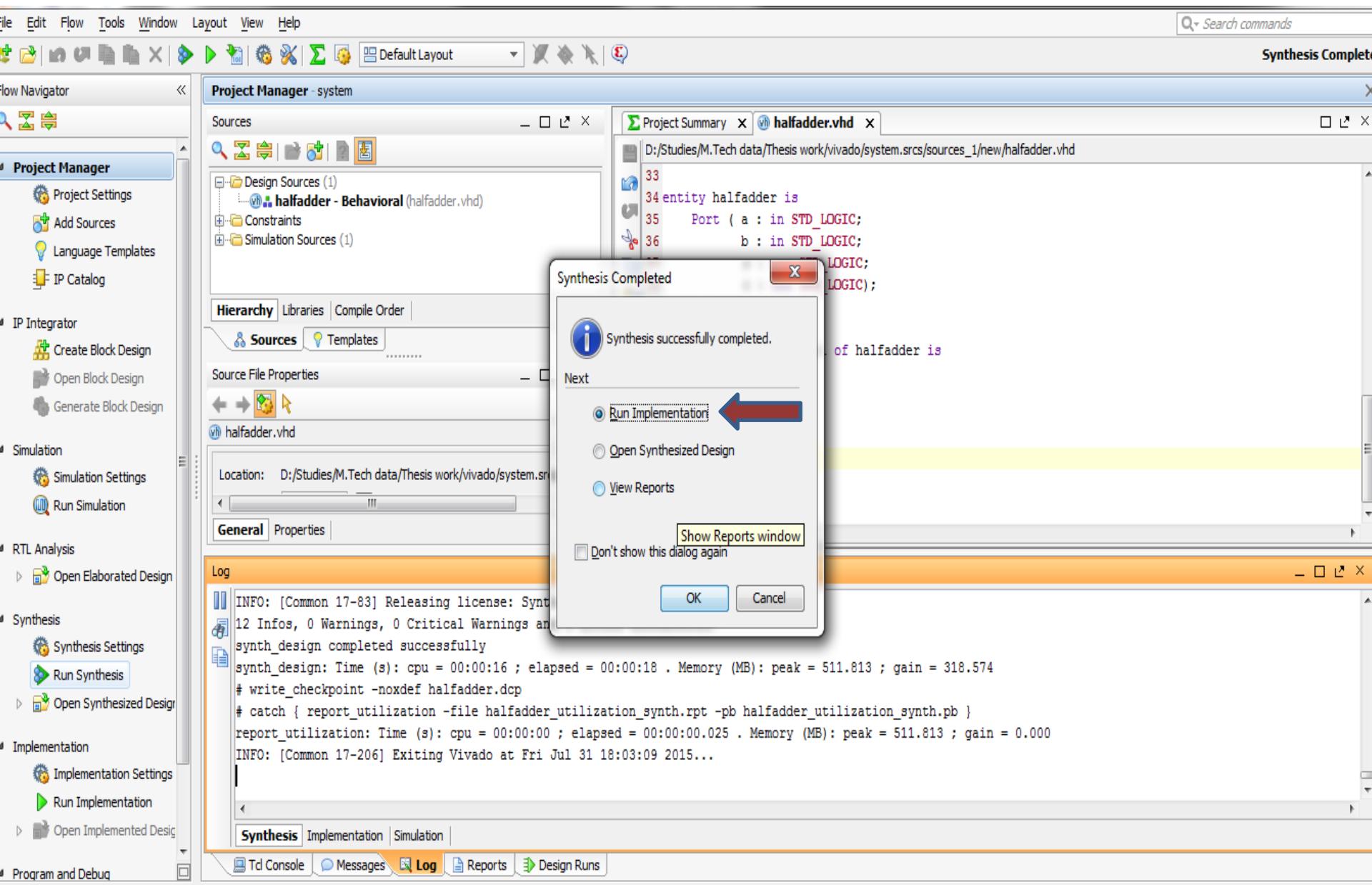
```
19
20
21
22 library IEEE;
23 use IEEE.STD_LOGIC_1164.ALL;
24
25 -- Uncomment the following library declaration if using
26 -- arithmetic functions with Signed or Unsigned values
27 --use IEEE.NUMERIC_STD.ALL;
28
29 -- Uncomment the following library declaration if instantiating
30 -- any Xilinx leaf cells in this code.
31 --library UNISIM;
32 --use UNISIM.VComponents.all;
33
34 entity halfadder is
35     Port ( a : in STD_LOGIC;
36            b : in STD_LOGIC;
37            s : out STD_LOGIC;
38            c : out STD_LOGIC);
39 end halfadder;
40
41 architecture Behavioral of halfadder is
42
43 begin
44     s<= a xor b;
45     c<= a and b;
46
47 end Behavioral;
48
```

These two lines performs the operation of half adder

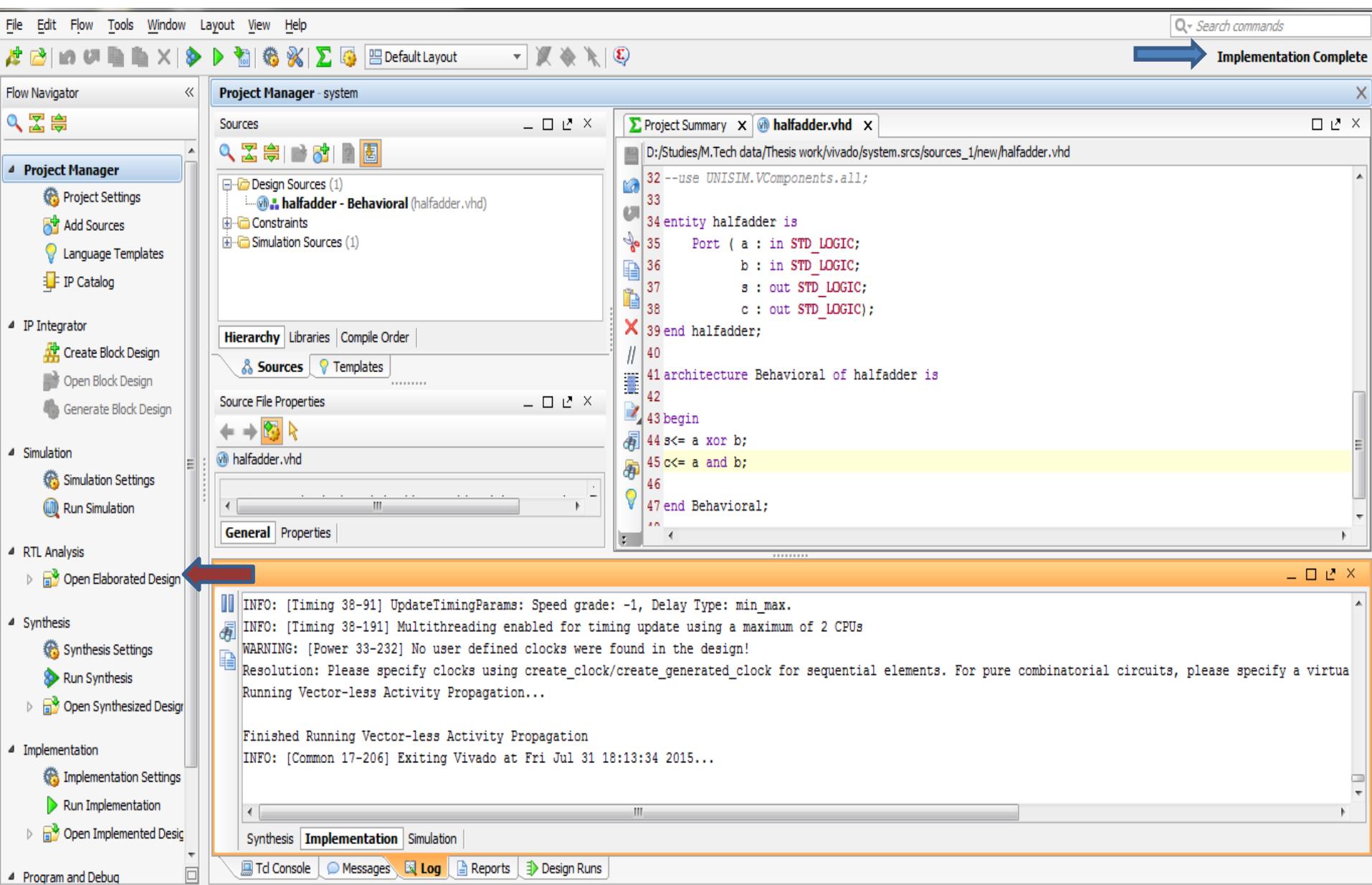
# xix) Now we need to synthesis the program, Click on Run Synthesis



## xx) After once Synthesis is completed, Click on Run Implementation



## xxi) After Once implementation done Click on open elaborated design



## xxii) Now it Shows the RTL schematic diagram of that circuit.

Screenshot of the Quartus Prime software interface showing the RTL Schematic view for a halfadder design.

The top menu bar includes: File, Edit, Flow, Tools, Window, Layout, View, Help, and a Search commands field.

The status bar indicates "Implementation Complete".

The left sidebar contains the Project Manager, IP Integrator, Simulation, and RTL Analysis sections. The RTL Analysis section is currently active, showing the "Elaborated Design" for the project "xc7z010clg400-1".

The main workspace displays the "RTL Schematic" tab, which shows the internal logic of the halfadder. The schematic consists of two AND gates (RTL\_AND) and one XOR gate (RTL\_XOR). The inputs are labeled  $a$  and  $b$ . The first AND gate has its output connected to the positive input of the XOR gate. The second AND gate has its output connected to the negative input of the XOR gate. The outputs of the XOR gate are labeled  $c$  and  $s$ .

The bottom navigation bar includes: Td Console, Messages, Log, Reports, and Design Runs.

Name	Constraints	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM	DSP	Start	Elapsed	Status	Progress
synth_1	constrs_1	0.00	0.00	0.00	0.00	0.00	0	0.01	0.00	0.00	0.00	7/31/15 6:11 PM	00:00:25	synth_design Complete!	
impl_1	constrs_1	0.00	0.00	0.00	0.00	0.00	0	0.01	0.00	0.00	0.00	7/31/15 6:12 PM	00:01:06	route_design Complete!	

## xxiii) It Shows the static power of the circuit.

The screenshot shows the Xilinx Vivado IDE interface. A red arrow points from the top center down to the 'Project Summary' tab in the central workspace. Another red arrow points from the bottom right corner up to the 'Power' section in the same workspace. The 'Project Summary' tab is active, displaying utilization graphs and tables for Post-Synthesis and Post-Implementation. The 'Power' section shows static power consumption details.

**Project Summary - Utilization - Post-Implementation**

Category	Utilization (%)
LUT	1%
I/O	4%

**Power**

Parameter	Value
Total On-Chip Power:	0.771 W
Junction Temperature:	33.9 °C
Thermal Margin:	51.1 °C (4.3 W)
Effective ΔJA:	11.5 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

**Design Runs**

Name	Constraints	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM	DSP	Start	Elapsed	Status	Progress
synth_1	constrs_1							0.01	0.00	0.00	0.00	8/1/15 4:44 PM	00:00:32	synth_design Complete!	
impl_1	constrs_1	0.00	0.00	0.00	0.00	0.00	0	0.01	0.00	0.00	0.00	8/1/15 4:44 PM	00:01:22	route_design Complete!	

**Implementation**

- Implementation Settings
- Run Implementation
- Implemented Design
- Constraints Wizard

File Edit Flow Tools Window Layout View Help Search commands Implementation Complete

## xxiv) It Shows the usage of LUT's and I/O.

The screenshot shows the Vivado IDE interface with the following details:

- File Navigator**: Shows the project structure with a **halfadder** folder containing **Nets (8)** and **Leaf Cells (6)**.
- Implementation Complete**: Status message in the top right.
- Project Summary** window (highlighted with an orange border):
  - Utilization - Post-Implementation** table:

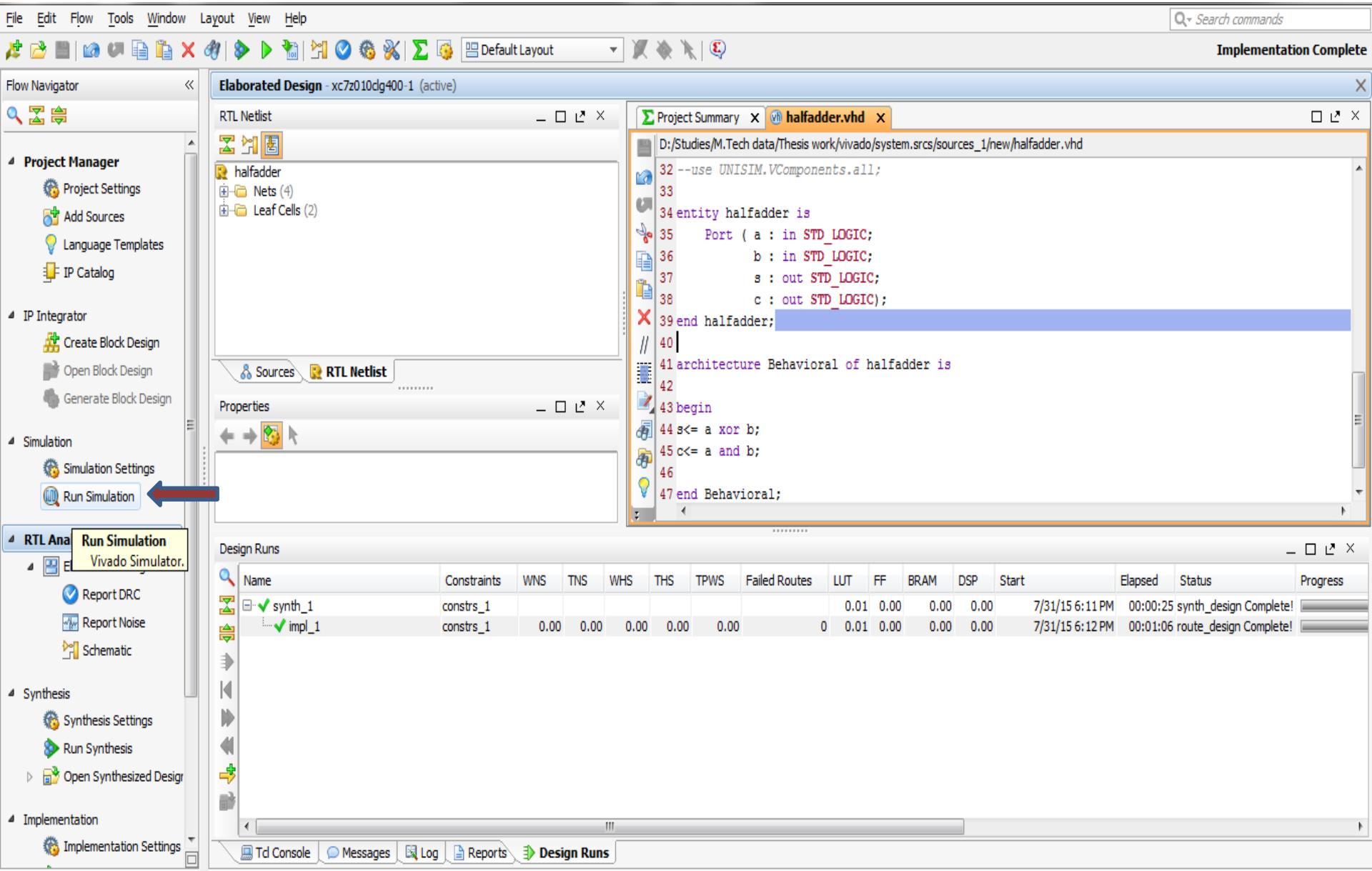
Resource	Utilization	Available	Utilization %
LUT	1	17600	0.01
I/O	4	100	4.00
  - Power** section:
    - Total On-Chip Power: 0.771 W
    - Junction Temperature: 33.9 °C
    - Thermal Margin: 51.1 °C (4.3 W)
    - Effective dJA: 11.5 °C/W
    - Power supplied to off-chip devices: 0 W
    - Confidence level: Low
  - Summary** and **On-Chip** buttons.
- Log** window:

INFO: [Corectcl 2-168] The results of DRC are in file D:/Studies/M.Tech data/Thesis work/vivado/praveen/runs/impl\_1/halfadder\_drc\_routed.rpt.  
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max.  
INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs  
WARNING: [Power 33-232] No user defined clocks were found in the design!  
Resolution: Please specify clocks using create\_clock/create\_generated\_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock in the design.  
Running Vector-less Activity Propagation...

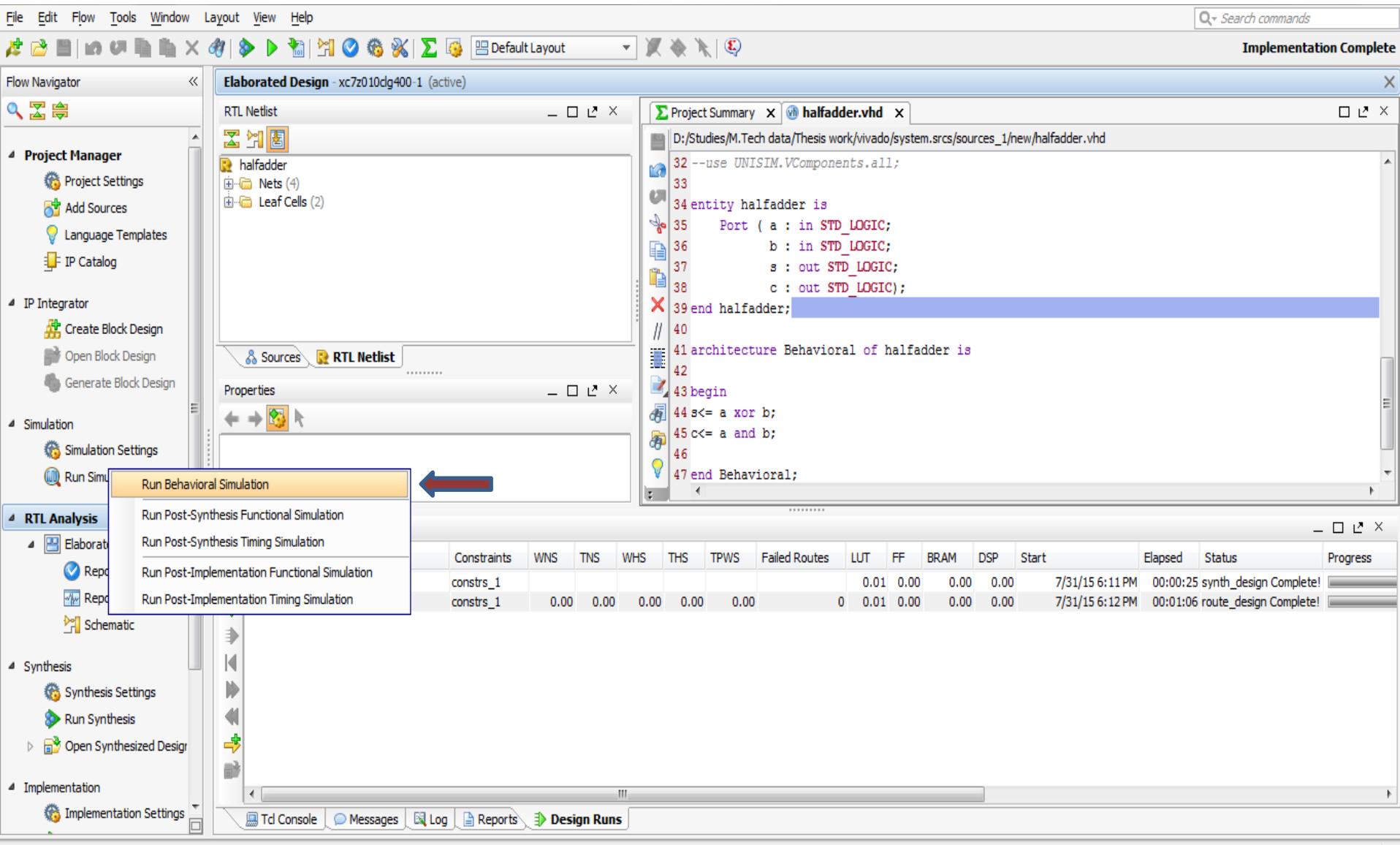
Finished Running Vector-less Activity Propagation  
INFO: [Common 17-206] Exiting Vivado at Sat Aug 01 17:06:02 2015...
- Implementation** tab selected in the bottom navigation bar.
- Td Console**, **Messages**, **Log**, **Reports**, **Design Runs**, and **Timing** tabs in the bottom navigation bar.

## 2. Run Simulation without Test Bench

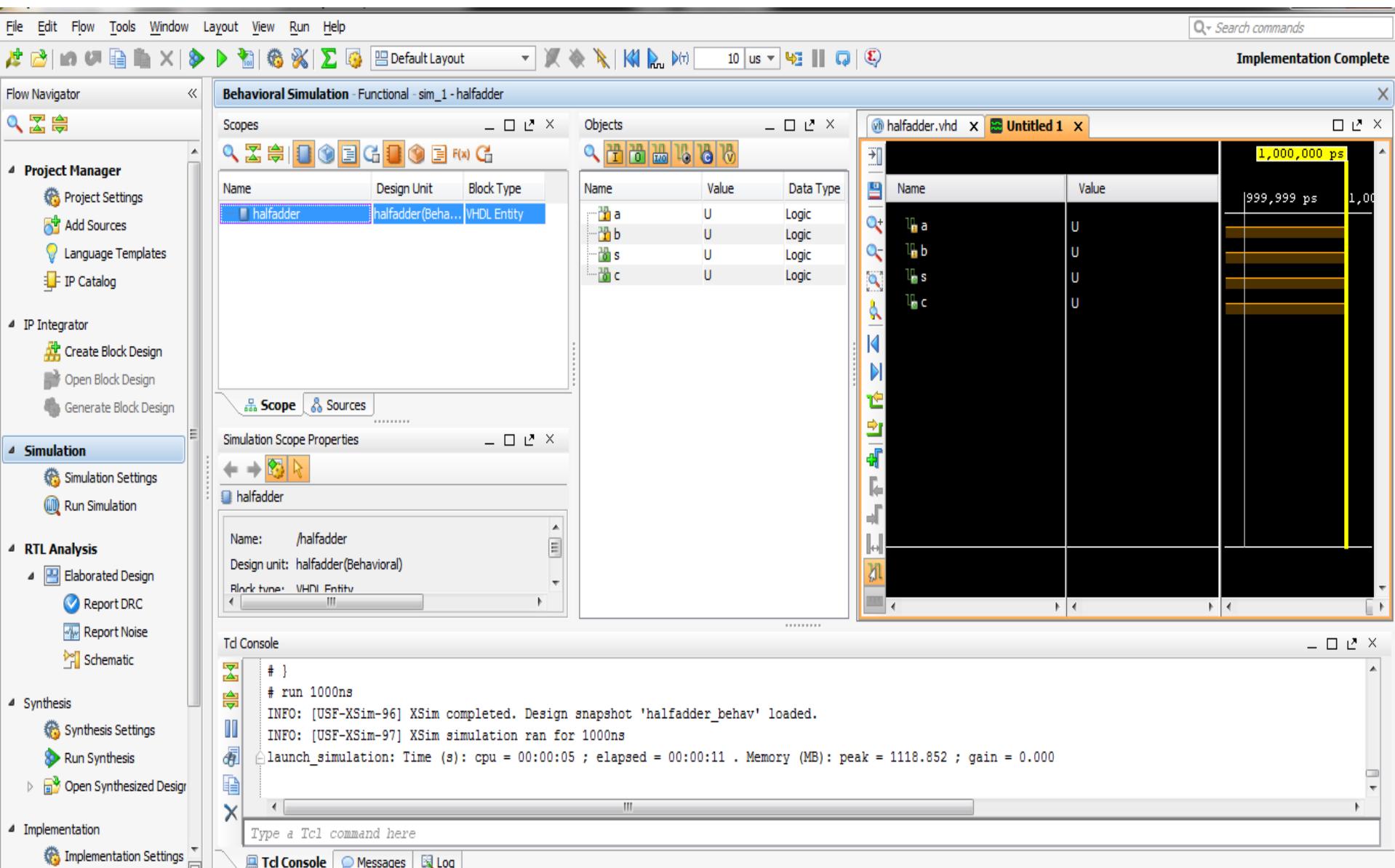
### i) Click on Run Simulation



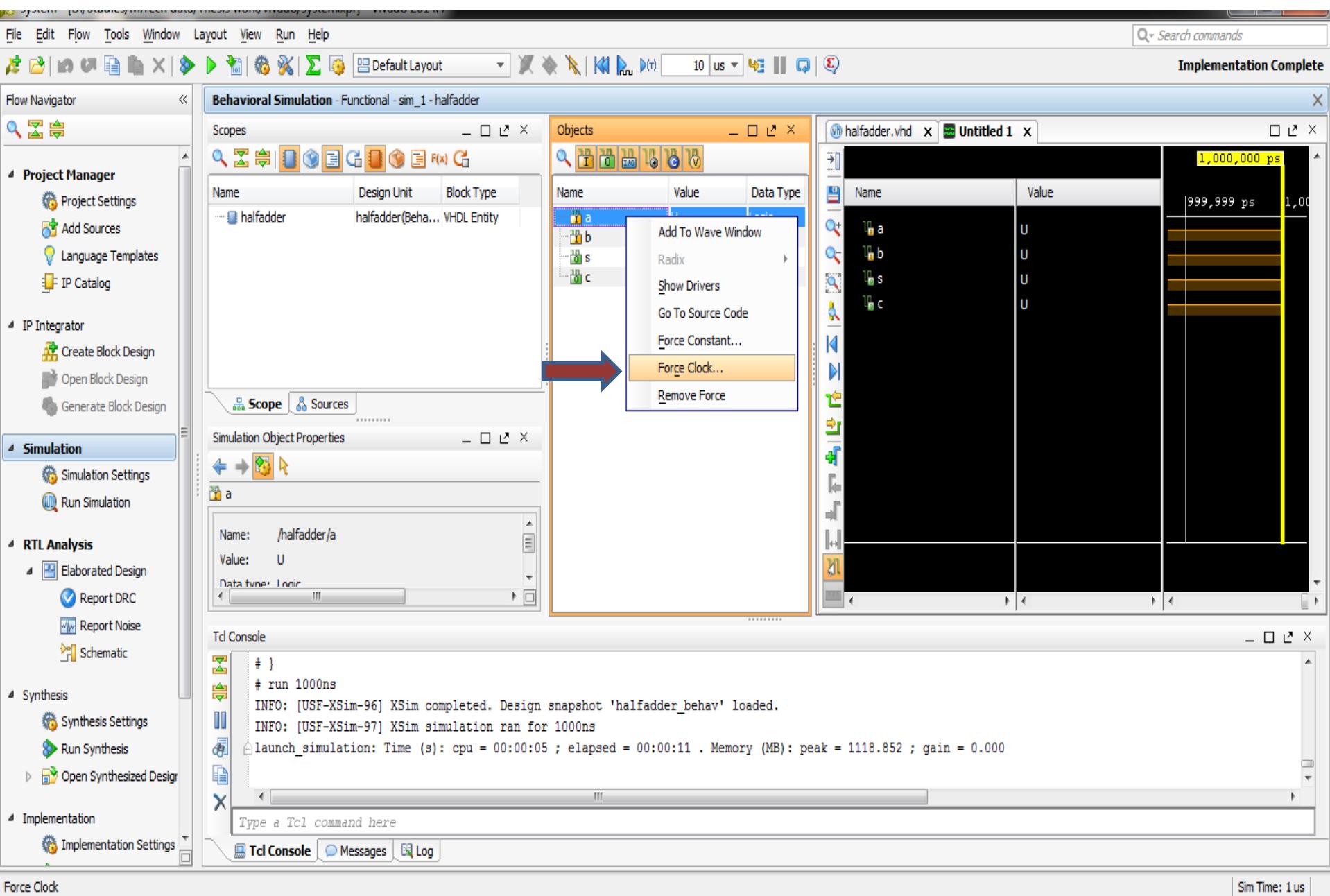
## ii) Select Run Behavioral Simulation



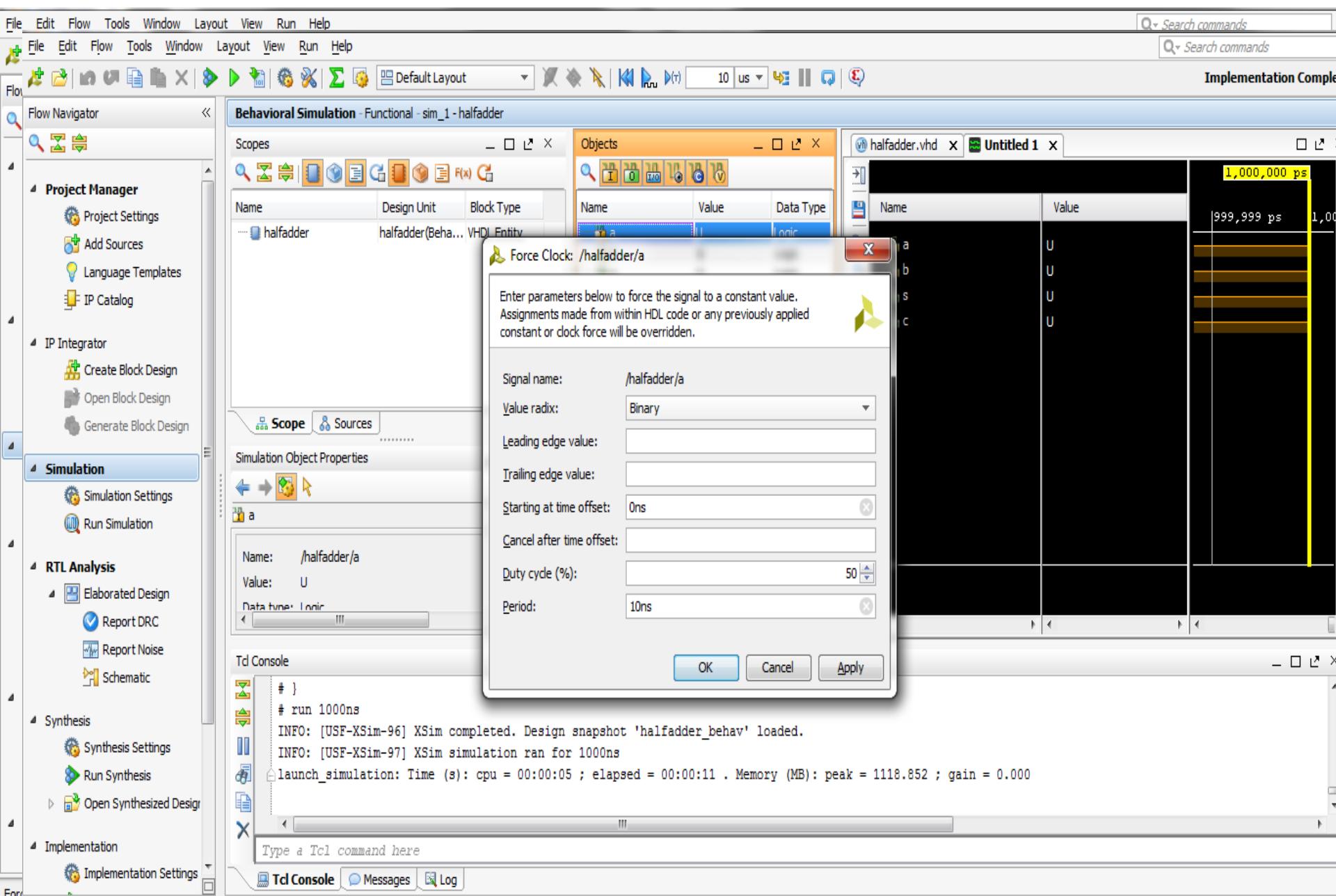
iii) Now this window popped up on screen.



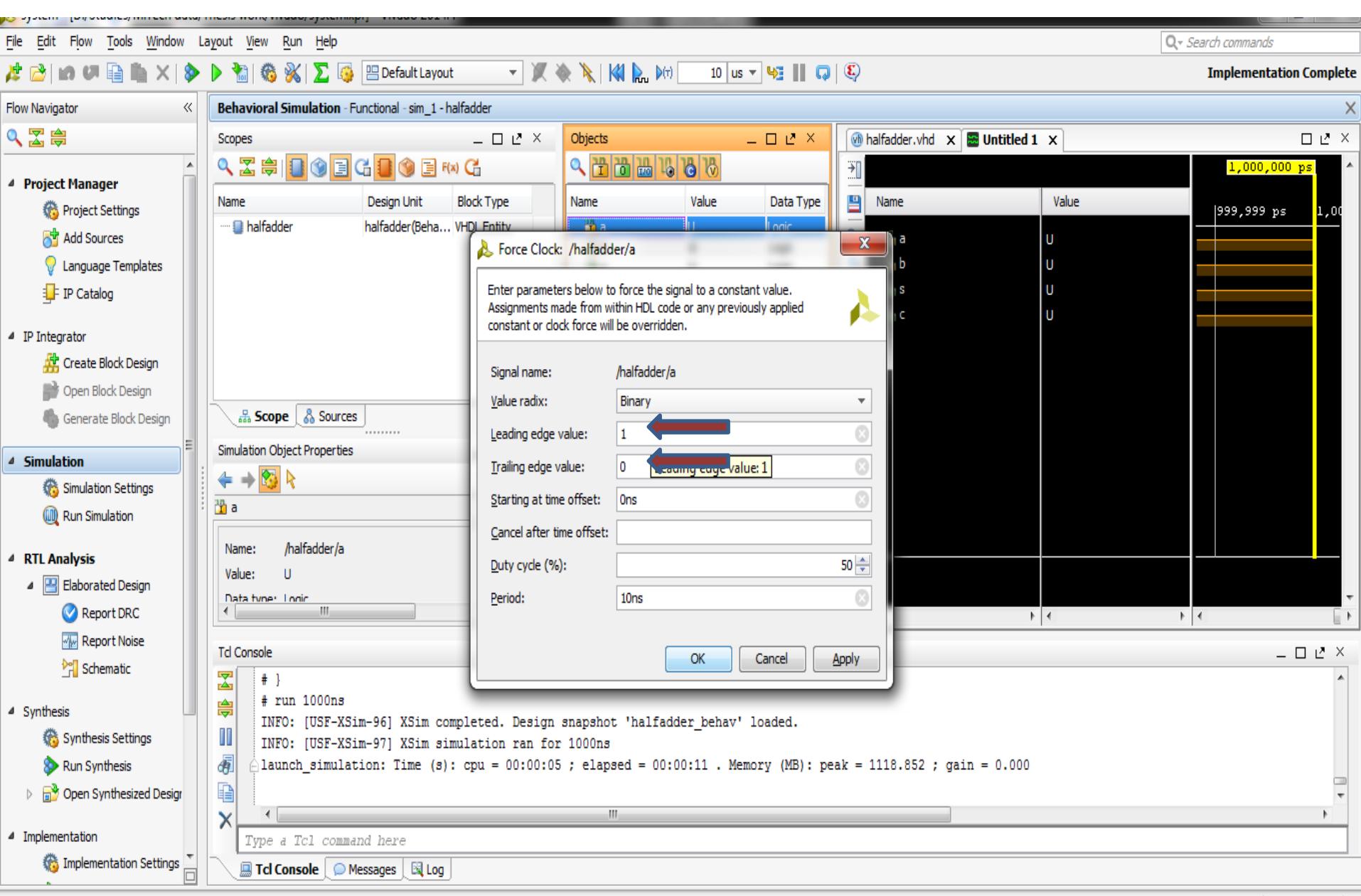
#### iv) Right click on input variable and select for force clock



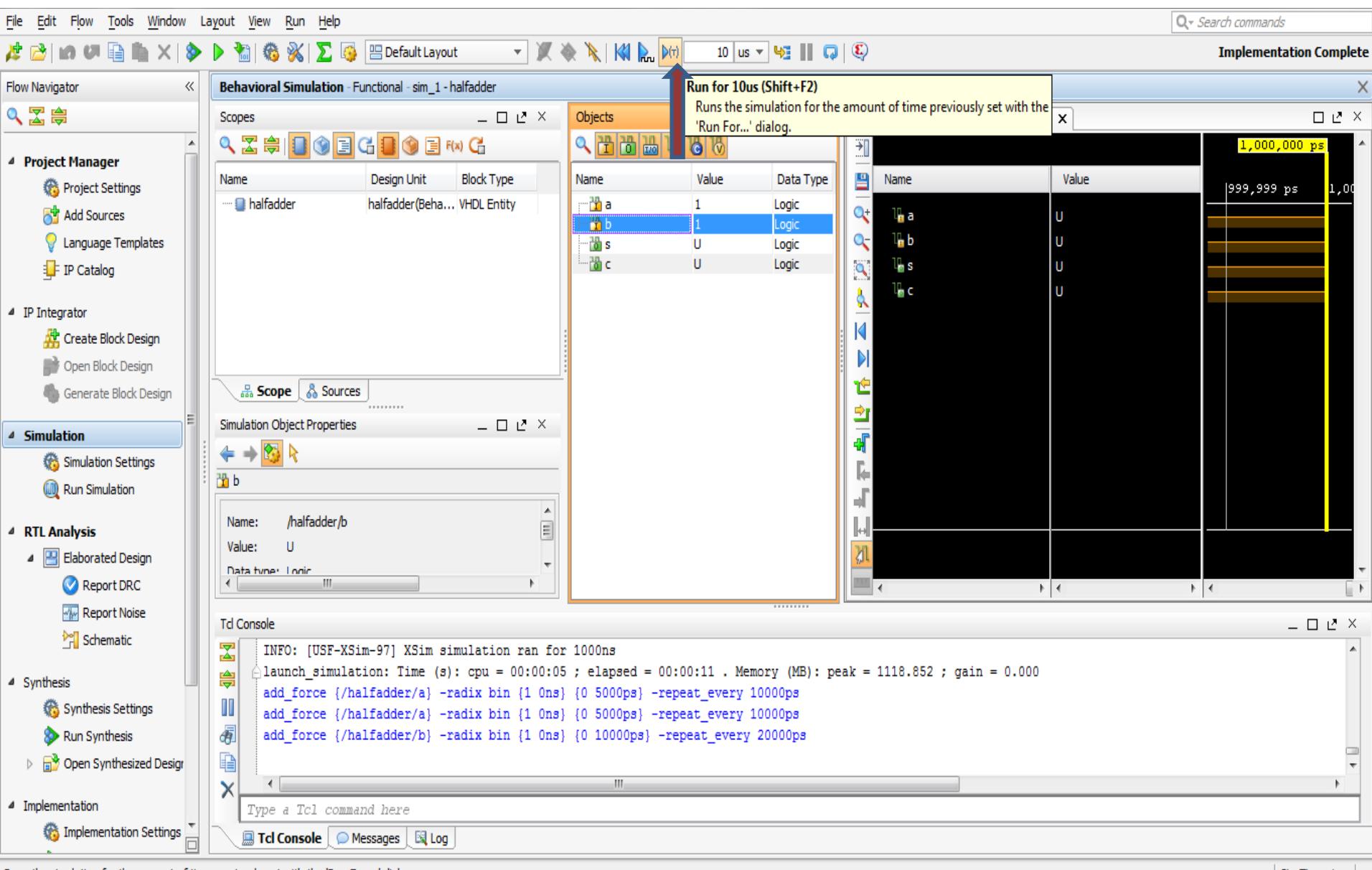
v) Now this window popped up on screen.



## vi) Select Leading and trailing edge values of the corresponding input



## vii) Click on Run for specified time



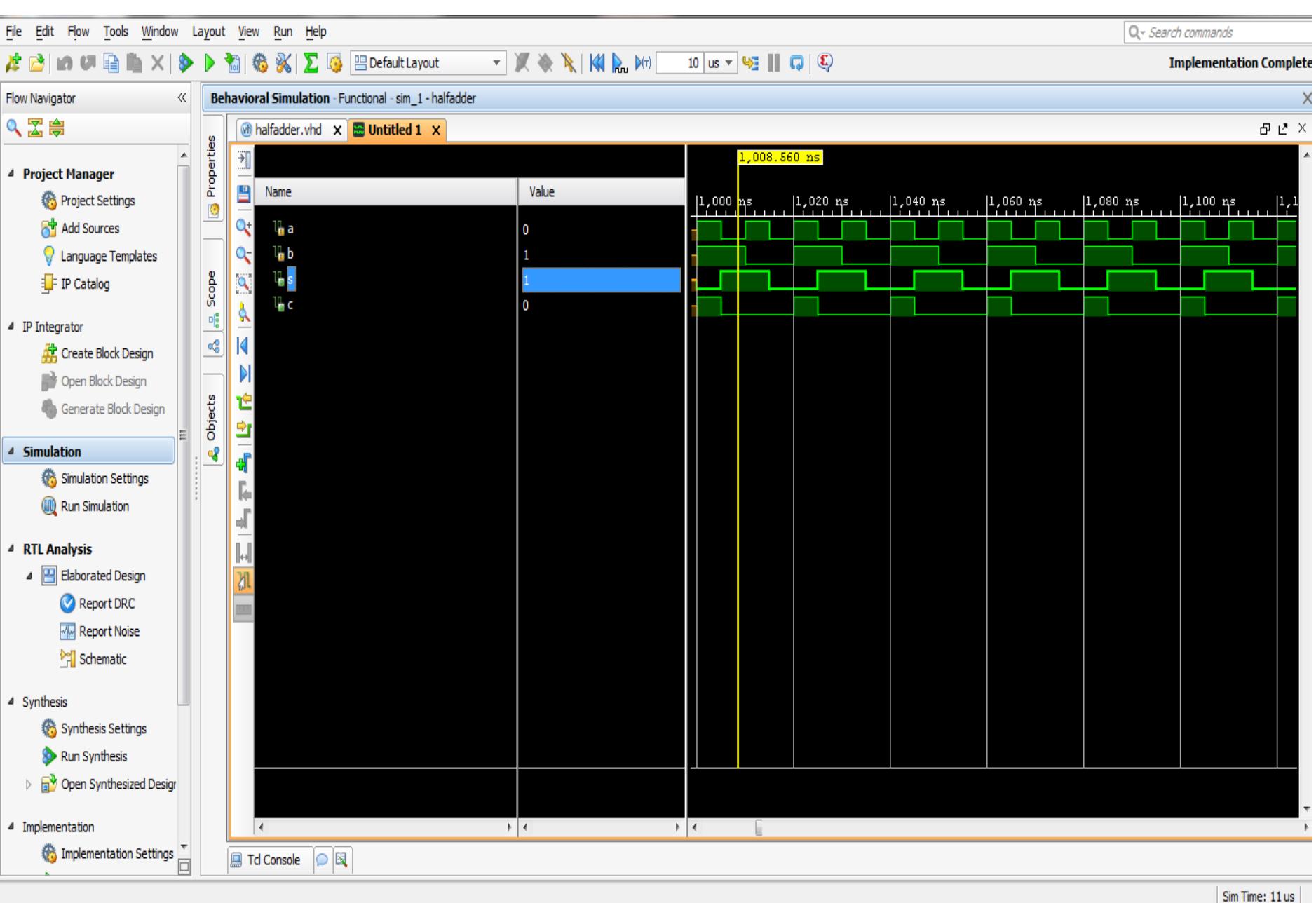
# viii) Now we can see the Results by maximizing the simulator window.

The screenshot shows the Quartus II software interface with the following windows and details:

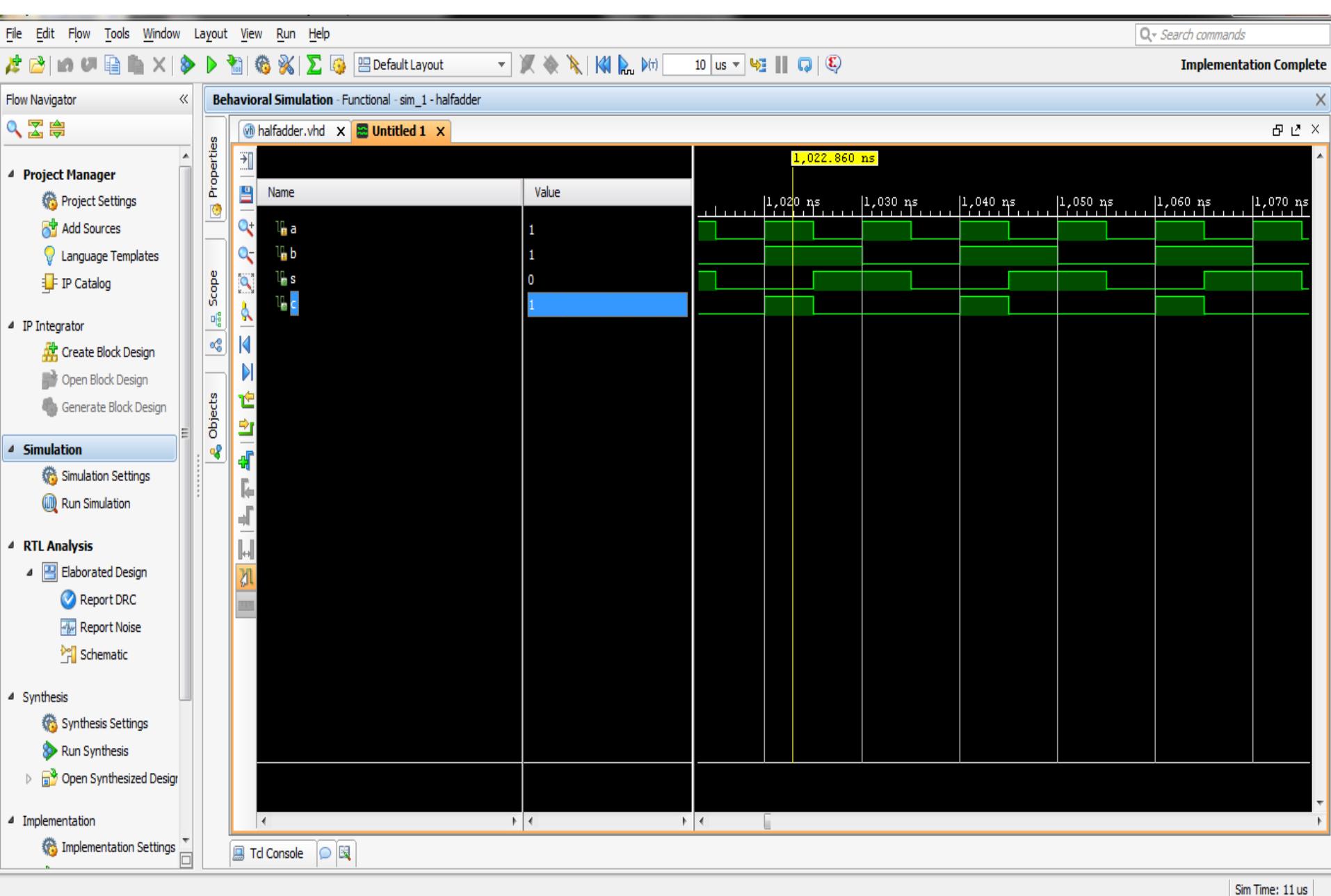
- File**, **Edit**, **Flow**, **Tools**, **Window**, **Layout**, **View**, **Run**, **Help** menu bar.
- Search commands** search bar.
- Implementation Complete** status message.
- Flow Navigator** pane on the left.
- Project Manager** pane:
  - Project Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP Integrator** pane:
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- Simulation** pane (selected):
  - Simulation Settings
  - Run Simulation
- RTL Analysis** pane:
  - Elaborated Design
    - Report DRC (checked)
    - Report Noise
    - Schematic
- Synthesis** pane:
  - Synthesis Settings
  - Run Synthesis
  - Open Synthesized Design
- Implementation** pane:
  - Implementation Settings
- Behavioral Simulation - Functional sim\_1 - halfadder** window:
  - Scopes** pane: Shows the design unit `halfadder` as a behavioral VHDL Entity.
  - Objects** pane: Shows the ports and their initial values: `a` (1), `b` (1), `s` (0), and `c` (1).
  - Scope** tab selected.
  - Simulation Scope Properties** pane: Shows the elaborated design node `/halfadder`.
- halfadder.vhd** and **Untitled 1** tabs in the top right.
- Waveform View**: Shows the simulation results for inputs `a` and `b` and outputs `s` and `c`. The time scale is 11,000,000 ps.
- Tcl Console** window:

```
launch_simulation: Time (s): cpu = 00:00:05 ; elapsed = 00:00:11 . Memory (MB): peak = 1118.852 ; gain = 0.000
add_force {/halfadder/a} -radix bin {1 Ons} {0 5000ps} -repeat_every 10000ps
add_force {/halfadder/a} -radix bin {1 Ons} {0 5000ps} -repeat_every 10000ps
add_force {/halfadder/b} -radix bin {1 Ons} {0 10000ps} -repeat_every 20000ps
run 10 us
```
- Type a Tcl command here** input field.
- Tcl Console**, **Messages**, and **Log** tabs at the bottom.
- Sim Time: 11 us** status message at the bottom right.

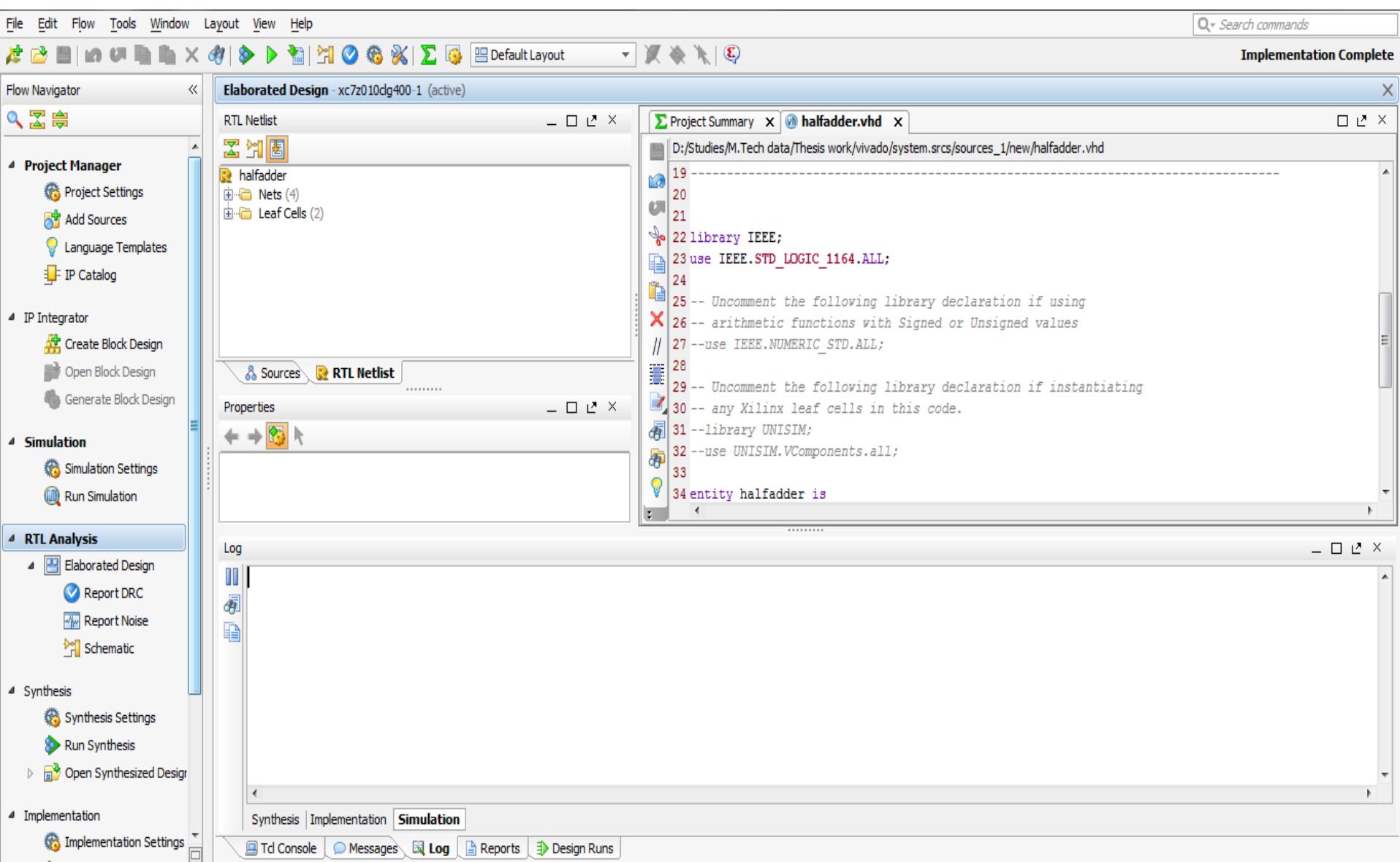
# ix) Output of one case having a=0,b=1.



# ix) Output of another case having a=1,b=1.

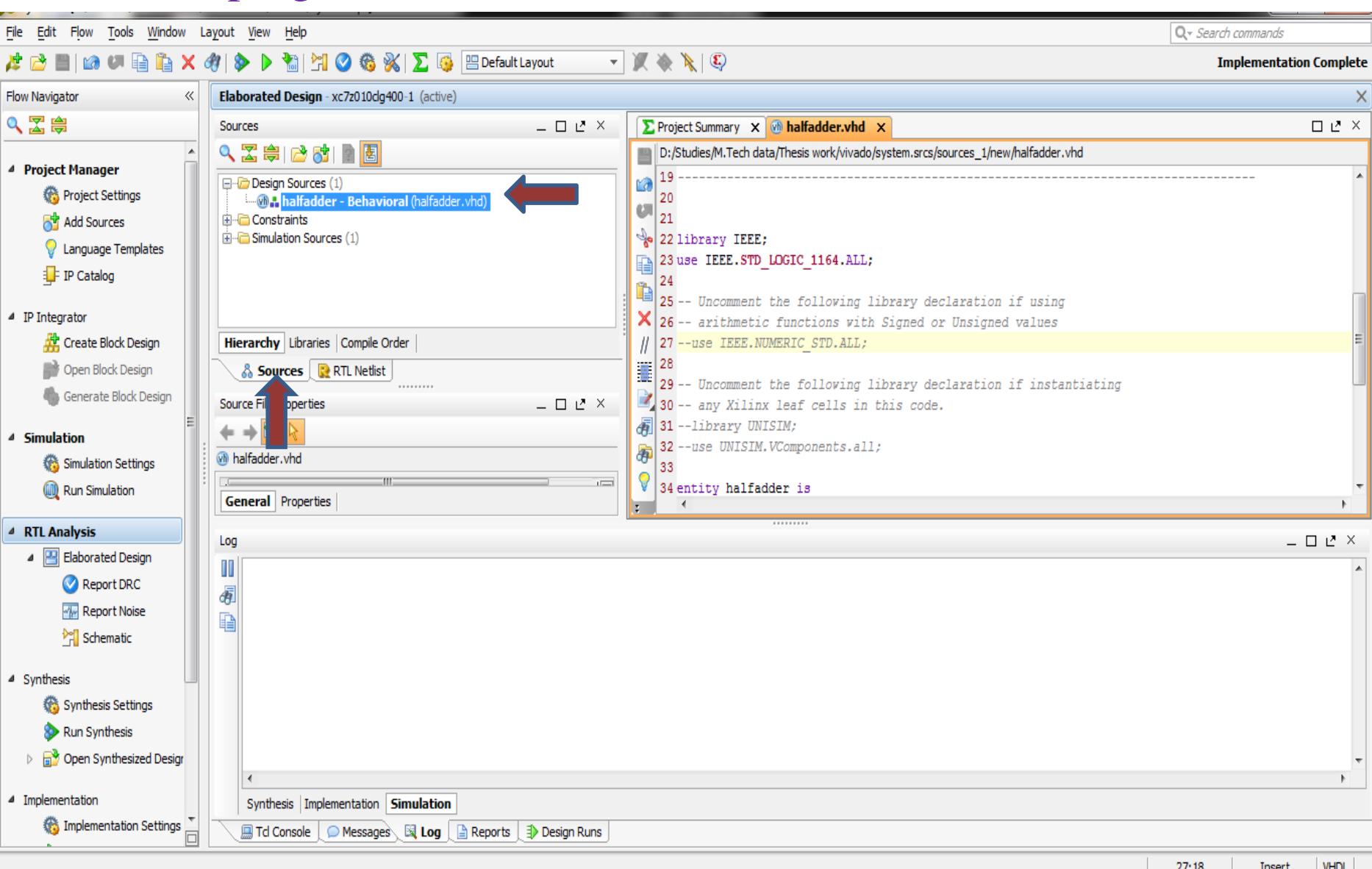


x) Now click on elaborated design then this window popped up on the screen

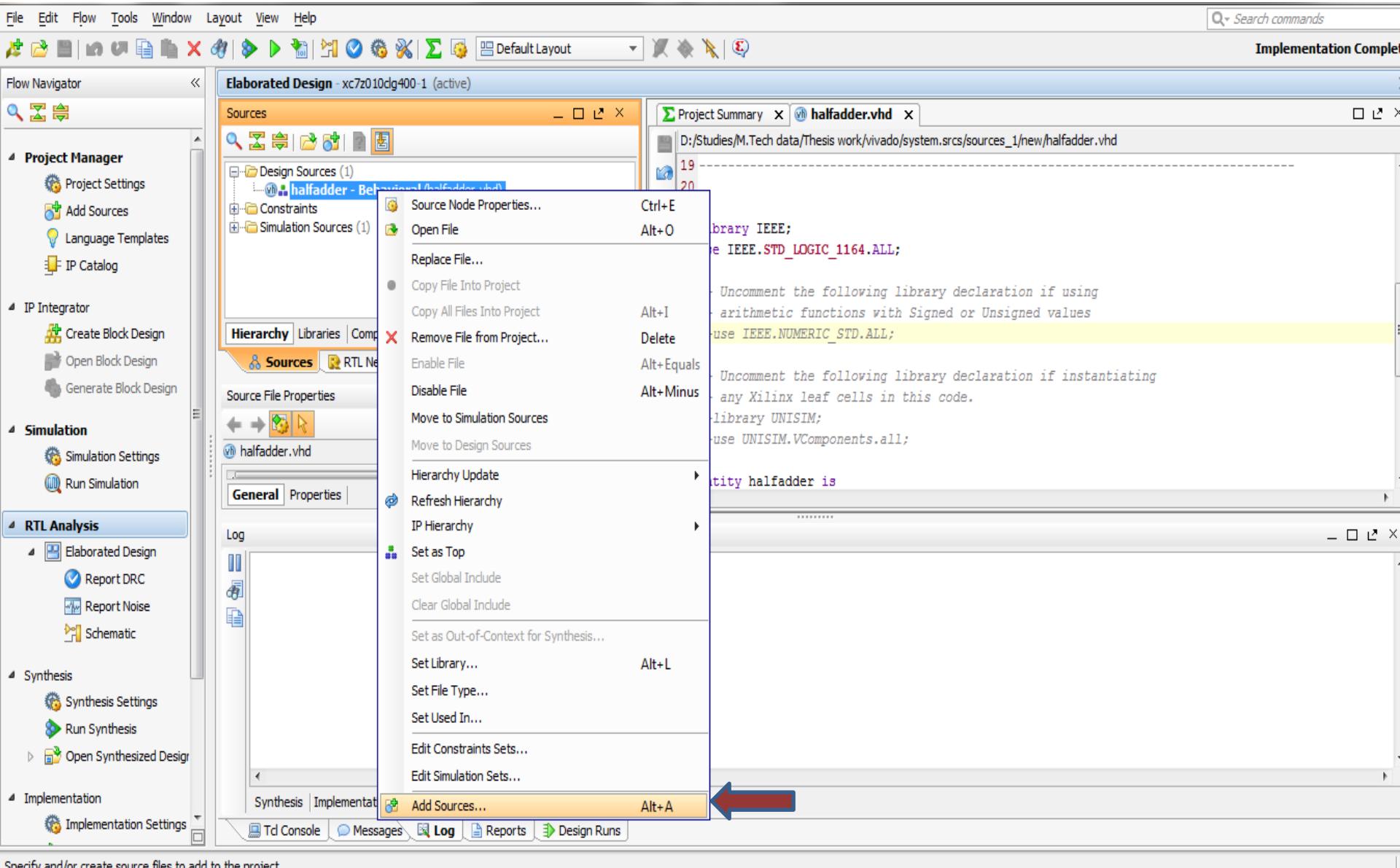


### 3. Run Simulation with Test Bench

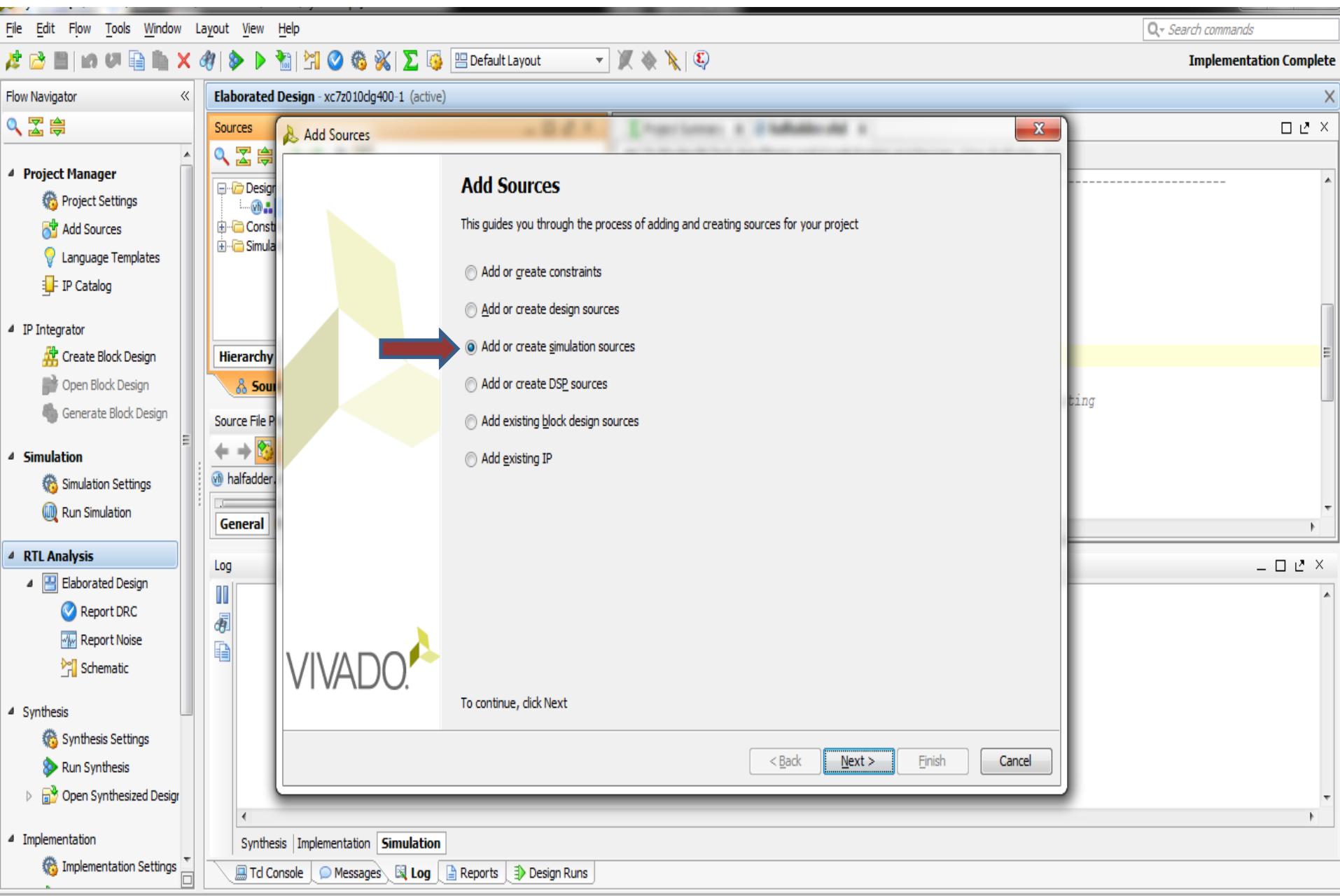
- i) Click on Sources and select the file name on which file we had written the program.



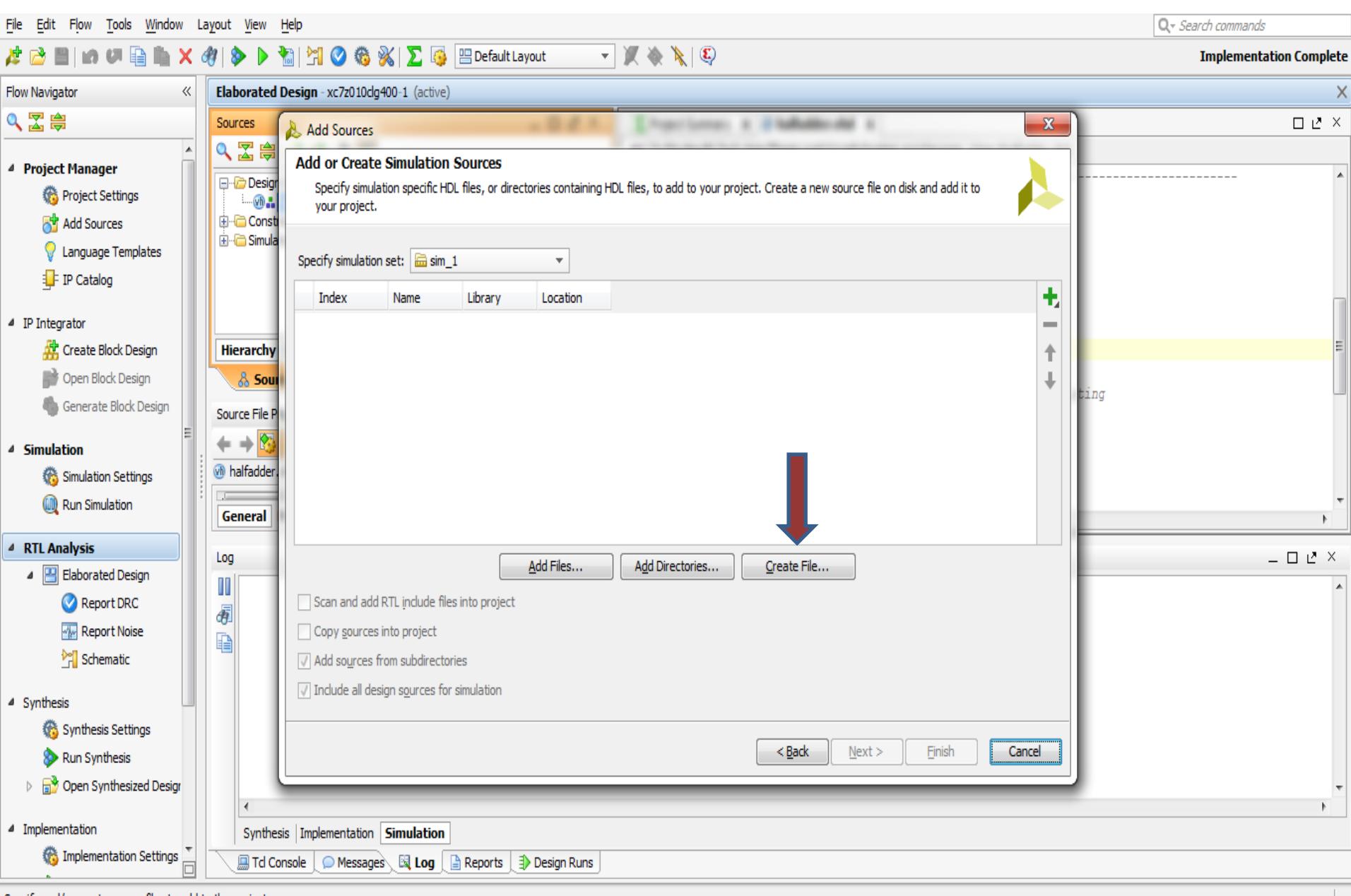
## ii) Right Click on file name and the select add sources.



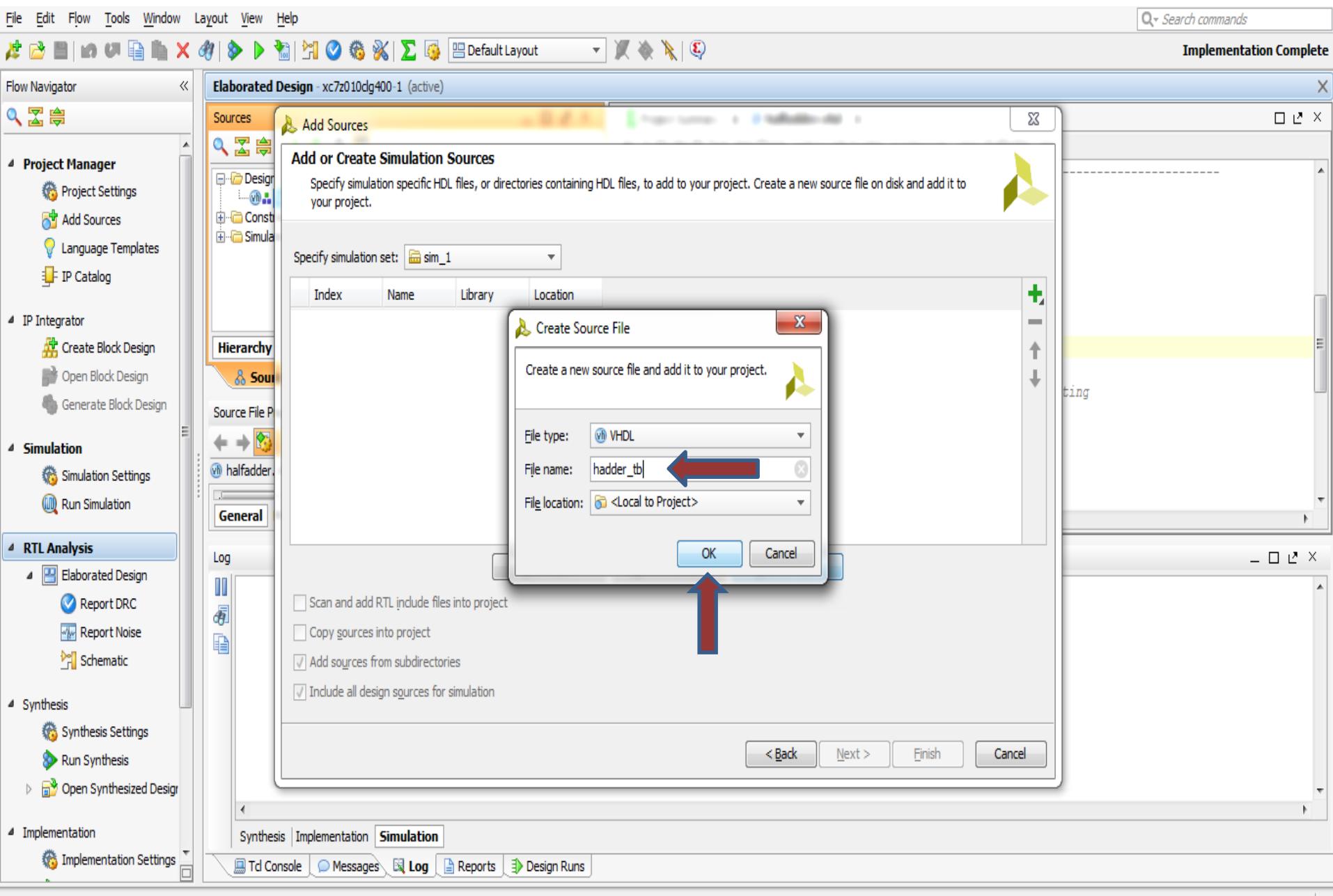
### iii) Select the add or create simulation sources.



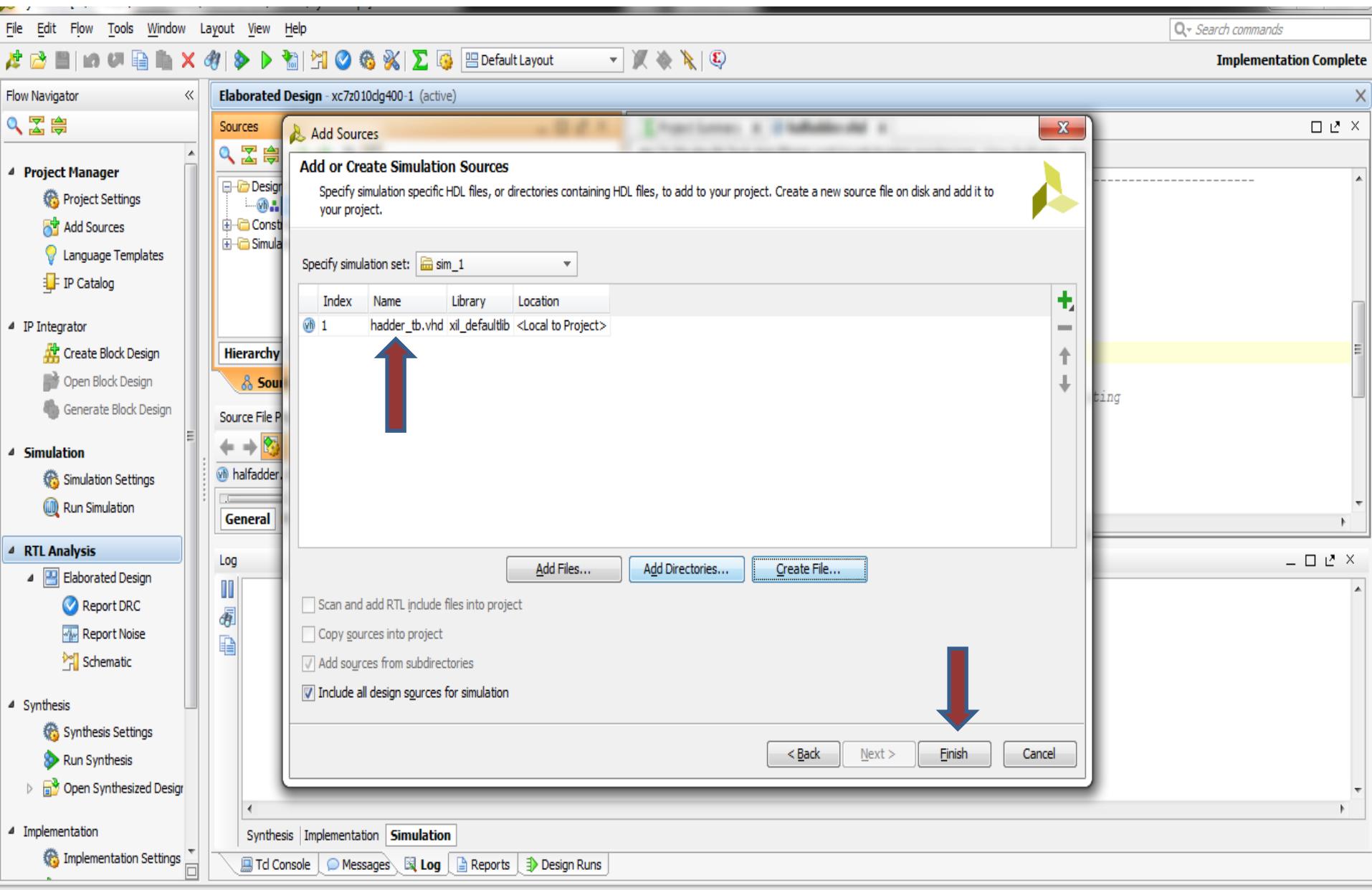
#### iv) Click on Create file option.



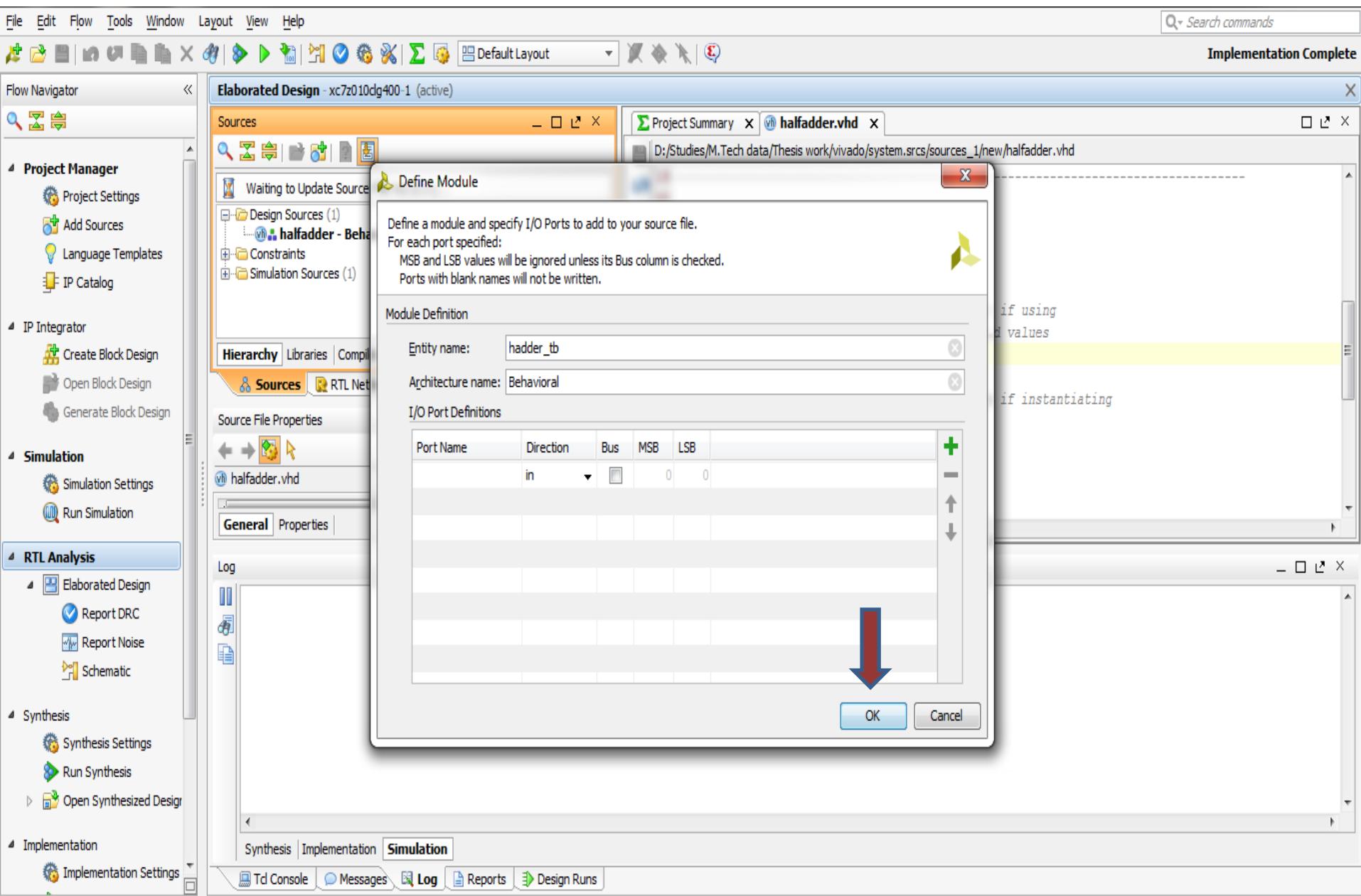
v) Specify the file name and then click on ok.



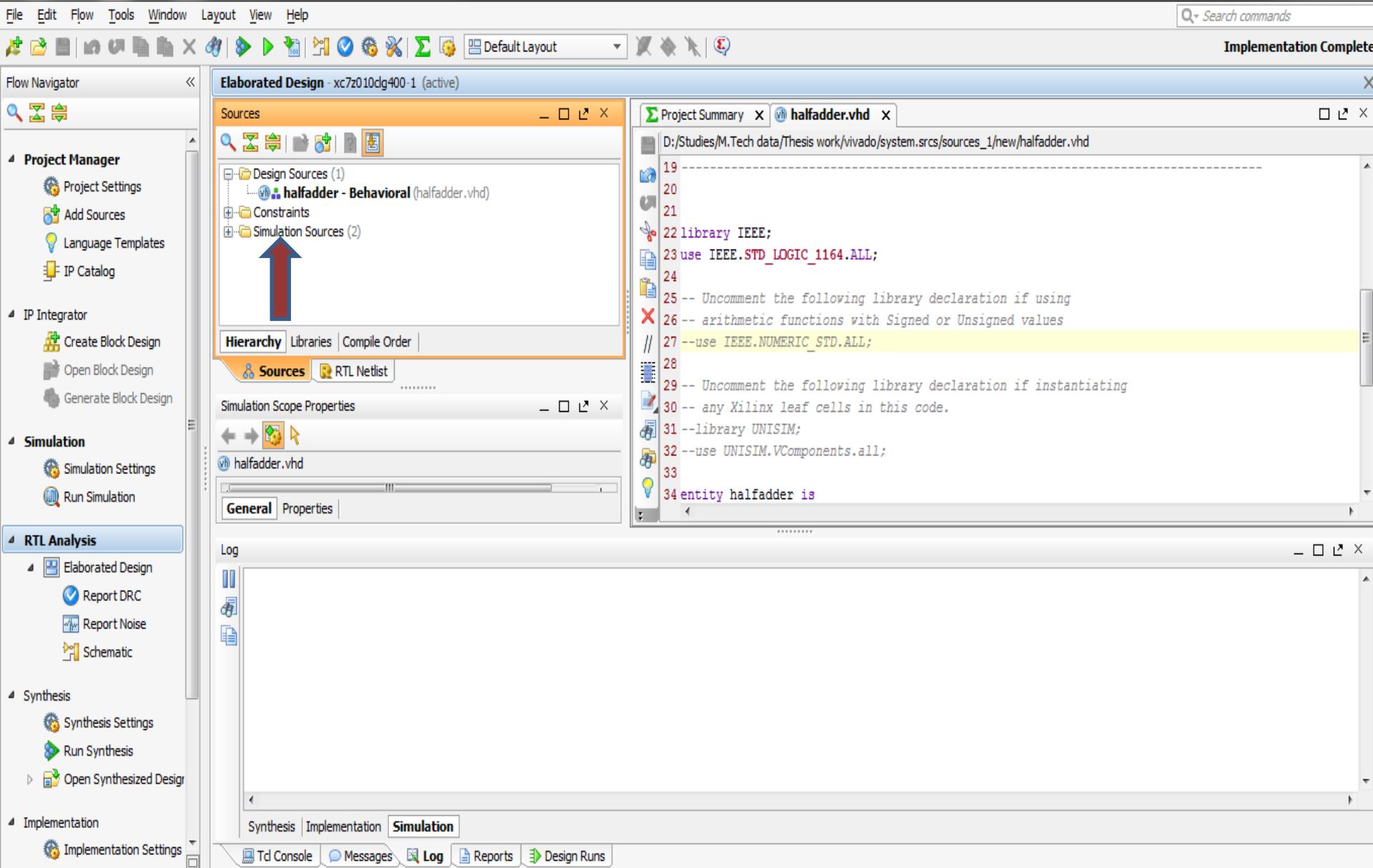
vi) Then it shows the testbench file name and then click on finish.



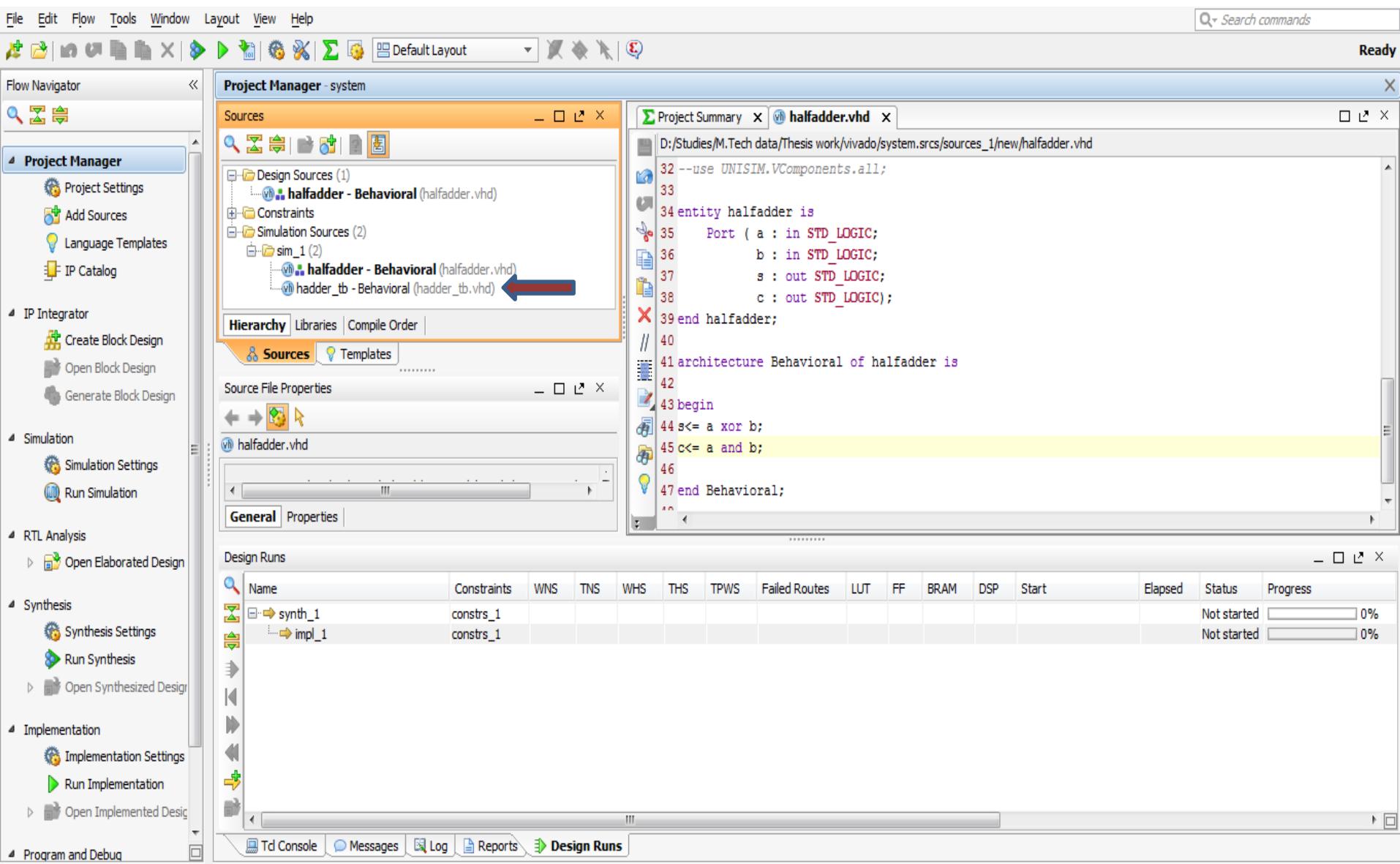
vii) Click on Ok



### viii) Click on simulation sources.



ix) Then we can see the testbench file double click on it then it will open.



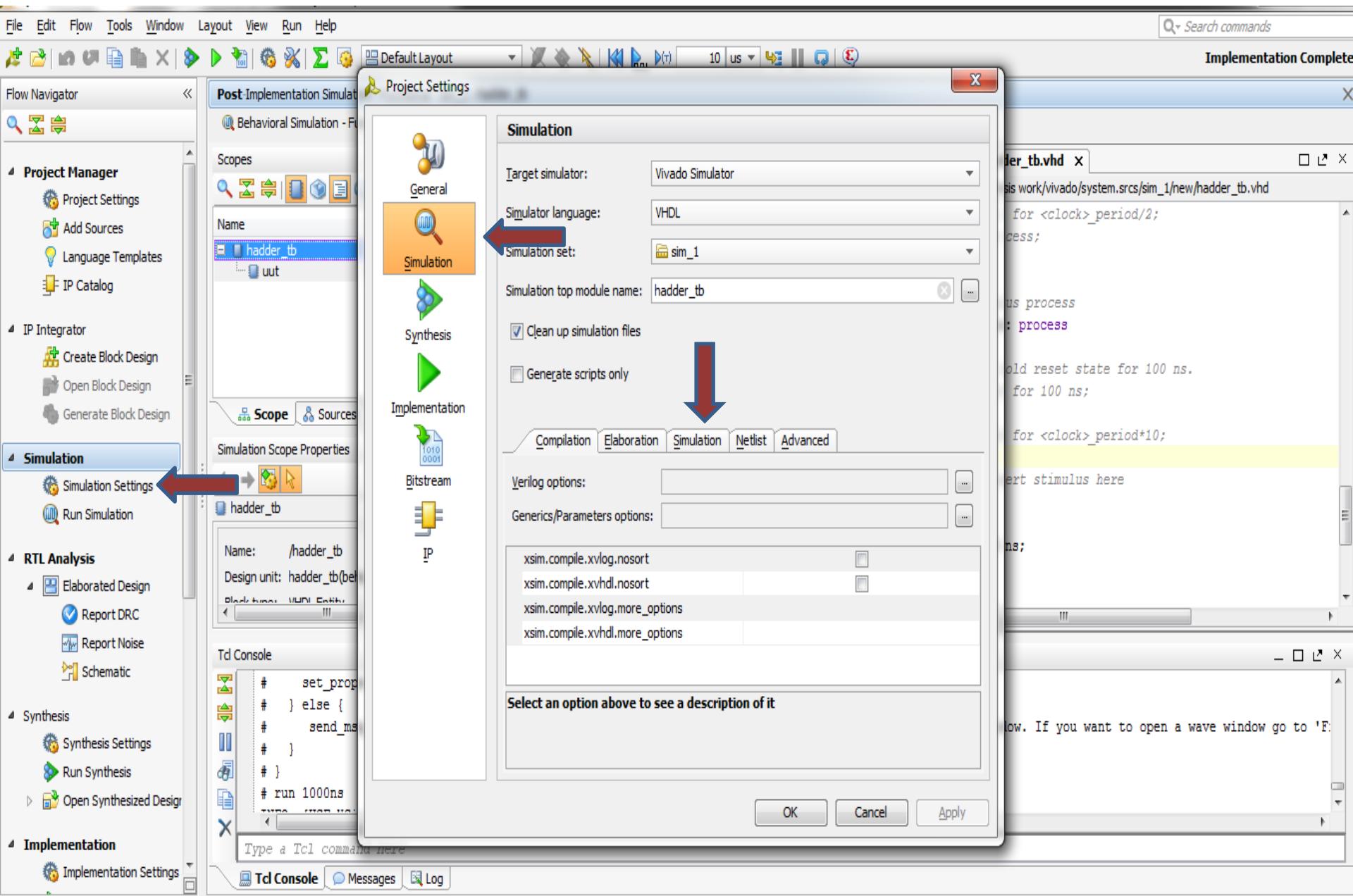
x) Test cases which are applied to that circuit had shown below and after once written test cases save it.

The screenshot shows the Vivado IDE's Project Manager window. The left sidebar contains navigation links for Flow Navigator, Project Manager, IP Integrator, Simulation, RTL Analysis, Synthesis, Implementation, and Program and Debug. The main area displays the 'Project Manager - system' window with tabs for Project Summary, halfadder.vhd, and hadder\_tb.vhd. The 'Sources' tab is selected, showing the file path D:/Studies/M.Tech data/Thesis work/vivado/system.srcs/sim\_1/new/hadder\_tb.vhd. The code editor displays the following VHDL script:

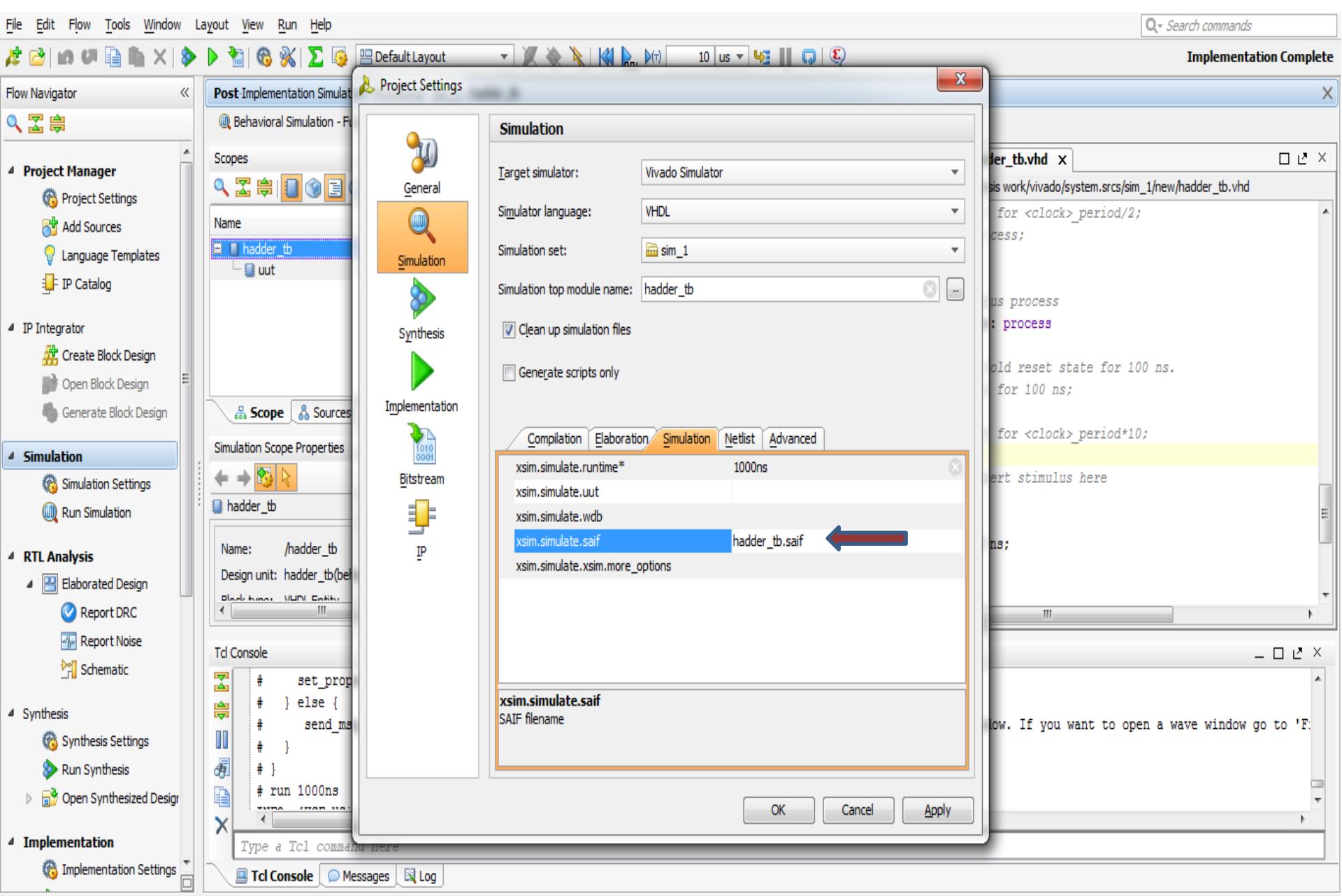
```
79 --      <clock> <= '1';
80 --      wait for <clock>_period/2;
81 --      end process;
82 --
83
84 -- Stimulus process
85 stim_proc: process
86 begin
//      -- hold reset state for 100 ns.
88 --      wait for 100 ns;
89 --
90 --      wait for <clock>_period*10;
91
92 -- insert stimulus here
93 a<='1';
94 b<='1';
95 wait for 10 ns;
96 a<='0';
97 b<='1';
98 wait for 10 ns;
99 a<='1';
100 b<='0';
101 wait for 10 ns;
102 a<='0';
103 b<='0';
104 wait for 10 ns;
105 end process;
106
107 END;
```

A blue bracket highlights the stimulus insertion section from line 93 to line 104. A callout box with a blue border and arrow points to this highlighted area with the text: "These are the test cases which we applied to half adder".

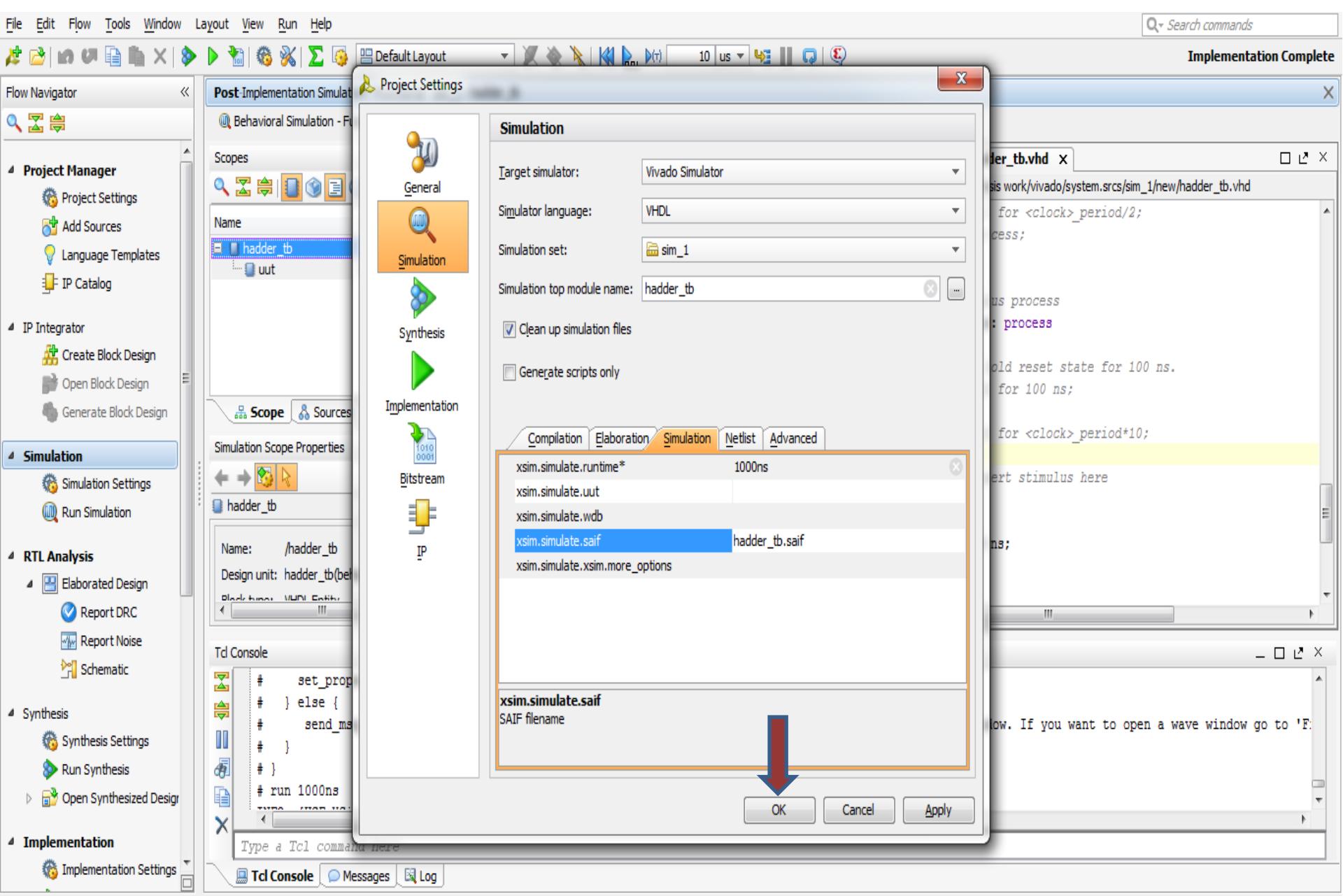
xi) Click on Simulation settings and then select simulation.



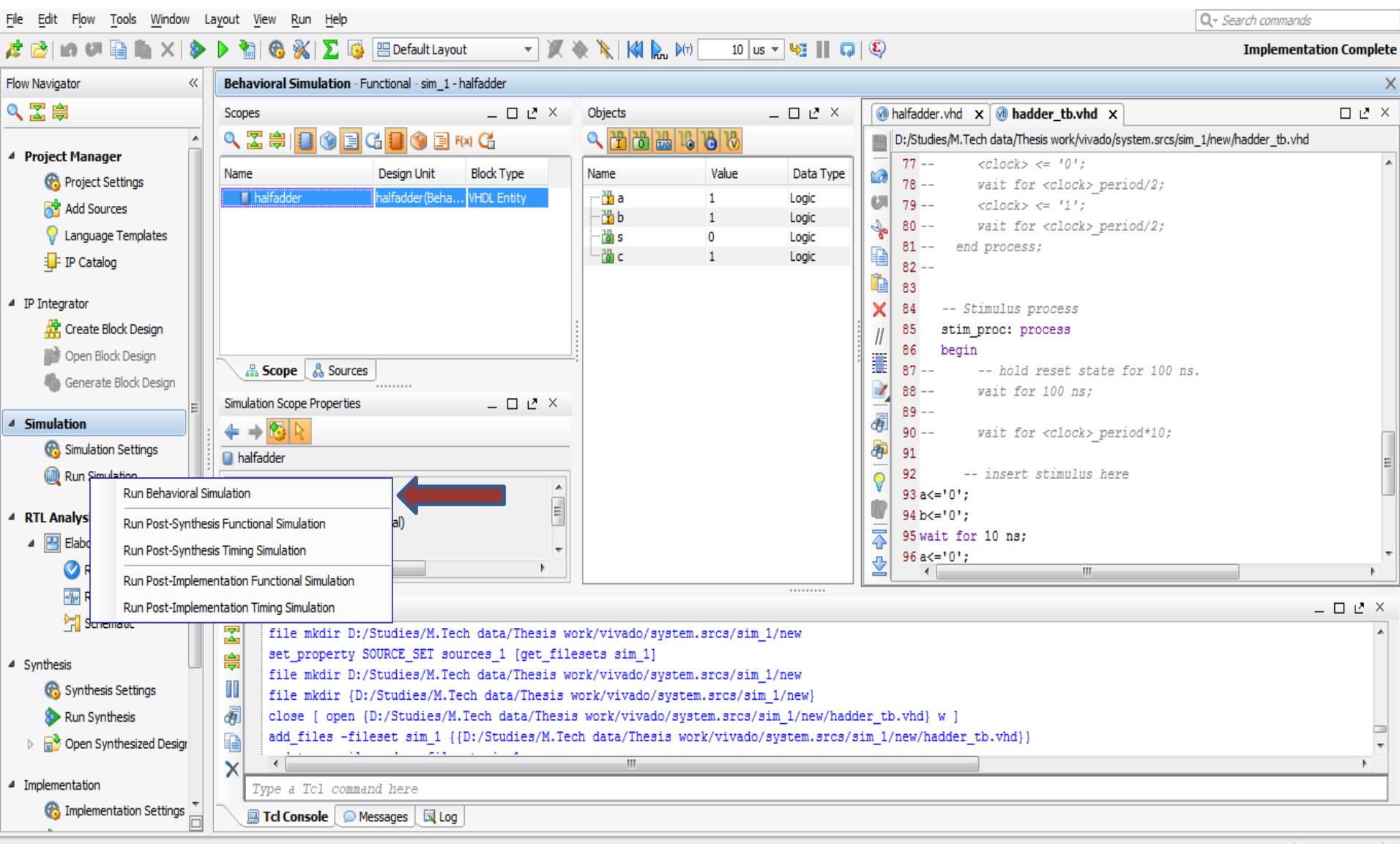
xii) Select the below shown row and specify the file name extension of .saif



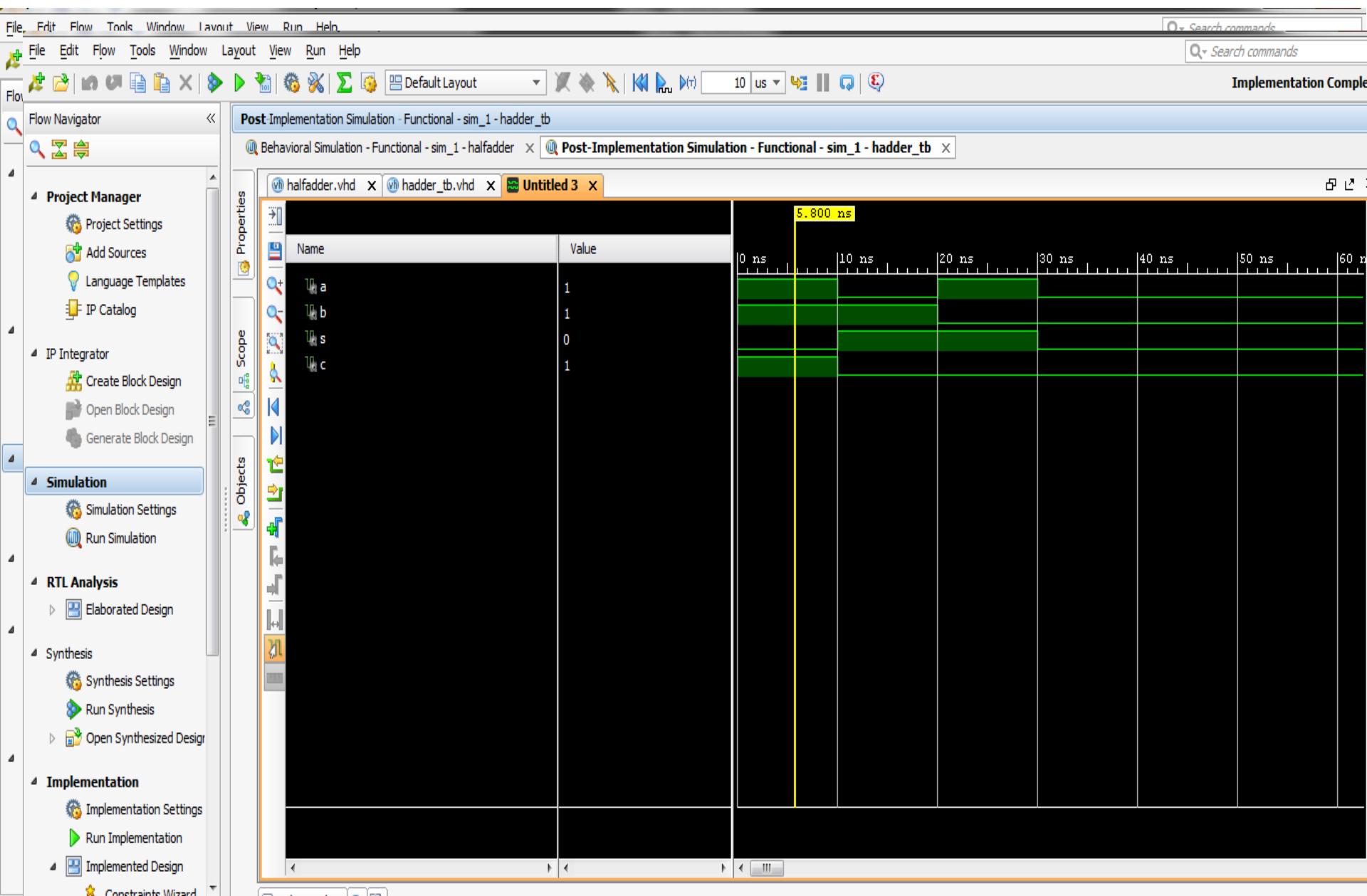
### xiii) After file name is specified, Click on ok



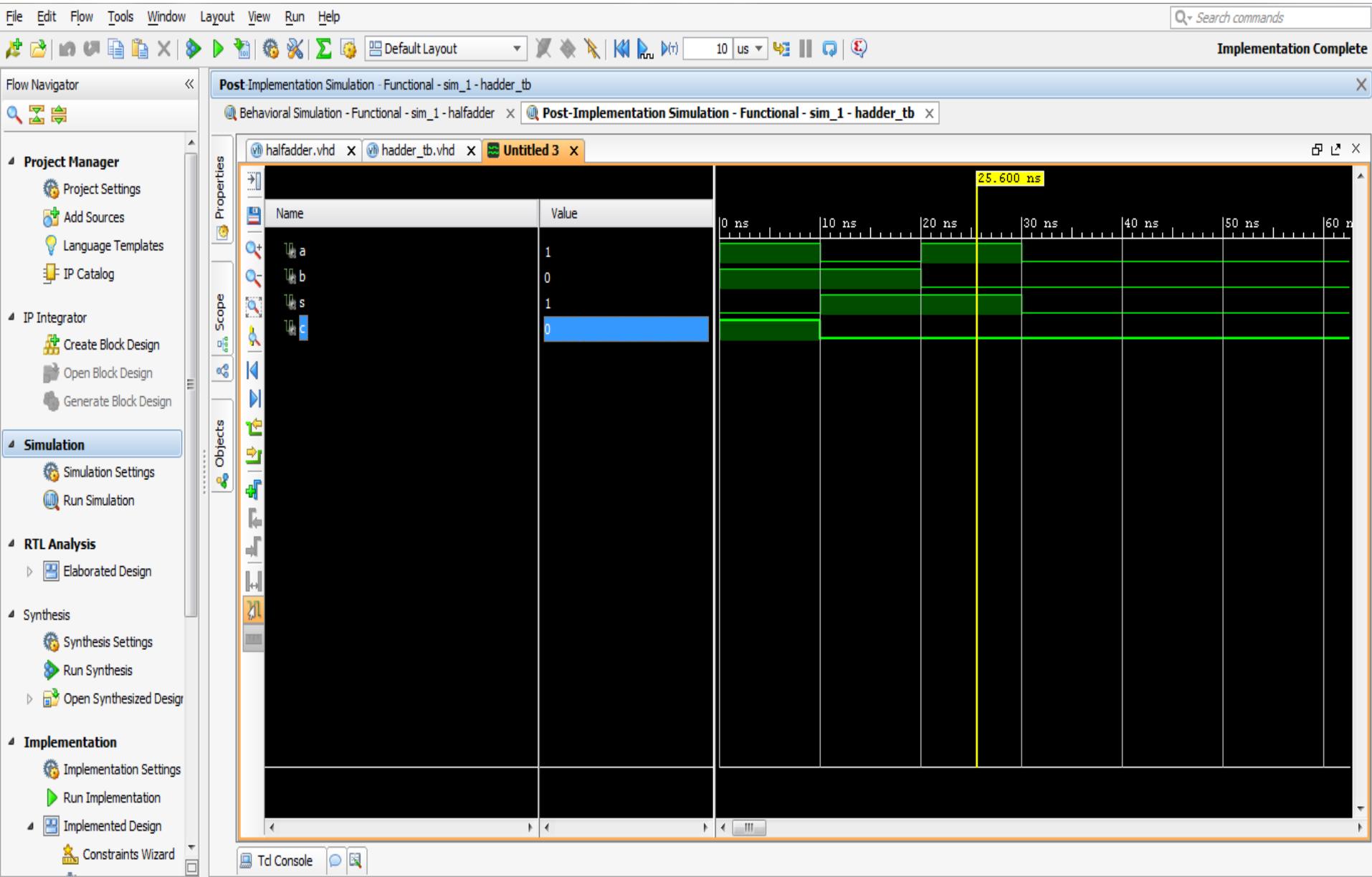
#### xiv) Click on Run simulation and then Select the run Behavioral simulation



xv) Once after did that it shows the output like below.

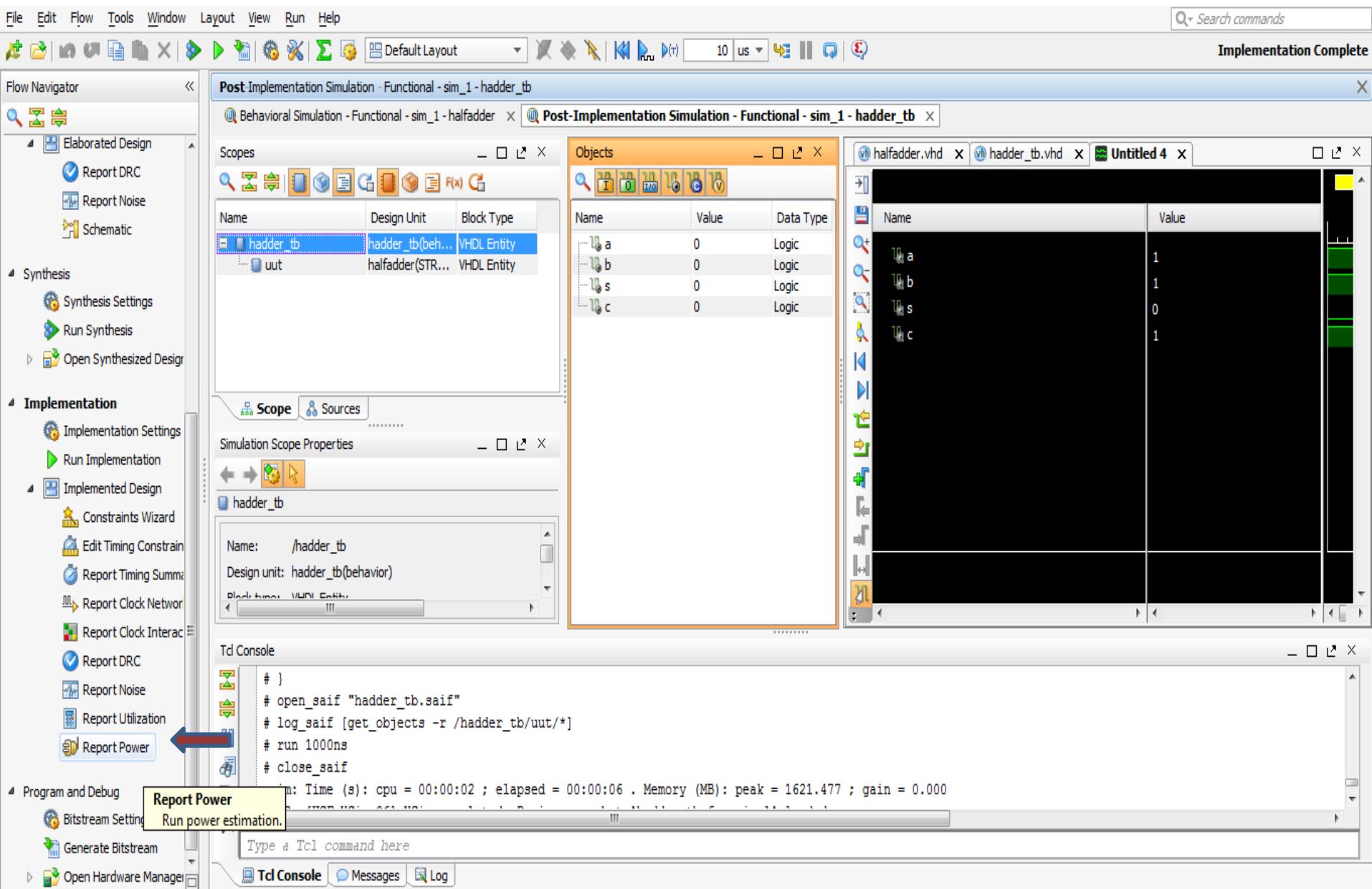


# xvi) Output for another test case.

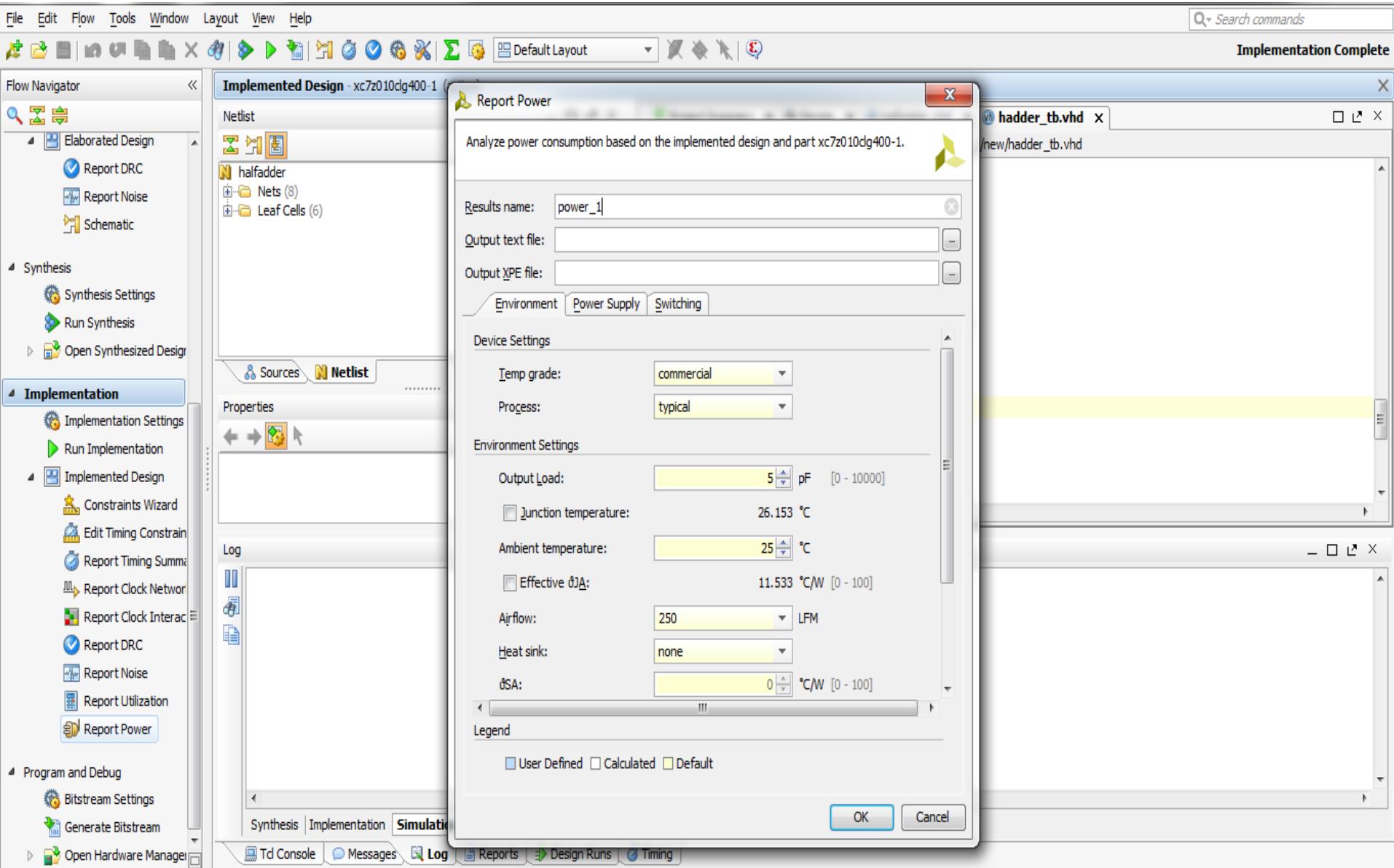


# 4. Power Calculation

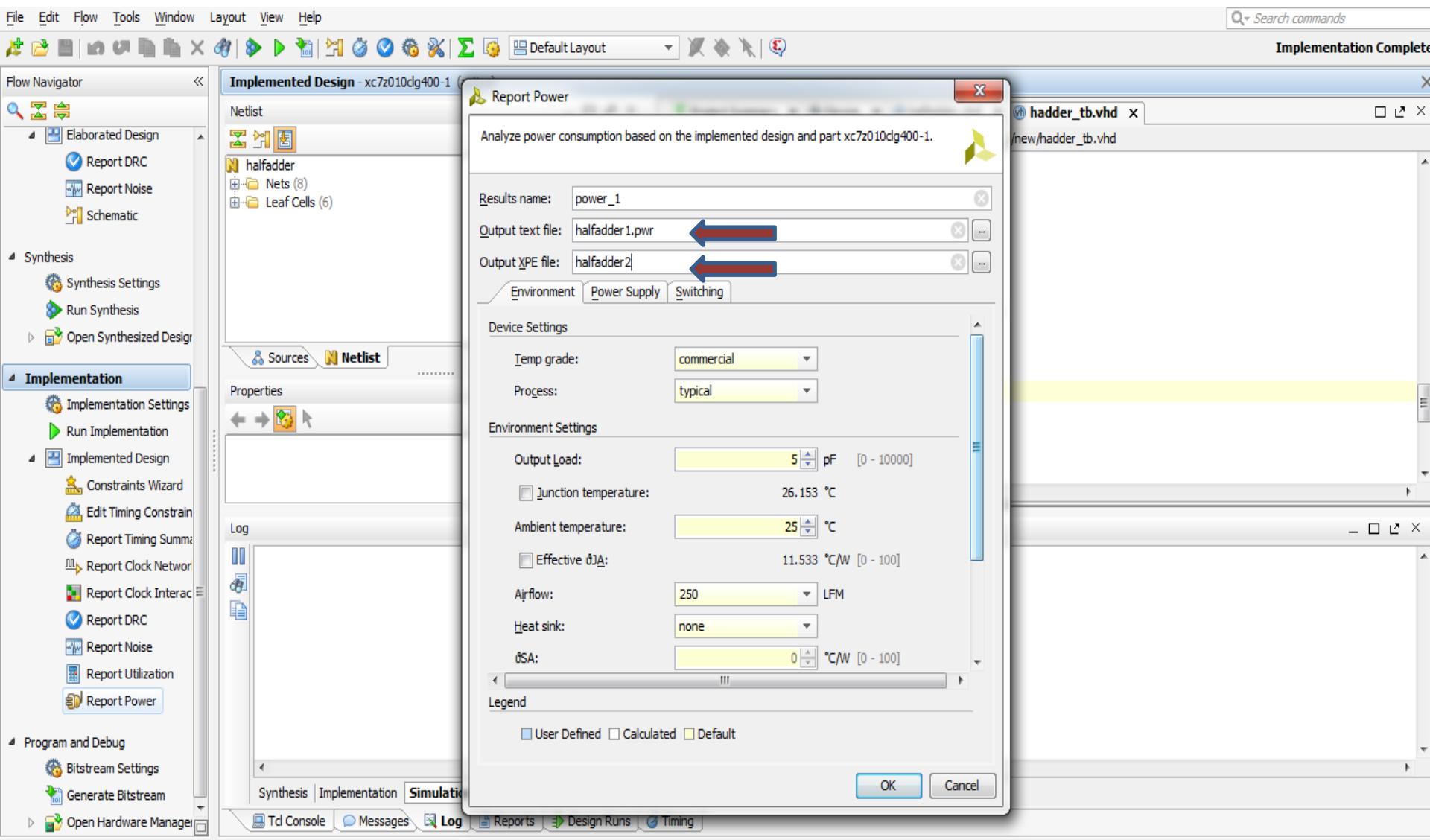
i) Click on Implemented design and then click on Report Power.



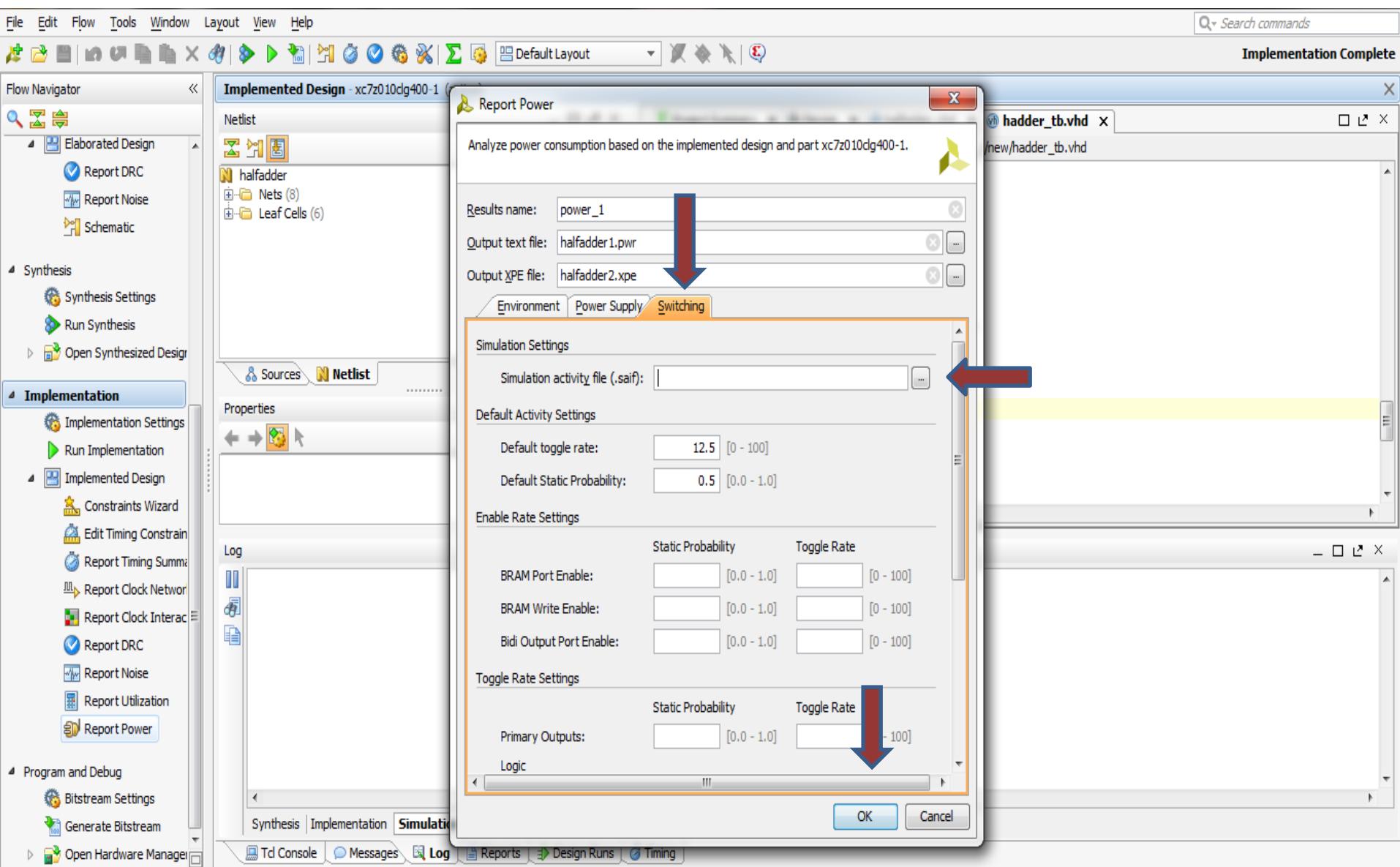
## ii) Now this popped up on the screen



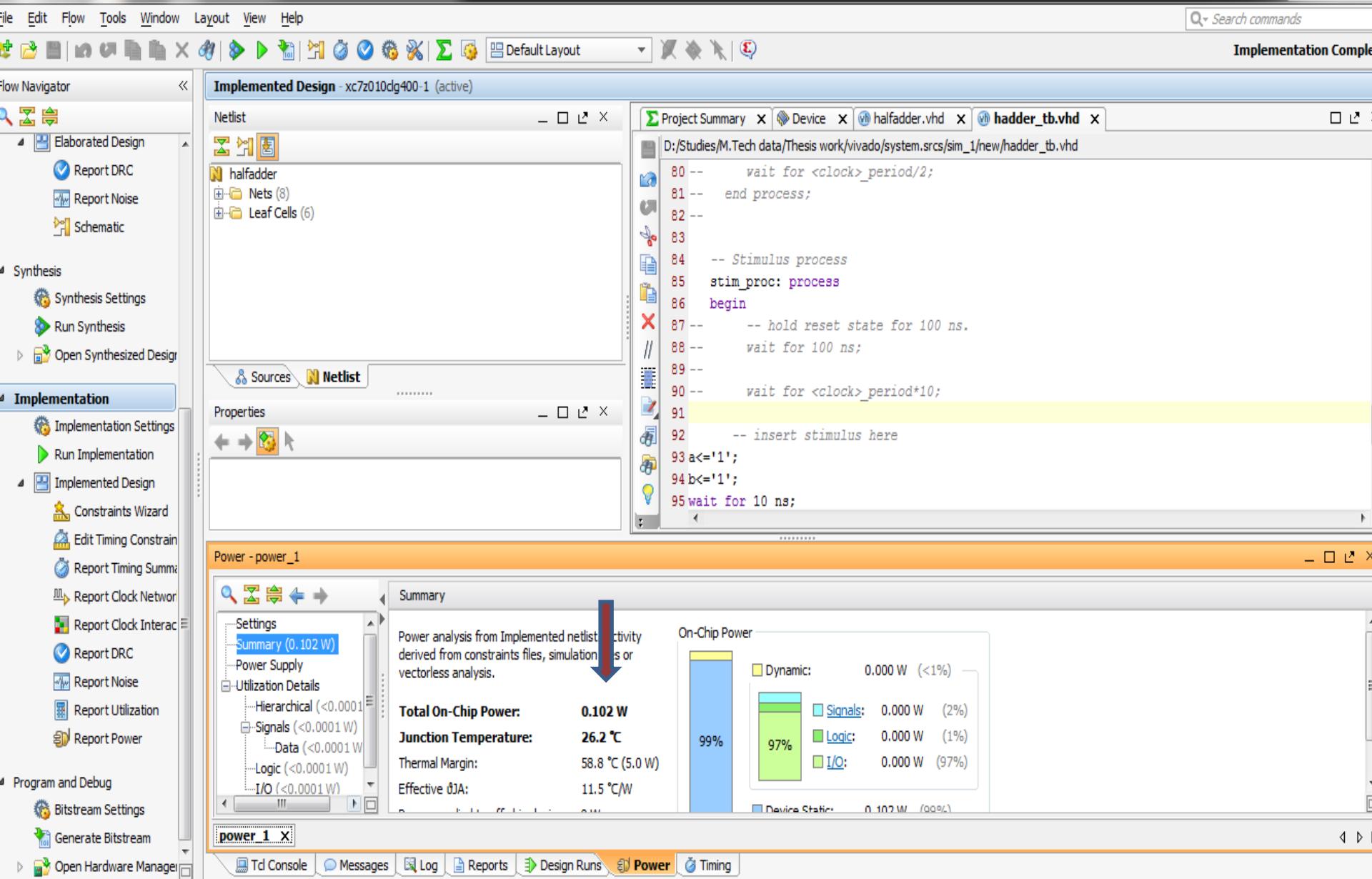
### iii) Specify the output test file and output XPE file.



iv) Select the Switching tab and then specify the path to .saif file and then click on ok.



v) Then window popped up like this and it shows Dynamic power like below.





Thank you

