Digital Circuits and System Lab

Semester: ODD

LIST OF EXPERIMENTS

S.No.	AIM OF EXPERIMENTS
1.	Design, simulate and implement Half adder, Full adder using dataflow, behavioral and structural modeling in VHDL
2.	Realize the function, mentioned below in at least four different physical ways: F(x) = x0 + x1 + x2 + x3 + x4 + x5 + x6 + x7 + x8 + x9
3.	Implementation of 2x1, 4x1 and 8x1 multiplexers using dataflow, behavioral and structural modeling in VHDL.
4.	Implement 4 bit ripple carry adder using structural modeling. Implement 4 bit adder/subtractor using structural modeling.
5.	Implement 1 to 2, 2 to 4 and 3 to 8 line decoder using dataflow, behavioral and mixed modeling in VHDL. Implement Booleans functions using decoders
6.	Design of D latch, JK FF, SR FF,T FF using Behavioral and Structural modelling
7.	Shift Register design using VHDL
8.	Sequential system design using state Machines
9.	Counters and its applications
10.	Traffic Light Controller using state Machines