EXPERIMENT No. 01

A. Aim: In this experiment we will get acquainted with basic electrical and electronic tools/components like breadboard, CRO, power supply, resistor etc. We will use these tools to test a simple voltage divider circuit for a DC and AC voltage input.

B. Apparatus Used: 1. DSO, DC Power supply, multimeter, breadboard.
2. Resistors R1, R2, R3, R4, (….KΩ), Potentiometer VR (….KΩ)

C. Theory: In electronics, we deal with electricity which is produced by the movement of electrons from one point to another between two different voltage sources. By controlling the flow of electrons, we can control the voltage and current at any node (point) along the circuit.

The resistor is an essential component that is used for this purpose. Its basic function is to oppose the flow of charge through it. With the help of *Ohm's law*, the value of output current can be calculated easily. By connecting two or more resistances in series, voltage can be reduced to a desired value at any given point along the circuit.

Resistor:-
Resistors are usually classified according to the following three properties:
i. Composition (e.g. carbon granule, carbon film, wire wound etc.)
ii. Power rating (e.g. 1/8 W, 1/4 W etc.)
iii. Tolerance (e.g. No Color-20 %,Silver-10%,Gold-5%,Brown-1%,Red-2% etc.)

Each resistor has two main characteristics:
1. Its resistance value in ohms

2. Its power dissipating capacity in watts

Power ratings are obtained from the manufacturer's specification sheet.
Tolerance is usually indicated on the resistor itself along with the value of the resistance.

The resistance value and the tolerance, unless printed on the resistor, are decoded by printed colored bands. The 1st and 2nd band represents the significant digits and the 3rd band represents the number of zeros to the right of the two significant digits. The ten colors denoting the 0-9 are the following black (0), brown (1), red (2), orange (3), yellow (4), green (5), blue (6), violet (7), grey (8), white (9). The 4th band indicates the tolerance. A golden band indicates a tolerance of 5% and a silver band indicates a tolerance of 10%. Absence of the 4th band implies a tolerance of 20%. A brown band indicates 1% tolerance.

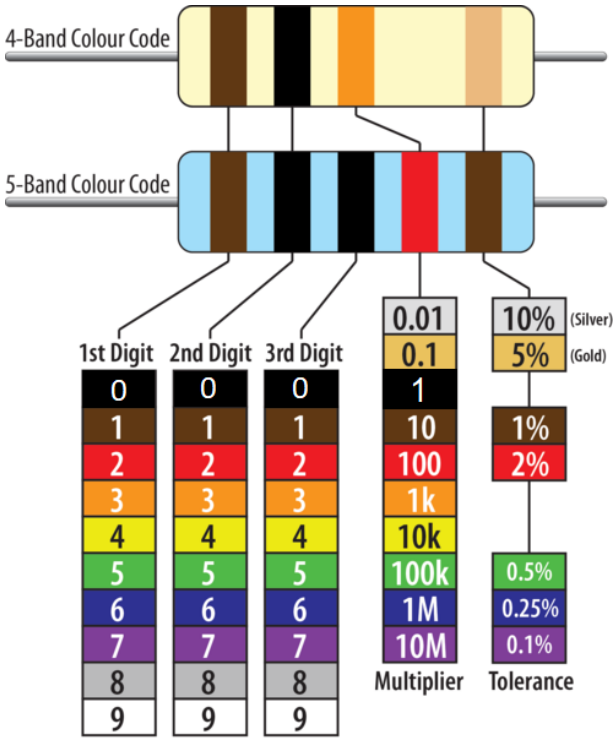
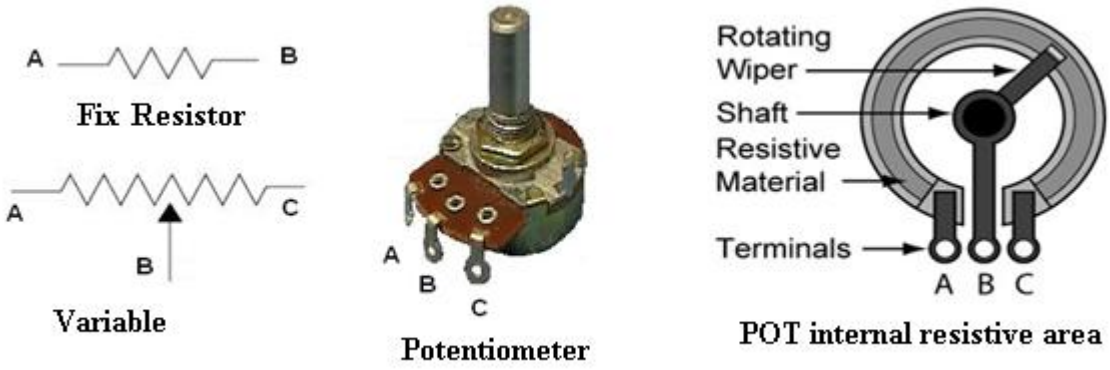


Image credit:
http://cdn.shopify.com/s/files/1/0045/8932/files/ResistorColourCodes_grande.png
Note: This is a color image.

Potentiometer:-



A potentiometer is a three-terminal resistor with a moving contact (by sliding or rotating). It is essentially a voltage divider and commonly used in the rotary volume controls of audio devices.

Definitions:-

Component: - A device with two or more terminals into which, or out of which, charge may flow.
Node: - A point at which terminals of more than two components are joined. A conductor with a substantially zero resistance is considered to be a node for the purpose of analysis.

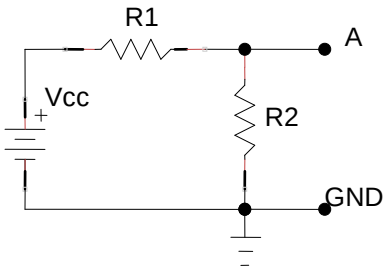
Branch: - The collection of one or more components between two adjacent nodes.

Mesh: - A group of branches within a network joined so as to form a complete loop.

Circuit: - An electronic circuit is composed of individual electronic components, such as resistors, transistors, capacitors, inductors and diodes, connected by conductive wires or traces through which electric current can flow. The combination of components and wires allows various simple and complex operations to be performed: signals can be amplified, computations can be performed, and data can be moved from one place to another.

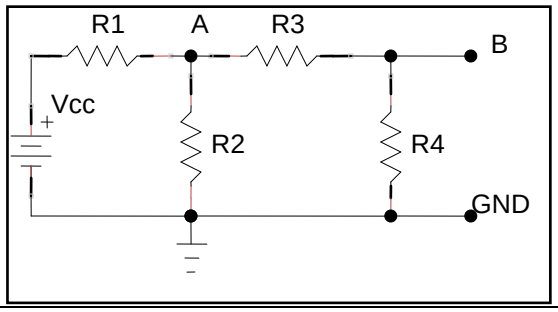
D. Exercises:

Figure 1.1



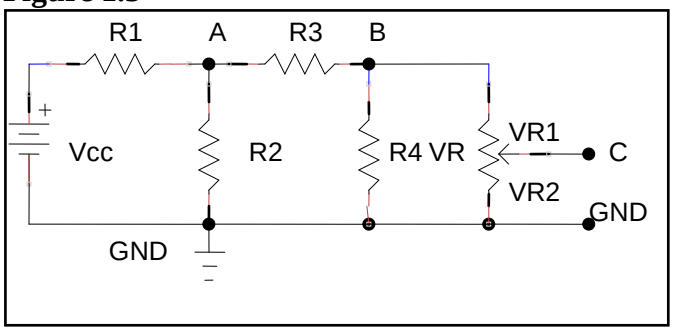
Exercise 1.1: Calculate and measure the value of voltage between A and GND.

Figure 1.2



Exercise 1.2: Calculate and also measure the value of the voltage at B.

Figure 1.3



Exercise 1.3: Given a potentiometer as shown in the circuit diagram, measure its value to get (select any voltage Vc)
$\mathbf{V_C}$ = +..... **V**
and find the values of VR1 and VR2.

Repeat exercises 1.1, 1.2 and 1.3 for an AC voltage input of 12 Vrms.

Repeat all the exercises for a total of three values of Vc.

E. Procedure:

Exercise 1.1:- Connect two resistors (R1 & R2) back to back on a breadboard and + 12 Volt across R1 and R2, as given in figure 1.1. Connect the CRO probe for voltage measurement.

Exercise 1.2:- Connect R3 and R4 as given in figure 1.2, connect the CRO probe as required for voltage measurement.

Exercise 1.3:- Connect POT (Potentiometer/Variable resistor, VR) as given in figure 1.3 and rotate the shaft to adjust the resistance of POT to obtain predetermined voltage.

F. **Observations**: *(Fill the tables below with your observations)*

	For DC input Voltage			**For AC input Voltage**		
Parameter (Volts)	Calculated value (Volts)	Measured value (Volts)	Error	Calculated value(Volts)	Measured value(Volts)	Error
V_A						
V_B						
V_C						
VR1 (Variable Resistance1)						
VR2 (Variable Resistance2)						

G. Analysis of Results:

(Include sample calculations/Display/plot/typical graph)

H. Conclusions: *This laboratory exercise helps us to understand:*

- ○ Designing and implementing a circuit using circuit elements/components.
- ○ Ohm's law.
- ○ Voltage divider circuit, resistance in series and parallel connection.
- ○ Using and analyzing a potentiometer.
- ○ Voltage and current measurement with CRO.

Precautions:

1. Always connect Vcc to positive rail and GND to the negative rail in the breadboard.
2. Do not short the positive and negative terminals.
3. The observation should be taken properly.
4. Do not try to sabotage the equipment by pressing or rotating unknown buttons.

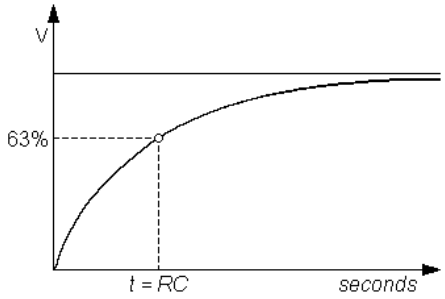
EXPERIMENT No. 02

A. Aim: To analyze and study the time response of RC and RL circuits.

B. Apparatus Used: 1. DSO, DC Power Supply, function generator, breadboard. Resistor 100Ω (1), Resistor 10KΩ (1), Capacitor 0.01μF (1), Inductor 1mH (1).

C. Theory: If a voltage is applied to a capacitor, of value C, through a resistance of value R, the voltage across the capacitor rises slowly, as it charges. The time constant is defined as the time it will take to charge to 63.21% of the final voltage value.

Graph between voltage and the charging time.



Formula for time constant (τ = RC) This value is derived from the mathematical constant *e*, specifically $1 - e^{-1}$, more specifically as voltage to charge the capacitor versus time

Charging , $\mathbf{V_C\,(t) = V\,(1 - e^{-t/\tau})}$, = 0.63**V**

Discharging , $\mathbf{V_C\,(t) = V\,(e^{-t/\tau})}$, = 0.37**V**

V_C (t) = Voltage across the capacitor, V = Supply voltage.

After a period equivalent to 5 time constants, (5T) the capacitor in this RC charging circuit is virtually fully charged and the voltage across the capacitor is now approx 99% of its maximum value, 0.99Vs. The time period taken for the capacitor to reach this 5T point is known as the *Transient Period.* After a time of 5T the capacitor is now fully charged and the voltage across the capacitor, (VC) is equal to the supply voltage, (Vs). As the capacitor is fully charged, no more current flows in the circuit. The time period after this 5T point is known as the *Steady State Period*.

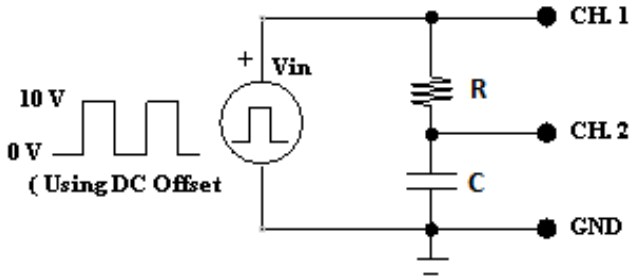


Figure 1.1: Integrator circuit

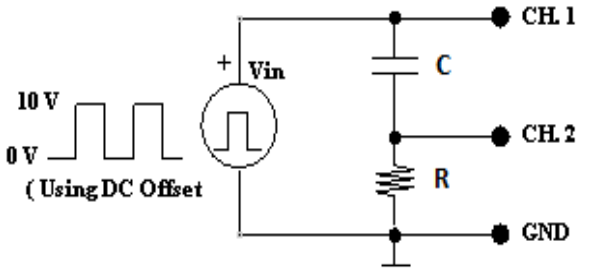
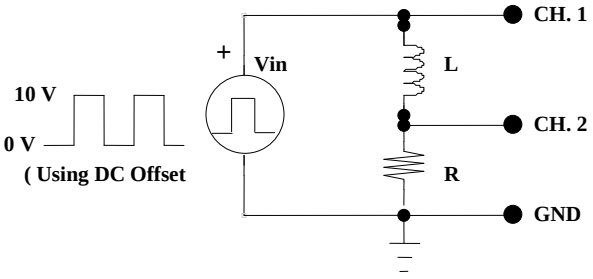


Figure 1.2: Differentiater circuit

For figures 1.1 and 1.2, use R = 10KΩ and C = 0.01μF



For figure 1.3, use R = 100Ω and L = 1mH

Figure 1.3: Series RL circuit

D. Procedure:

Exercise 1:- *STEP RESPONSE OF AN INTEGRATOR CIRCUIT:-*

Wire the circuit of figure 1.1. Connect the output of the function generator (FG) to the RC circuit and also the CH-1 input of the CRO. Choose a square wave signal. Adjust the amplitude control of the FG to obtain a waveform of 10V peak to peak (0-10). Connect the output of the RC circuit to the CH-2 input of the CRO (in DC Mode).

(i) Step response when T/2>>5τ; Choose the waveform frequency (f) to be 4 KHz. Observe and sketch V_i and V_o w.r.t. time. Note down the salient features of V_o.

Choose any two convenient points on the rising or falling part of V_o and measure the corresponding voltages and the time interval. Calculated (τ =RC) and compare the results with the values used.

(ii) Step response when $T/2 = 5\tau$. Choose $f = (1/2\pi\ \tau)$ Hz. Adjust the input signal frequency slightly, if necessary, to satisfy $T/2 = 5\tau$. Observe and sketch V_i and V_o.

(iii) Step response when $T/2 << 5\tau$: Choose f = 500Hz. Observe and sketch V_i and V_o.

Exercise 2:-*STEP RESPONSE OF A RC DIFFERENTIATOR CIRCUIT:*

Wire the circuit of fig.2. As in the case of RC integrator, Obtain step response of the RC circuit for the following three cases. Sketch V_i and V_o of each case.

1. Step response when $T/2 >> 5\tau$.

2. Step response when $T/2 = 5\tau$.

3. Step response when $T/2 << 5\tau$.

4. Increase the input signal frequency beyond 40 KHz and note the minimum frequency at which the linear tilt (drop) seen in the *Vo* waveform is negligible.

In case of charging V_{in} = Initial voltage at the start of charging, V_F = Supply voltage (p-p).

In case of discharging ; V_{in} = Initial voltage at the start of discharging, , V_F = 0.

Exercise 3:-*STEP RESPONSE OF RL CIRCUITS:* ($\tau = \frac{L}{R}$)*:*

Wire the RL circuit of Fig. 3. Keep the amplitude control of the FG as in the previous cases. Observe the step response when T/2<<5τ. The inductor given to you has a nominal value of 1mH. Adjust the frequency of the input signal in such a way that the maximum V_o *and* amplitude is well below its steady-state value. Choose any two convenient points on the rising and falling parts of V_o and calculate it. Note down the signal frequency.

$$I_c(t) = I_{in} + (I_F - I_{in})\, e^{\frac{-t}{\tau}}$$

E. Observation: *(Include your own Table relevant to the Experiment)*

For Integrator circuit:-

Theoretical value of **τ:**		
Input Frequency (Hz)	Experimental value of **τ**	Error (%)
500Hz (Square wave, 0-10 Volt)		
(1/ **2πτ)** Hz (Square wave, 0-10 Volt)		
4KHz (Square wave, 0-10 Volt)		

For Differentiator circuit:-

Theoretical value of **τ:**		
Input Frequency (Hz)	Experimental value of **τ**	Error (%)
500Hz (Square wave, 0-10 Volt)		
(1/ **2πτ)** Hz (Square wave, 0-10 Volt)		
4KHz (Square wave, 0-10 Volt)		

For RL circuit:-

Theoretical value of **τ:**		
Input Frequency (Hz)	Experimental value of **τ**	Error (%)
5KHz (Square wave, 0-10 Volt)		
(1/ **2πτ)** Hz (Square wave, 0-10 Volt)		
40KHz (Square wave, 0-10 Volt)		

(Adjust input voltage after connecting FG to RL circuit)

F. Analysis of Results: - *(Include sample calculations/Display/plot/typical graph)*

○ Also draw the input and output frequency at each frequency division with indicating t_1, t_2 and v_1, v_2 on the observation sheet.

G. Conclusions: *This practical practice helps us to understand:*

○ Making of a circuit with circuit elements.
○ Behavior of a signal passing through an RC circuit.
○ Time constant and its usefulness.
○ Voltage and current measurement with CRO.

Precautions:

1. Always connect V_{cc} to positive rail and GND to the negative rail in the breadboard.
2. Do not short positive and negative terminal each other.
3. The observation should be taken properly.
4. If possible draw the waveform on plain paper/ rough notebook with time and voltages.

EXPERIMENT No. : 03

A. Aim: To analyze and study the frequency response of RC and RL circuit.

B. Apparatus Used: 1. DSO, DC Power Supply, Function Generator, Breadboard.
2. Resistor 10KΩ (1), Resistor 100Ω (1), Capacitor 0.01µF (1), Inductor 1mH (1)

C. Theory: RC and RL circuits are often used in electronics circuits to achieve frequency selection. For example RC and RL filters that are commonly used to pass a certain band of frequencies and to stop (attenuate) another band of frequencies. For applications such as the above, understanding the frequency response of a circuit is important. The aim of this experiment is to study the frequency response characteristics of some of the commonly used RC and RL circuits. For this purpose sinusoidal signals are applied to the inputs of these circuits and their output responses are observed and then compared with theory.

Figure 3.1: RC Low Pass Circuit:-

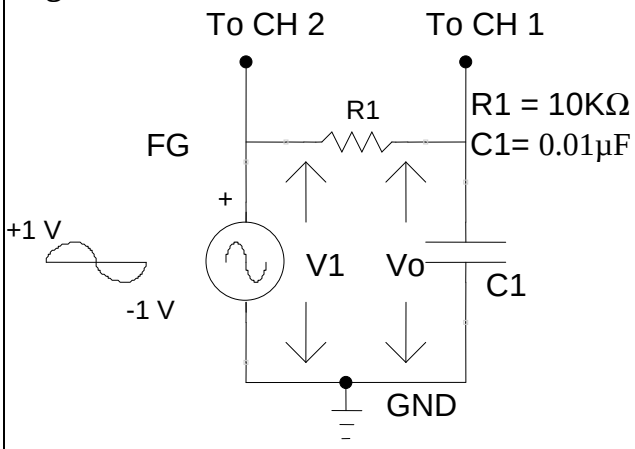


Figure 3.2: RC High Pass Circuit:-

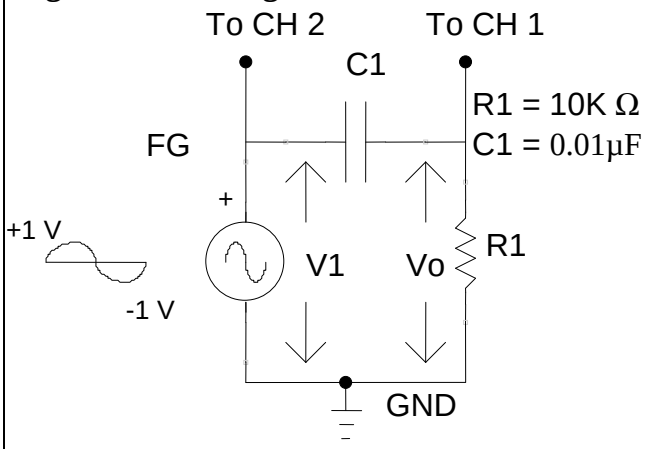


Figure 3.3: RL Low Pass Circuit:-

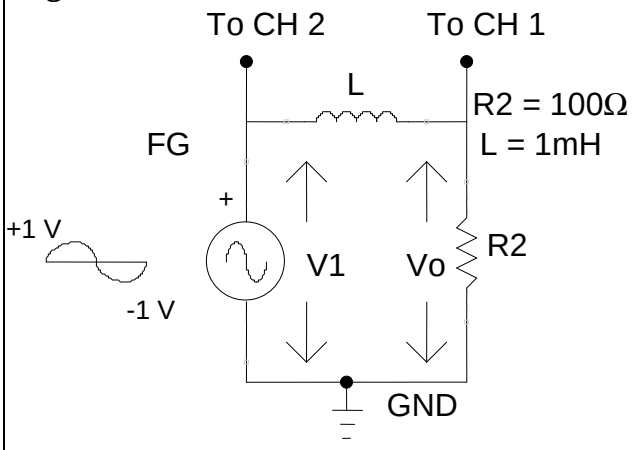
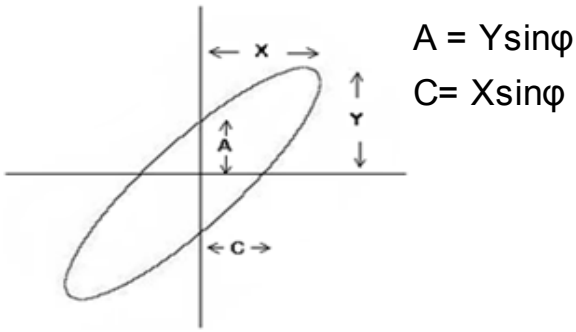


Figure 3.4: Phase measurement.



A = Ysinφ

C= Xsinφ

(Lissajous pattern)

If input is a sine wave, then the output also is a sine wave, but with a different amplitude and phase shift. Gain and output amplitude may be calculated with the following formulas,

The gain of an RC circuit is = $\frac{1}{\sqrt{jwRC+1}}$,

Magnitude of output waveform =$\frac{1}{\sqrt{1+(wRC)^2}}$ and

Phase shift = - arctan ($\frac{wRC}{1}$).

D. Procedure:

For RC low pass circuit:

Exercise 1:- *Frequency Response:*

Wire the RC low pass circuit of figure 3.1. Set up the function generator to produce a sine wave of amplitude of 2 V peak to peak (-1 V to +1 V). Connect V_O to CH. 1 and V_1 to CH. 2 of the CRO.

For several frequencies from about 100 Hz to 40 KHz, measure the gain $\frac{V_O}{V_I}$ (take more reading around the -3db points), for each of these frequencies. Plot the frequency response G *(f)* = $20log\left(\frac{V_O}{V_I}\right)$ versus *f* on a semi log graph paper. Measure the -3db frequency f_c. Calculate F_C =$\frac{1}{2\pi RC}$ using the given R and C values. Compare this $\boldsymbol{f_c}$ with the measured value.

Exercise 2:- Lissajous pattern:- Display the X-Y points of the two waveforms $\boldsymbol{V_i}$ **(t)** and $\boldsymbol{V_o}$ **(t)**. Keep the sensitivities of both CH1 and CH2 of the CRO to be the same. Ensure that when CH. 1 and CH. 2 are put to GND. The X-Y plot appears as a dot exactly at the center of the CRO (origin).

Vary the frequency of the sine wave supplied and observe the shape of the Lissajous pattern. A sample Lissajous pattern is shown in figure e1.2. Measure the X coordinates – (C and X) and Y Coordinates – (A and Y), as a cross check for three frequencies $<<f_c$, $f = f_c$ and $f>>f_c$.

Calculate 'φ'from the relationship C = Xsinφ or A = Ysinφ . Comment on the changes in the shape of the ellipse observed on the CRO.

For RC high pass circuit:

Wire the RC high pass of figure1.3. Repeat exercise (1) and (2).Use the same 10KΩ and 0.01 μF.

For RL low pass circuit:

Wire the RL low pass circuit of figure 1.4. Repeat exercise (1) and (2).

A. E. Observation*: (Include your own Table relevant to the Experiment)*

RC Low pass filter

Frequency	V_o	Gain	Gain(dB)	X	C	φ= arcsin(C/X)
1. 500 Hz						
….						
10. 50 KHz						

RC High pass filter

Frequency	V_o	Gain	Gain(dB)	X	C	φ= arcsin(C/X)
1. 500 Hz						
….						
10. 35 KHz						

RL Low pass filter

Frequency	V_o	Gain	Gain(dB)	X	C	φ= arcsin(C/X)
1. 5 KHz						
….						
10. 500 KHz						

(Choose the frequencies so that they cover the entire frequency range uniformly and take more number of readings close to the cut-off frequency)

F. Analysis of Results:

(Include sample calculations/Display/plot/typical graph)

G. Conclusions: *This practical practice helps us to understand:*

- Relationship between frequency and impedance of a RC and RL circuit.
- Measuring the phase difference with the help of CRO and Lissajous pattern.
- Low pass and high pass circuit working.

Precautions:

1. Use separate zero voltage label for both channels if visualized both channel at the same time.
2. Take more number of readings close to the cutoff frequency, to generate a smooth response.
3. At the time of creating Lissajous pattern Volts/Div. of both channels of CRO should be equal.
4. Reduce the CRO intensity if the dot is much brighter, to avoid damage to the screen.

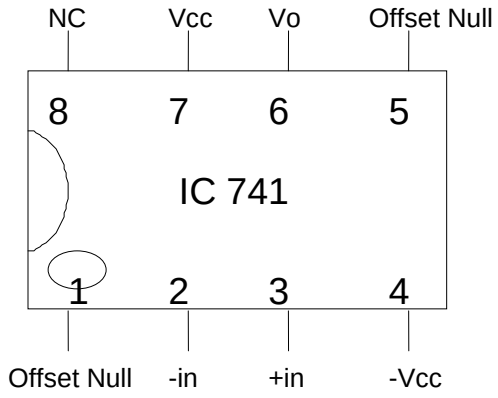
EXPERIMENT No. : 04

A. Aim: To design and analyze an inverting and non- inverting mode amplifier using operational amplifier.

B. Apparatus Used: 1. DSO, Function generator, breadboard, DC Power supply.
2. IC Op-Amp (1), resistor R1 (1), resistor R2(1)

C. Theory: An operational amplifier (op amp) is an electronic unit, which functions as a voltage controlled voltage source. It can be configured for various other operations like an integrator, a differentiator, adder, subtractor etc., hence, the name "an operational amplifier".
IC 741 is the most popular op amp available as an IC package. A typical 741 IC has 8 terminals as elaborated below.

Figure 4.0:



Pin configuration of Op Amp 741

Pin no. 1:- To adjust offset Null.
Pin no. 2:- Inverting input.
Pin no. 3:- Non inverting input.
Pin no. 4:- Negative supply (-12Vcc) pin.
Pin no. 5:- To adjust offset Null.
Pin no. 6:- Output terminal.
Pin no. 7:- Positive supply (+12Vcc) pin.
Pin no. 8:- Not connected.

Figure 4.1: Inverting mode amplifier

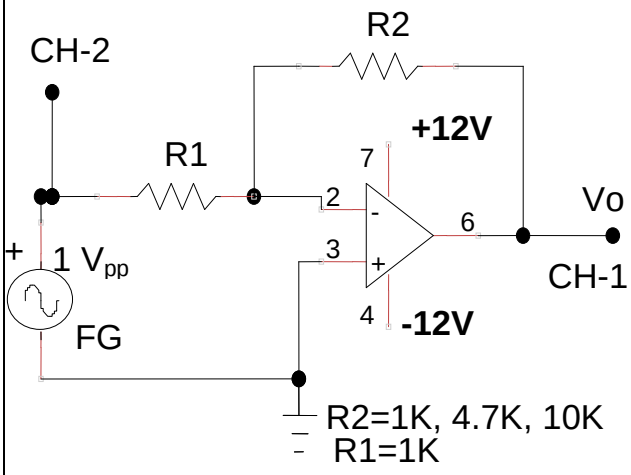
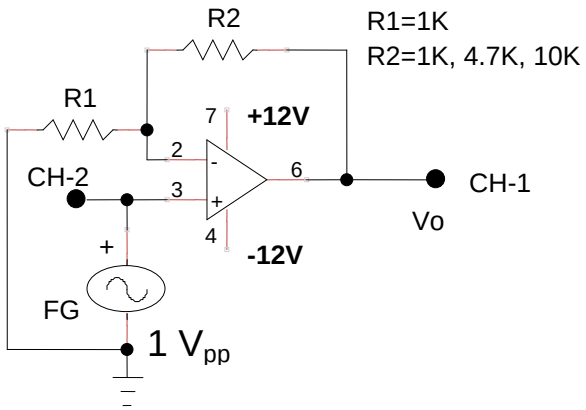


Figure 4.2: Non inverting mode amplifier

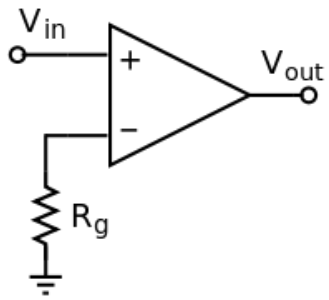


Basic information about 741IC:
Supply Voltage- (**LM741A**) ±22V, (**LM741**) ±22V, (**LM741C**) ±18V

Power Dissipation- (**LM741A**) 500 mW, (**LM741**) 500 mW, (**LM741C**) 500 mW

Input Voltage- (**LM741A**) ±15V, (**LM741**) ±15V, (**LM741C**) ±15V

Operating Tem.-- (**LM741A**) −55°C to +125°C , (**LM741**) −55°C to +125°C, (**LM741C**) 0°C to +70°C.



An op-amp without negative feedback (a comparator)

Operation:-The amplifier's differential inputs consist of a non-inverting input (+ve) and an inverting input (–ve); ideally the op-amp amplifies only the difference in voltage between the two, which is called the *differential input voltage*. The output voltage of the op-amp $\mathbf{V_{out}}$ is given by the equation:

$$V_{\text{out}} = A_{\text{OL}}(V_+ - V_-)$$

Where A_{OL} is the open loop gain of the amplifier (the term "open-loop" refers to the absence of a feedback loop from the output to the input).

D. Procedure: ***For Inverting Mode: -***
Step 1:- Design an inverting mode amplifier configuration **for a gain of 1 (unity gain)** as shown in figure1.1.
Step 2:- Apply a sinusoidal input of amplitude 1 V (peak-to-peak),
Step 3:- Vary the frequency of the input signal from low frequency (e.g. 100Hz) to high frequency (e.g. 100 KHz).
Step 4:- Observe the lowest and the highest input signal frequency for which gain remains constant.
Step 5:- Take two readings of output voltage, one at the lowest and the other at the highest frequency for which gain remains constant.
Step 6:- Near the highest frequency, take multiple readings. Note down the output voltage and measure – 3db frequency.
Step 7:- Plot the frequency response and calculate the bandwidth. i.e. Bandwidth = F_H - F_L.
Step 8:- Calculate and note the Gain-Bandwidth product (GBP).
Repeat Steps 1-8 for gains of 4.7 and 10.

For Non- inverting Mode:-
Step 1:- Design a non- inverting mode amplifier configuration as shown in figure 1.2.
Step 2:- Repeat the steps, as mentioned above for gains of 2, 5.7 and 11.

E. Observation*:* -

For Inverting Mode: -

Input voltage V_{in} =							
S.No.	Input frequency	Designed Gain = 1		Designed Gain = 4.7		Designed Gain = 10	
		V_o	Gain (dB)	V_o	Gain (dB)	V_o	Gain (dB)
1							
…..							
20							
		Bandwidth		Bandwidth		Bandwidth	
		GBP		GBP		GBP	

For Non inverting Mode: -

Input voltage V_{in} =							
S.No.	Input frequency	Designed Gain = 2		Designed Gain = 5.7		Designed Gain = 11	
		V_o	Gain (dB)	V_o	Gain (dB)	V_o	Gain (dB)
1							
…..							
20							
		Bandwidth		Bandwidth		Bandwidth	
		GBP		GBP		GBP	

F. Analysis of Results:

(Include sample calculations/Display/plot/typical graph)

G. Conclusions: *This practical practice helps us to understand:*

- Working of an operational amplifier IC 741.
- Inverting and non-inverting mode of operational amplifier.
- Negative feedback in an operational amplifier.
- Effect of gain on bandwidth of the amplifier, and the behavior of Gain-Bandwidth product (GBP).

Precautions:

1. Measure the function generator voltage on CRO by appropriately choosing V/D.
2. Connect +12V to pin no. 7 and -12V to pin no. 4, in IC741.
3. Connections should be done properly and readings should be taken carefully.

EXPERIMENT No. : 05

A. Aim: To design, analyze and implement summing and scaling amplifier circuit using Op Amp (IC 741).

B. Apparatus Used: 1. DSO, Function Generator, Breadboard,
2. Resistor 10KΩ (4), 150Ω (3), 5.6KΩ (1), IC741, Jumper wires.

C. Theory: ***Summing Amplifier: -***
As the name 'operational amplifier' suggests, depending on the nature and placing of various electrical components in combination with an op-amp with feedback, the whole circuit can be configured to execute various operations. In this experiment, we will configure IC741 to function as a summing amplifier.

Consider the circuit as shown in figure 5.1. Applying KCL at node X, $\mathbf{I_a + I_b + I_c = I_F}$
Because of the very high open loop gain, we can apply the virtual ground concept and deduce that Vx = 0, as the terminal 3 is connected to ground.
Therefore, $I_a = \frac{V_a}{R_{in}}$, $I_b = \frac{V_b}{R_{in}}$, $I_c = \frac{V_c}{R_{in}}$ and $I_F = -\frac{V_o}{R_F}$
Thus, we get

$$\boldsymbol{V_o = -\frac{R_F}{R_{in}}[\,Va + Vb + Vc\,]}$$

If $R_F = R_{in}$ then we get, $\mathbf{V_o = -(V_a + V_b + V_c)}$. We have hence configured a summing amplifier.

Figure 5.1: Circuit diagram for summing amplifier

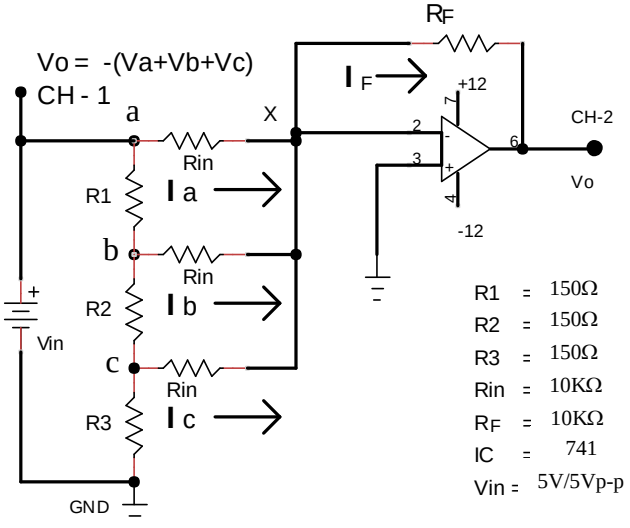
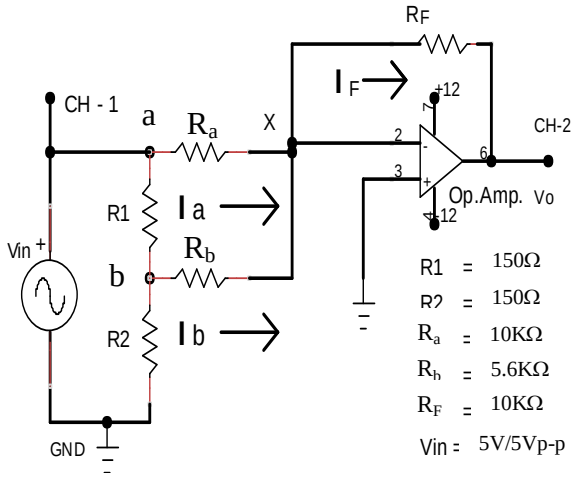


Figure 5.2: Scaling Amplifier:-



It must be noted that for the summing amplifier case, the input resistors (resistors connected between the input voltage node, and terminal 2) were kept same (R_{in}).

A **Scaling Amplifier** can be made if the individual input resistors are "NOT" same. Then the equation would become:

$$V_o = -R_F\left(\frac{V_a}{R_a} + \frac{V_b}{R_b} \ldots \text{etc}\right)$$

Thus, the output will be a scaled (weighted) combination of the input voltages.

D. Procedure:-

Summing amplifier (All DC and All AC case)

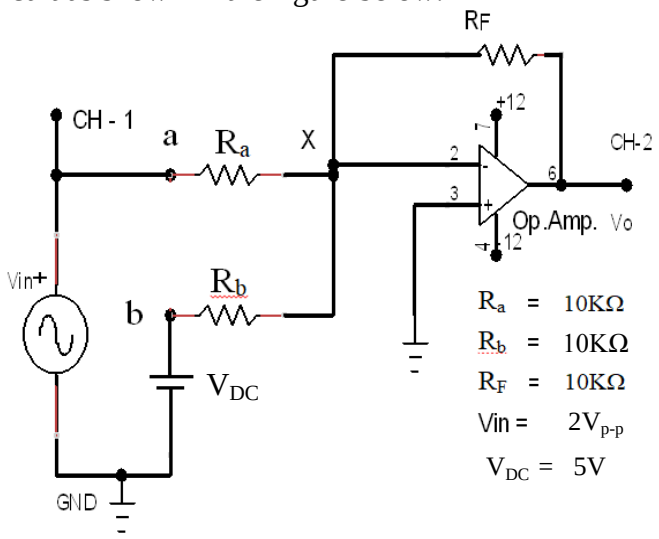
Step 1:- Connect the circuit as shown in the figure 5.1.

Step 2:- Apply input voltage of 5V DC/ 5V $_{P\text{-}P}$ amplitude at 1 KHz frequency (AC). Note down the output voltage from the CRO for each circuit.

Step 3:- Compare the observed output voltage with the theoretical values.

Summing amplifier (AC with DC case)

Step 1:- Connect the circuit as shown in the figure below:



Step 2:- Apply input voltage of $2V_{P\text{-}P}$ amplitude at 1 KHz frequency (AC) to node a and $5V_{DC}$ to node b.

Step 3:- Observe the observed output voltage.

Step 4:- On a tracing chart, first plot V_a. Then plot V_b below it and finally plot observed V_o.

Scaling amplifier (All DC and All AC case)

Step 1:- Connect the circuit as shown in figure 5.2.

Step 2:- Apply input voltage of 5V DC/ 5V $_{p\text{-}p}$ amplitude at 1 KHz frequency (AC). Note down the output voltage from the CRO for each circuit.

Step 3:- Compare the observed output voltage with the theoretical values.

E. Observation*:*

Input	**V_a**	**V_b**	**V_c**	**Gain** ($-R_f/R_i$)	**Theoretical V_o**	**Experimental V_o**	**% Error (V_o)**
	Summing Amplifier						
All DC							
All AC							
	Scaling Amplifier						

	V_a	**V_b**	**Scale factor**		**Theoretical V_o**	**Experimental V_o**	**% Error (V_o)**
			A	**b**			
All DC							
All AC							

For summing amplifier (AC with DC case), attach the plots.

F. Analysis of Results:

(Include sample calculations/Display/plot/typical graph)

G. Conclusions: *This practical practice helps us to understand:*

○ How to design and implement a summing and scaling amplifier for all DC, all AC, AC with DC signals using resistive components and op-amp IC741.

Precautions:

1. The Voltage may be applied from different sources.
2. Feedback resistor should be connected between pin 2 and 6.
3. Connect proper polarity of voltage to the IC.

EXPERIMENT No. : 06

A. Aim: - To analyze and design an active band pass circuit using Op-Amp 741.

B. Apparatus Used:-

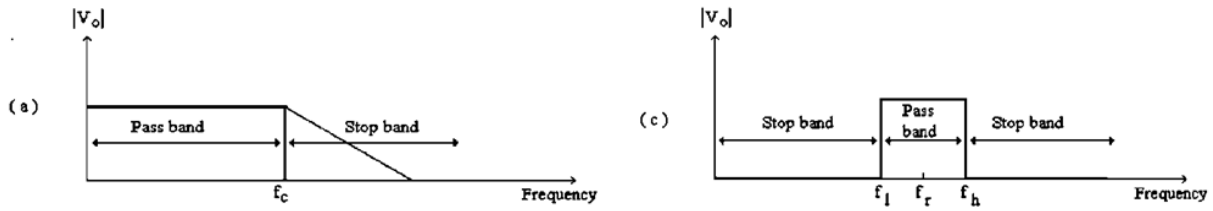
1. DSO, Function Generator, Breadboard, DC power supply.
2. Op Amp 742 IC (1 or 2), Resistor R1, R2, R3, R4, R5, R6 and capacitor C1, C2,

C. Theory: - An electric filter is a frequency-selecting circuit designed to pass a specified band of frequencies while attenuating signals of frequencies outside this band. Filters may be either active or passive depending on the type of elements used in their circuitry. ***Passive filters*** contain only resistors, capacitors, and inductors. ***Active filters*** employ transistors or op-amps in addition to resistors and capacitors. Active filters offer several advantages over passive filters. Since the op-amp is capable of providing a gain, the input signal is not attenuated as it is in a passive filter. Because of the high input and low output resistance of the op-amp, the active filter does not cause loading of the source or load.

A ***low-pass filter*** has a constant gain (***Gain = Vout / Vin***) generally from 0 Hz to a high cut off frequency f_H. This cut off frequency is defined as the frequency where the voltage gain is reduced to ***0.707 Volts*** times the maximum voltage, that is at f_H the gain is down by **3 dB**; after that ($f > f_H$) the gain decreases as frequency f increases. The frequencies between 0 Hz and f_H are called ***pass band*** frequencies, whereas the frequencies beyond f_H are the so-called ***stop band*** frequencies. A common use of a low-pass filter is to remove noise or other unwanted high-frequency components in a signal for which you are only interested in the DC or low frequency components.

Correspondingly, a ***high-pass*** filter has a stop band for $0 < f < f_L$ and where f_L is the low cut off frequency. A common use for a high-pass filter is to remove the DC component of a signal for which you are only interested in the AC components (such as an audio signal).

A ***bandpass filter*** has a pass band between two cut off frequencies f_H and f_L, $(f_H > f_L)$, and two stop bands $0 < f < f_L$ and $f > f_H$. The bandwidth of a bandpass filter is equal to $\sqrt{F_H - F_L}$. Figure 6.1 shows different frequency responses obtained from filters mentioned above.



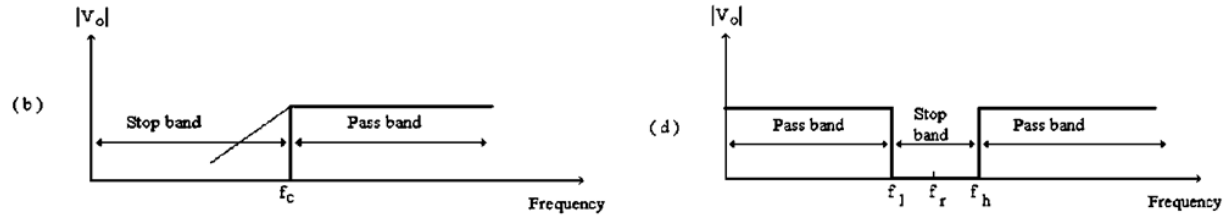


Figure 6.1 Frequency response of: a) Low Pass Filter, b) High Pass Filter, c) Band Pass Filter, and d) Band Stop Filter

The actual response curves of the filters in the stop band either steadily decrease or increase with increase of frequency. The ***roll-off rate***, measured at [dB/decade] or [dB/octave] is defined as rate change of power at 10 times (decade) or 2 times (octave) change of frequency in the stop band. The "***First-order***" filters attenuate voltages in the stop band ***20 dB/decade*** (for example, a first-order Lowpass filter would attenuate a signal at a frequency 100 times (2 decades) higher than f_H by 40 dB. The ***second-order filters*** attenuate by about ***40 dB/decade***. Figure 6.2 a) explains the concept mentioned above.

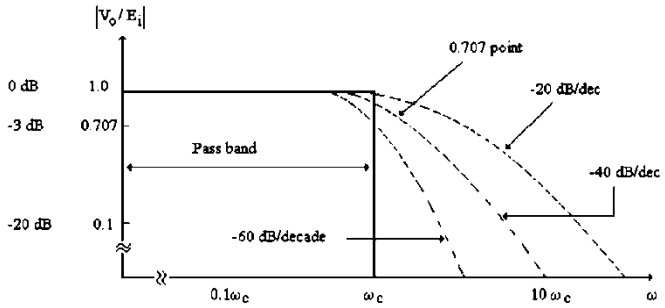


Figure 6.2 a) Ideal Vs Practical Frequency Response of 3 Different Low Pass Filters

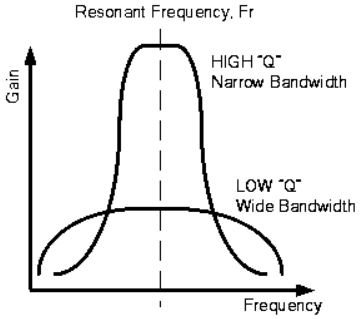


Figure 6.2 b) Bandwidth Vs Q Factor

Q Factor:-

A band-pass filter can be characterized by its ***Q factor***. The Q factor is the inverse of the fraction of bandwidth. A high Q filter will have a narrow pass band and a low Q filter will have a wide pass band. These are respectively referred to as narrow-band and wideband filters.

1. Design of first order high pass filter with given value of R_2 = 10KΩ and C_1 = 0.047μ*F*. Find the value of F_L (-3db frequency) using the formula $\frac{1}{2\pi R_2 C_1}$. Since a ***pass band gain of 4*** is required, the ***gain of each section is 2***, let $R_F = R_{in}$ =10 K, since the filter designed in the lab is a non-inverting the gain of the filter can be calculated using the formula = $1 + \frac{R_f}{R_{in}}$.

2. Design of first order low pass filter with the given value of R_2 = 10 KΩ and C_2 = 220pF. The value of F_H (-3db frequency) can be obtained using the formula = $\frac{1}{2\pi R_4 C_2}$.

Figure 6.1:- Band Pass Filter:-

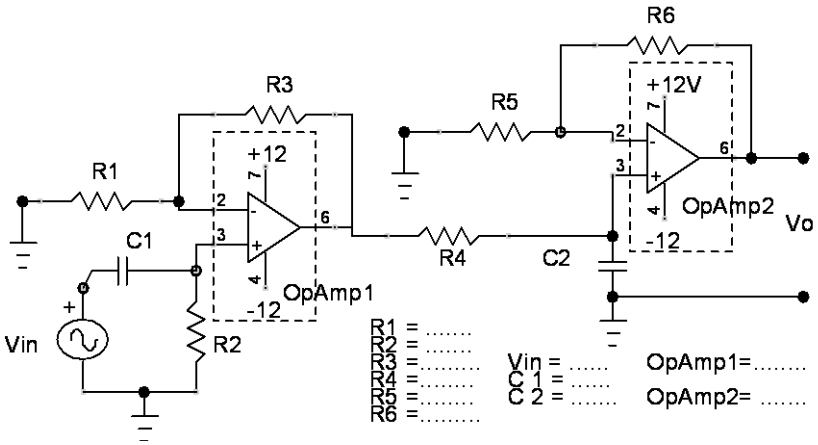


Figure 6.3 Two Stage Active Band Pass Filter Circuit

D. Procedure:-

Exercise 1:- Connect the circuit as shown in ***Figure 6.3***.

Exercise 2:- Apply sinusoidal input signal of ***0.2 Volt peak to peak amplitude of 500 Hz*** and vary the frequency and observe the frequency range for which you get a constant output voltage. Take two readings of output voltage at the two extreme ends of the frequency for which the gain remains constant. Now vary the frequency in period (as instructed in Lab.) on both sides of this corner frequency and note down the output voltages an measure – 3db frequency on both sides.

- ***-3dB frequency is the point where the total output power decreases by half of the maximum power or 0.707 volts lower than the maximum output voltage***

Exercise 3:- Calculate the gain obtained from the circuit in dB and plot the frequency response on a semi log graph paper.

Exercise 4:- Find bandwidth and value of **Q** using the formula provided below:

$$Q = \text{Central Frequency / Bandwidth} = \frac{f_c}{BW}$$

$$\text{Where } f_c = \sqrt{f_H f_L}$$

E. Observation Table: Fill the observation table with the values obtained experimentally.

S. No.	*Input Frequency*	*Input Voltage*	*Output voltage (In Volts)*	*Gain (V2/V1)*	*Gain in dB (20 log V2/V1)*
1.		**0.2 Vpp**			
2.		**0.2Vpp**			
3.		**0.2 Vpp**			
4.		**0.2 Vpp**			
5.		**0.2 Vpp**			
…..		**0.2 Vpp**			
15.		**0.2 Vpp**			

(***Take more readings around cut off frequency to create a linear graph***)

F. Analysis of Results:

(Include sample calculations/Display/plot/typical graph)

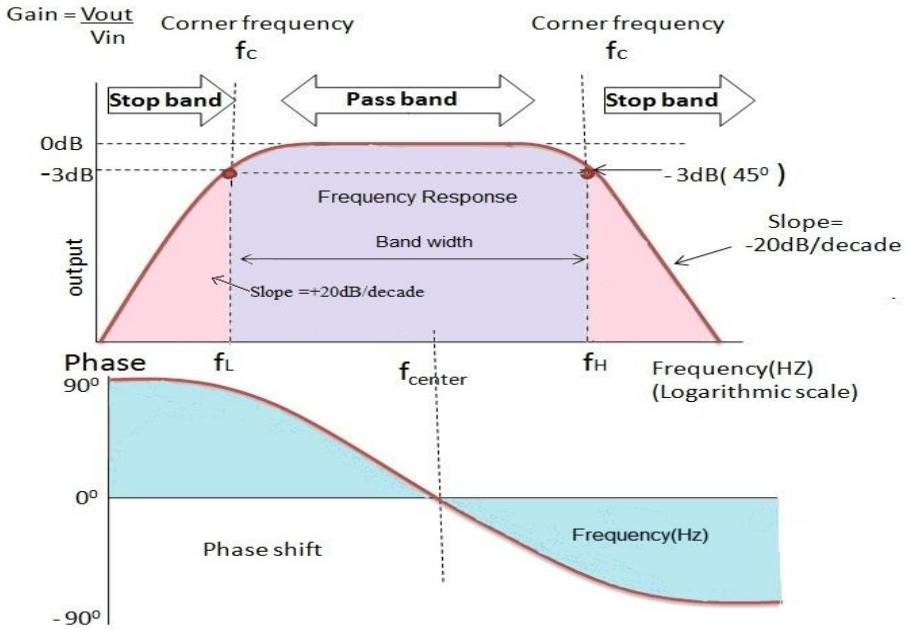


Figure 6.4 Frequency and Phase Response of a Band Pass Filter

G. Conclusions: *This practice helps us to understand:*

- Gain bandwidth product.
- Center frequency, cutoff frequency (3 dB).
- Use of two IC 741 in a circuit.

Precautions:

- Check the connections before switching on the circuit.
- Connections should be done properly. ***Remember +12 V and -12V are connected to pin 7 and 4 of the Op-Amp.***
- Take smaller frequency division near the lower and higher ends of the cutoff frequency.

EXPERIMENT No. : 07

A. Aim: - To study and analyze the basic logic gates and universal gates.

B. Apparatus Used:-

1. DSO, Breadboard, DC Power Supply.
2. Logic gates IC (7400, 7402, 7404, 7408, 7432, and 7486)

C. Theory: - The voltage in a digital circuit is allowed to be in only one of two states HIGH and LOW.
HIGH is taken to mean logical '1' or logical TRUE.
LOW is taken to mean logical '0' or logical FALSE.

***In The TTL logic family*:-**

Logic gates are classified by their logical functions and their logical families. In any implementation of a digital system, an understanding of a logic element's physical capabilities and limitations, determined by its logic family, are critical to proper operation. The purpose of this experiment is to provide an understanding of some of the characteristics of the transistor - transistor logic (TTL) family.

According to TTL logic, any voltage in the range 2 to 5.0 V is considered to be HIGH and any voltage in between 0 to 0.8 V is considered to be LOW. Any voltage outside this range is considered undefined, except for the very small durations of transition period. In TTL ICs transistors are used as switches with just two states, i.e., OPEN and CLOSED.

Logic signals interact by means of gates. The three fundamental gates AND, OR, and NOT are named after these three fundamental logical operations that they carry out. The function of each gate is defined by its TRUTH TABLE, which specifies the output state for each possible combination of input states. The physical basis for the truth tables can be understood in terms of two of more input switches providing logical HIGH or LOW and correspondingly output signals obtained from logic gates. A two input AND gate function resembles two switches in series, whereas, a two input OR gate works like two switches connected in parallel.

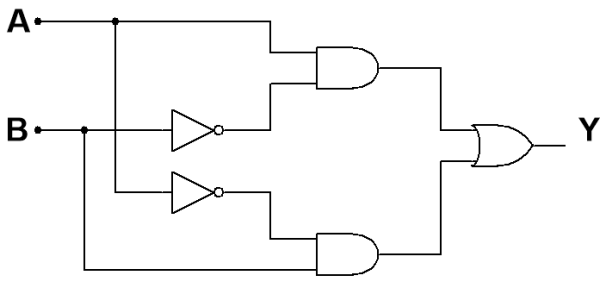


Figure7.1 X-OR Gate Designed Using Basic Logic Gates

- ***NAND and NOR gates are considered universal gates.***

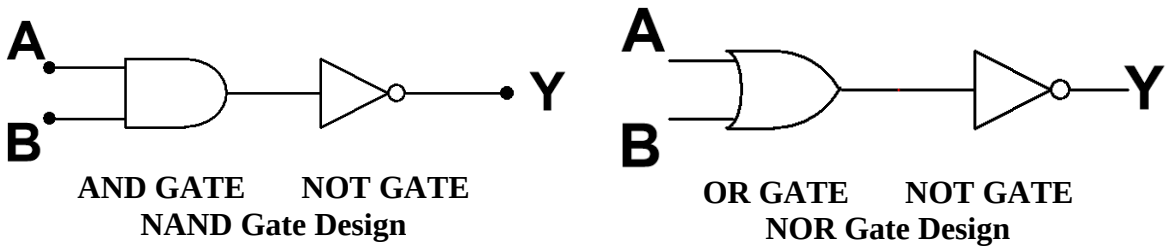


Figure7.2 Universal Gate using basic logic gates

D. Procedure:-

Exercise 1:- There are four logic AND gates in an IC7408 (***Quad 2-Input AND Gates***), IC7432 contains four OR gates (***Quad 2-input OR Gates***), and six logic NOT gates in IC7404 (***Hex Inverting Gates***). Similarly IC 7400, 7402 and 7486 contains multiple NAND, NOR and OR gates in them (***please refer Figure 7.3***). Observe the input and output pins of the ICs mentioned above carefully.

Exercise 2:- Connect the gates provided in the ICs test and verify the truth tables of each gate individually and fill in the tables provided below.

Exercise 3:- Verify the truth table of AND, OR, NOT, NOR, NAND Gates.

E. Observation*:* Verify the truth tables given below using the ICs provided in the lab.

NOT Gate

A	A′
0	
1	

AND Gate

A	B	Y
0	0	
0	1	
1	0	
1	1	

OR Gate

A	B	Y
0	0	
0	1	
1	0	
1	1	

Ex-OR Gate

A	B	Y
0	0	
0	1	
1	0	
1	1	

NAND Gate

A	B	Y
0	0	
0	1	
1	0	
1	1	

NOR Gate

A	B	Y
0	0	
0	1	
1	0	
1	1	

Ex-NOR Gate

A	B	Y
0	0	
0	1	
1	0	
1	1	

F. Analysis of Results:- Write your analysis of experiment in this section.

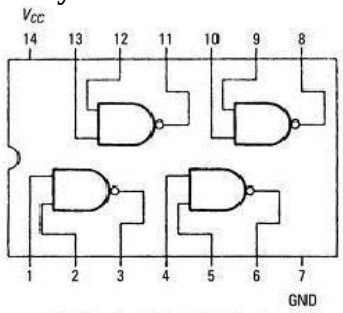


Fig: 7400 Quadruple 2-input NAND gates

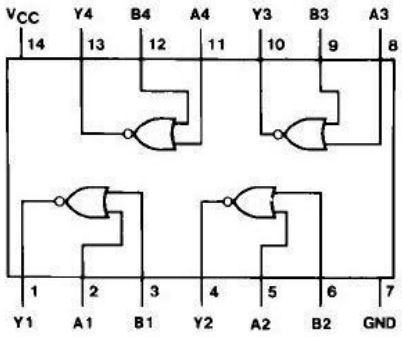


Fig: 7402 Quad 2 imput NOR Gate

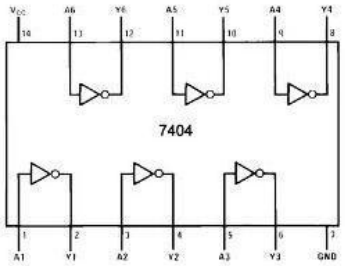


Figure: 7404 Hex Inverter

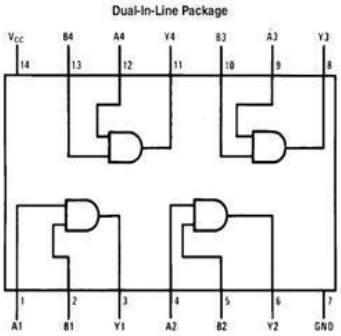


Illustration 1: IC 7408 Quad 2 input AND Gate

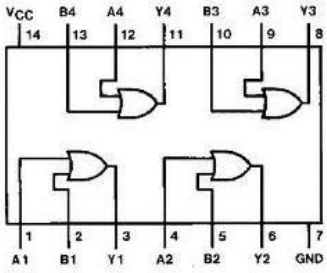


Fig: 7432 Quad-2 input OR Gate

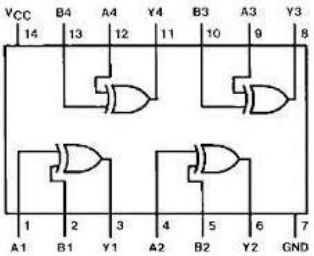


Fig: 7486 Quad- 2 input XOR Gate

Figure 7.3: Internal Configuration of Different Logic Gate ICs

G. Conclusions: - *This practical practice helps us to understand:*

- Concept of digital input and output become clear.
- Functioning of various digital IC.

Precautions:-

1. Check the connections before switching on the kit.
2. Connections should be done properly.
3. Do not connect more than +5 volt VCC in TTL IC.

EXPERIMENT No. : 08

A. Aim: - To analyze and design digital circuits used for performing basic arithmetic operations: addition and subtraction.

B. Apparatus Used: - 1. DSO, Function Generator, Breadboard, DC power supply.

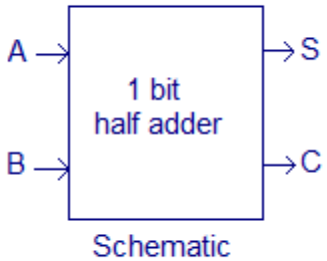
2. IC 7400(2), 7408(1), 7432(1), 7486(1), Jumper wires.

C. Theory: *Binary Adder:* -Adder plays an important role in digital circuits, especially, of course, in computers as digital circuits are typically binary adders, Multidigit binary values are added 1 bit position at a time each position produces a sum digit and a carry output (C_{out}) into the next bit position.

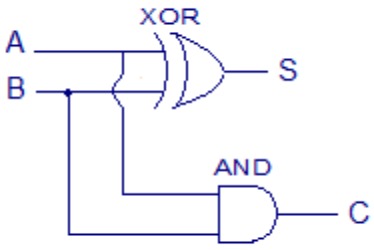
Half Adder: **-** The addition table for two binary digits is shown in Table 1. This table shows that the sum and carry produced by the addition of 2 bits. Note that the sum is The Exclusive- OR function, and carry is simply the AND function. Since the previous bit position can produce carry, the adder really reads three inputs, the 2 bits to be added, plus carry from previous bit position. An adder without the carry input C_{in} is referred to is a half adder. An Adder that provides for the carry input is termed a Full Adder. Shown in table 2 is the truth table for a Full Adder.

Inputs		Outputs	
A	B	S	C
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

Truth table



Schematic

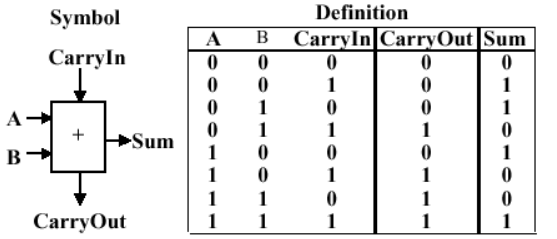


Realization

Full Adder: - This type of adder is a little more difficult to implement than a half-adder. The main difference between a half-adder and a full-adder is that the full-adder has three inputs and two outputs. The first two inputs are A and B and the third input is an input carry designated as C_{IN}. When full adder logic is designed we will be able to string eight of them together to create a byte-wide adder and cascade the carry bit from one adder to the next.

The output carry is designated as C_{OUT} and the sum output is designated as S. Take a look at the truth-table.

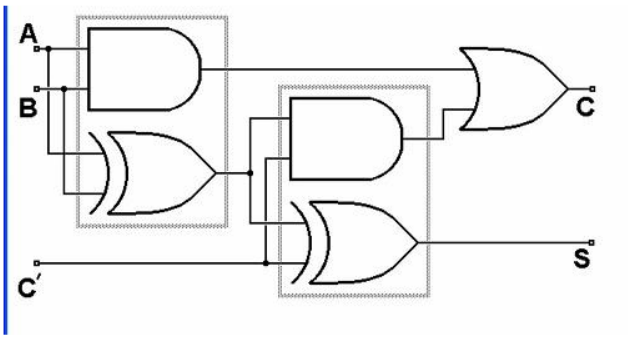
From the truth-table, the full adder logic can be implemented. We can see that the output S is an EX-OR between the input A and the half-adder SUM output with B and C_{IN} inputs. We must also note that the C_{OUT} will only be true if any of the two inputs out of the three are HIGH.



Definition

A	B	CarryIn	CarryOut	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

CarryOut = (A*B*CarryIn) + (A*B*CarryIn) + (A*B*CarryIn) + (A*B*CarryIn)
= (B*CarryIn) + (A*CarryIn) + (A*B)
Sum = (A*B*CarryIn) + (A*B*CarryIn) + (A*B*CarryIn) + (A*B*CarryIn)



Half subtractor: - The half subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, A (minuend) and B (subtrahend) and two outputs D_I (difference) and B_O (borrow). An important point worth mentioning is that the half subtractor diagram aside implements (b-a) and not (a-b) as borrow is calculated from the equation,

D_I (difference)= $\bar{A}.B$

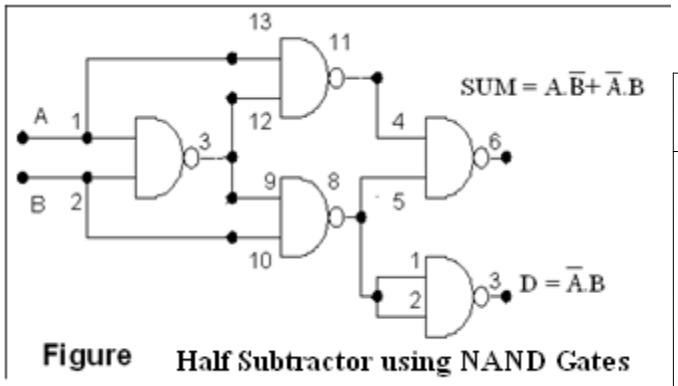


Figure Half Subtractor using NAND Gates

A	B	Diff.	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

D. Procedure: ***Exercise 1:-*** Connect whole circuit on Breadboard and Vcc and GND.

Exercise 2:- For logic 1 input connects particular pin to + 5 V and for logic 0 connects to ground with the help of jumper wire.

Exercise 3:-Enable AC/DC mode of CRO and adjust trace at zero voltage.

Exercise 4:-Now Change input variable (voltage) and note down the output (voltage). All exercises are common for HA, FA and HS.

E. Observation: (Include sample calculations/Display/plot/typical graph)

F. Analysis of Results: (Include sample calculations/Display/plot/typical graph)

G. Conclusions: This practical practice helps us to understand:

○ Binary adder and subtractor.

H. Precautions:

1. Check the connections before switching on the power supply.
2. Connections should be done properly.
3. The observation should be taken properly.

EXPERIMENT No.: 09

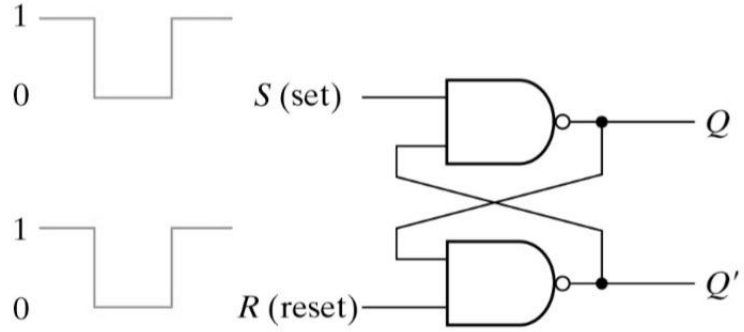
A. Aim: To analyze and design a sequential logic circuits (different Latches and Flip Flops).

B. Apparatus Used: 1. DSO, Function Generator, Breadboard.
2. ICs: 7400, 7404, 4027, LEDs, limiting resistors and jumper wires.

C. Theory: In digital circuit systems, ***sequential logic*** is a type of logic circuit whose output depends not only on the present value of its input signals but also on the past history of its inputs. This is in contrast to combinational logic, whose output is a function of only the present input. Consequently, sequential logic has state (memory, or storage element) while combinational logic does not; in other words, sequential logic is a combinational logic system with memory or storage element. Sequential logic is used to construct finite state machines, a basic building block in all digital circuitry, as well as memory circuits and other devices. Virtually all circuits in practical digital devices are a mixture of combinational and sequential logic.

Storage elements that operate with signal levels are referred to as **latches** and those operated with signal transition are **flip-flops**. In electronics, a latch or a flip-flop is a circuit that has two stable states and can be used to store state information. A flip-flop is a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Latches and flip-flops are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems.

SR Latch (SET/ RESET):
The SR latch is a circuit with cross-coupled NAND gates as shown in below figures. Two inputs *S* and *R* represent SET and RESET of the latch, respectively. The latch has two useful states. When output *Q = 1* and *Q' = 0*, the latch is said to be in SET state conversely, *Q = 0* and *Q' = 1*, the latch is said to be in RESET state.



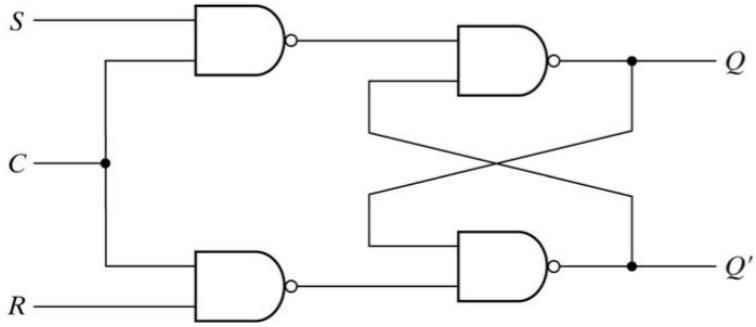
(a) Logic diagram

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	

(b) Function table

Figure 9.1: Building block of SET/ RESET Latch with NAND gates.

As shown in **Figure 9.1,** when *S = 0* and *R = 1* latch is in SET state and when *S = 1* and *R = 0* latch is in RESET state. Thus, is it called a S'R' latch. To make an *SR* latch using *S'R'* latch as a building block, two additional NAND gates is being used as shown in **Figure 9.2** with an additional control signal, which enables the *S* and *R* inputs to update the latch states *Q* and *Q'*. As in **Figure 9.2**, when *S = 1* and *R = 0* latch is in SET state and when *S = 0* and *R = 1* latch is in RESET state, thus making it an *SR* latch.



(a) Logic diagram

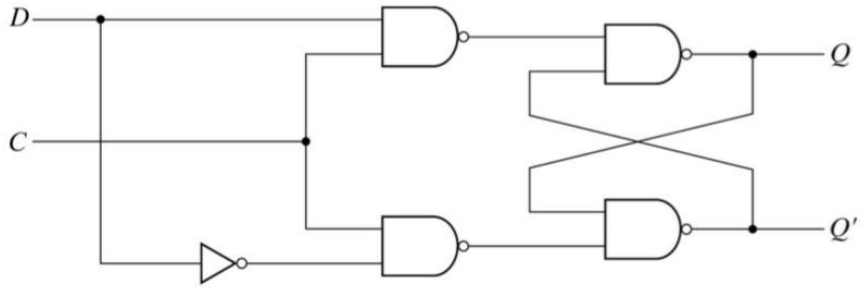
C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	Q = 0; Reset state
1	1	0	Q = 1; set state
1	1	1	Indeterminate

(b) Function table

Figure 9.2: SET/ RESET Latch with NAND gates.

D Latch:

If both *S* and *R* inputs go to logic HIGH at the same time with control input HIGH as shown in the functional table of **Figure 9.2**, output states go to indeterminate state. One way to alleviate this undesired condition of the indeterminate state is to ensure that inputs *S* and *R* are never equal to logic HIGH at the same time. This is done in the D type latch as shown in **Figure 9.3.** This latch has only two inputs *D* (Data) and *C* (control or enable). The D goes directly to the S input and its complimented version goes to R input. If *D = 1* with *C = 1* then latch is in SET state and if *D = 0* with *C = 1* then it is in RESET state.



(a) Logic diagram

C	D	Next state of Q
0	X	No change
1	0	Q = 0; Reset state
1	1	Q = 1; Set state

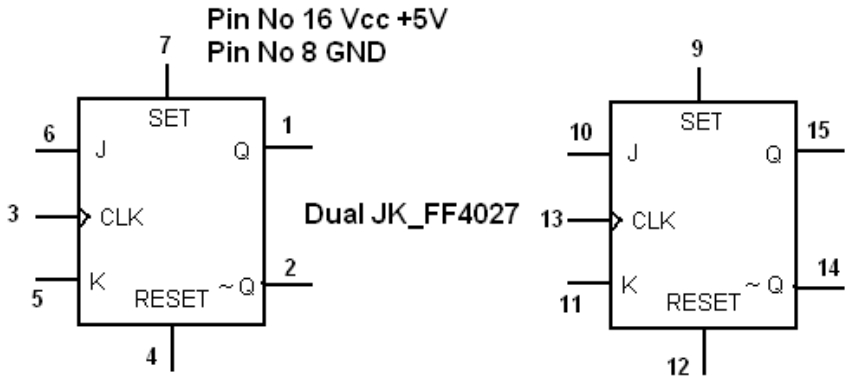
(b) Function table

Figure 9.3: D type latch with NAND gates.

JK Flip-Flop:

We are not supposed to make both inputs of the *RS* latch active at the same time (as discussed earlier), because it makes *Q* and *Q'* outputs the same value, and this is logically incorrect. The *Q'* outputs should always be the compliment of *Q* output. It would be useful to have a flip-flop that does something new and useful when both inputs are active, and This section describes the first attempt at designing a useful *JK* flip-flop.

Figure 9.4: IC 4027(Dual JK flip flop) pin configuration.



►The IC 4027 is an edge triggered dual *JK* flip-flop. Data is accepted when clock pulse is LOW, and transferred to the output on the positive-going edge of the clock.

►V_{CC} can be *5V*, *10V*, and *15V* power supply ratings at pin no. 16.

►V_{EE} at pin no. 8 connect to GND.

D and T Flip Flop using JK Flip Flop:

A *D* flip flop can be designed by using a *JK* flip flop and a NAND gate set as an inverter (or use inverter IC if available) as shown below in **Figure 9.5(a)**. If we short (joint) both the input of a *JK* flip flop, then it becomes a *T* flip flop as shown below in **Figure 9.5(b)**.

(a) **(b)**

Figure 9.5: *D* and *T* flip flops using a *JK* flip flop

Truth Tables for *D*, *JK* and *T* Flip Flops:

D	*CP*	*Q*
0	↑	*0*
1	↑	*1*

J	*K*	*CP*	*Q*
0	*0*	↑	*Q*
0	*1*	↑	*0*
1	*0*	↑	*1*
1	*1*	↑	*Q'*

T	*CP*	*Q*
0	↑	*Q*
1	↑	*Q'*

D. Procedure: ***Exercise 1:*** Design circuits as given in Figures from **Figure 9.1** to **Figure 9.3** and verify their functional (truth) tables. Prepare your tables as given in the example table below.

Exercise 2: Test *JK* flip-flop using the given *JK* flip-flop IC, prepare your truth table as given by the example table below. Use **Figure 9.5(a)** and **Figure 9.5(b)** to design and prepare also truth tables for *D* and *T* type flip-flops, respectively.

E. Observation: Include your own table relevant to the Experiment, two table examples for a latch and a flip-flop are given below.

Truth Table*:* ***RS Latch:***

R*(Voltage)*	**S***(Voltage)*	**Q***(Voltage)*	**Q'***(Voltage)*

Truth Table*:* ***Clocked J-K flip flop:***

CLK	J (Voltage)	K (Voltage)	Q(Voltage)	$\overline{Q}$(Voltage)
↑	0	0		
↑	0	1		
↑	1	0		
↑	1	1		

F. Analysis of Results:-

(Include sample calculations/Display/plot/typical graph)

G. Conclusions:-*This practical practice helps us to understand:-*

- Use of IC 4027.
- Memory element and array.
- Clocked *JK* flip-flop and latches.

Precautions:

1. Check the connections before switching on the DC supply.
2. Connections should be done properly.
3. The observation should be taken properly.