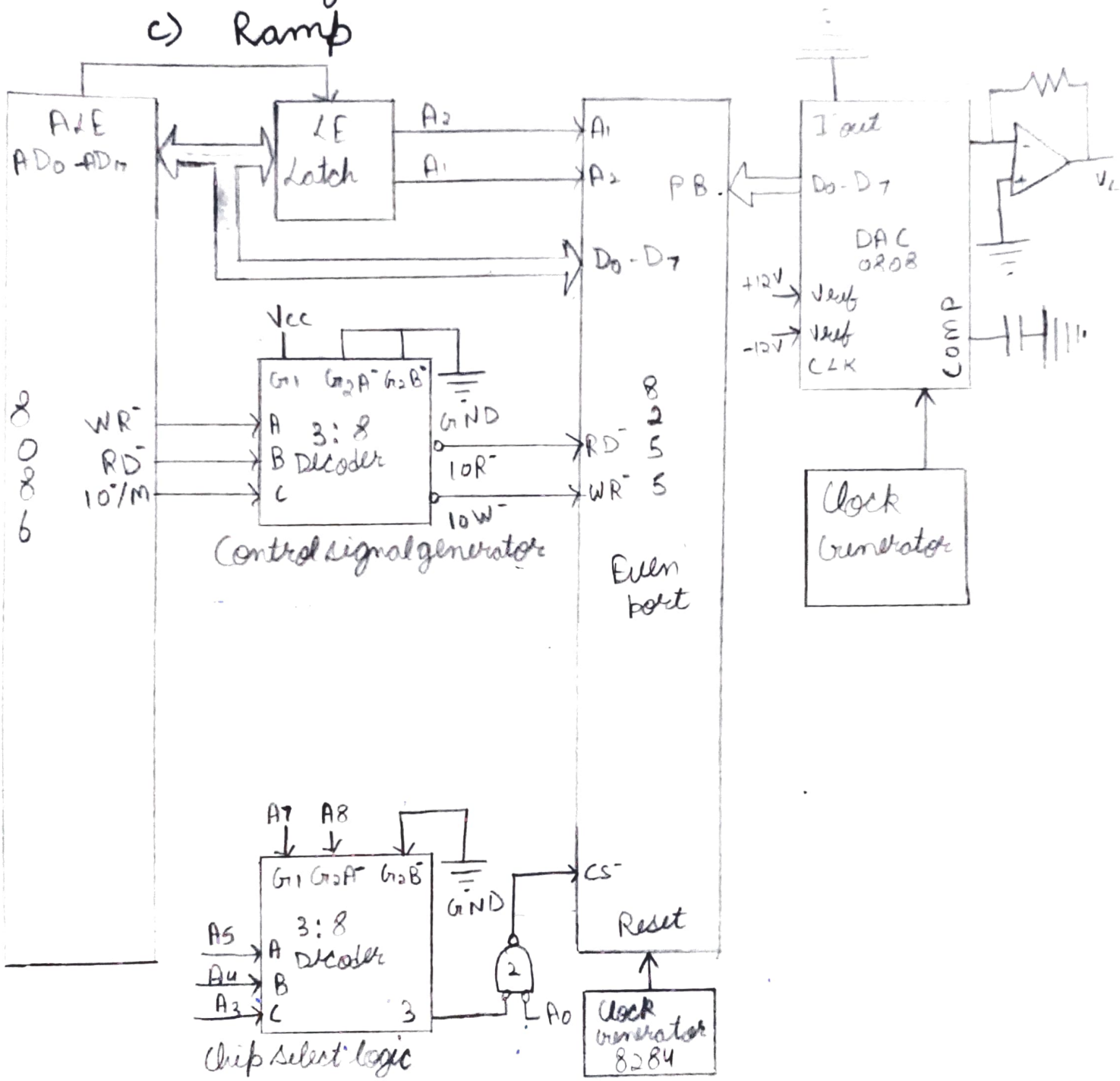
Q4 Interface an 8-bit DAC 0808 to 8086 through 8255 in IO mapped IO technique. Write a program to generate :-

a) Square wave

b) Triangular wave

c) Ramp



The port addresses and the addresses of the CWR may be decoded from this interfacing as :-

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
1	0	0	1	1	0	0	0	= 98H = PORTA
1	0	0	1	1	0	1	0	= 9AH = PORT B
1	0	0	1	1	1	0	0	= 9CH = PORT C
1	0	0	1	1	1	1	0	= 9EH = CWR

Decided by chip select logic

The control word will be 80H.

a) Program for square wave.


```
MOV AL, 80H  : Initialise all ports as output
OUT 9EH, AL  : Loads CWR
UP: MOV AL, 00H
    OUT 9AH, AL : Output 00 for 0V level.
    CALL DELAY : Calldelay.
    MOV AL, FFH : Output FF for 5 V level.
    OUT 9AH, AL
    CALL DELAY : Call delay
    JMP UP
```

b) Program for triangular wave.


```
MOV AL, 80H : Initialise all ports as output
OUT 9EH, AL : Load CWR
BEGIN: MOV AL, 00H: Output 00 for 0 V level
UP : OUT 9AH, AL: Output 00 for 0V level
     INC AL      : To raise wave from 0 V to 5 V increment
                   A
     CMP AL, 00H
     JNZ UP      : Jump up till rising edge is reached i.e.
                   5 V
```

```
    MOV AL, FFH
UP1: OUT 9AH, AL
     DEC AL        : To fall wave from 5V to 0V decrement AL
     CMP AL, FFH
     JNZ UP1       : Jump up till falling edge is reached, i.e. 0V
JMP BEGIN
```

c) Program for Ramp wave


```
     MOV AL, 80H : Initialise all ports as output.
     OUT 9EH, AL : Loads CWR
     MOV BL, FFH : Take FFH in B analog equivalent to 5V.
RAMP: MOV AL, BL : Copy to AL
     OUT 9AH, AL : And output it on the port.
     DEC BL      : To generate ramp wave this 5V is
                   continuously decreased till 0.
     JNZ RAMP    : Jump to RAMP if not 0
     MOV BL, FFH: To generate the same wave this procedure
                  is repeated
     JMP RAMP
     HLT
```