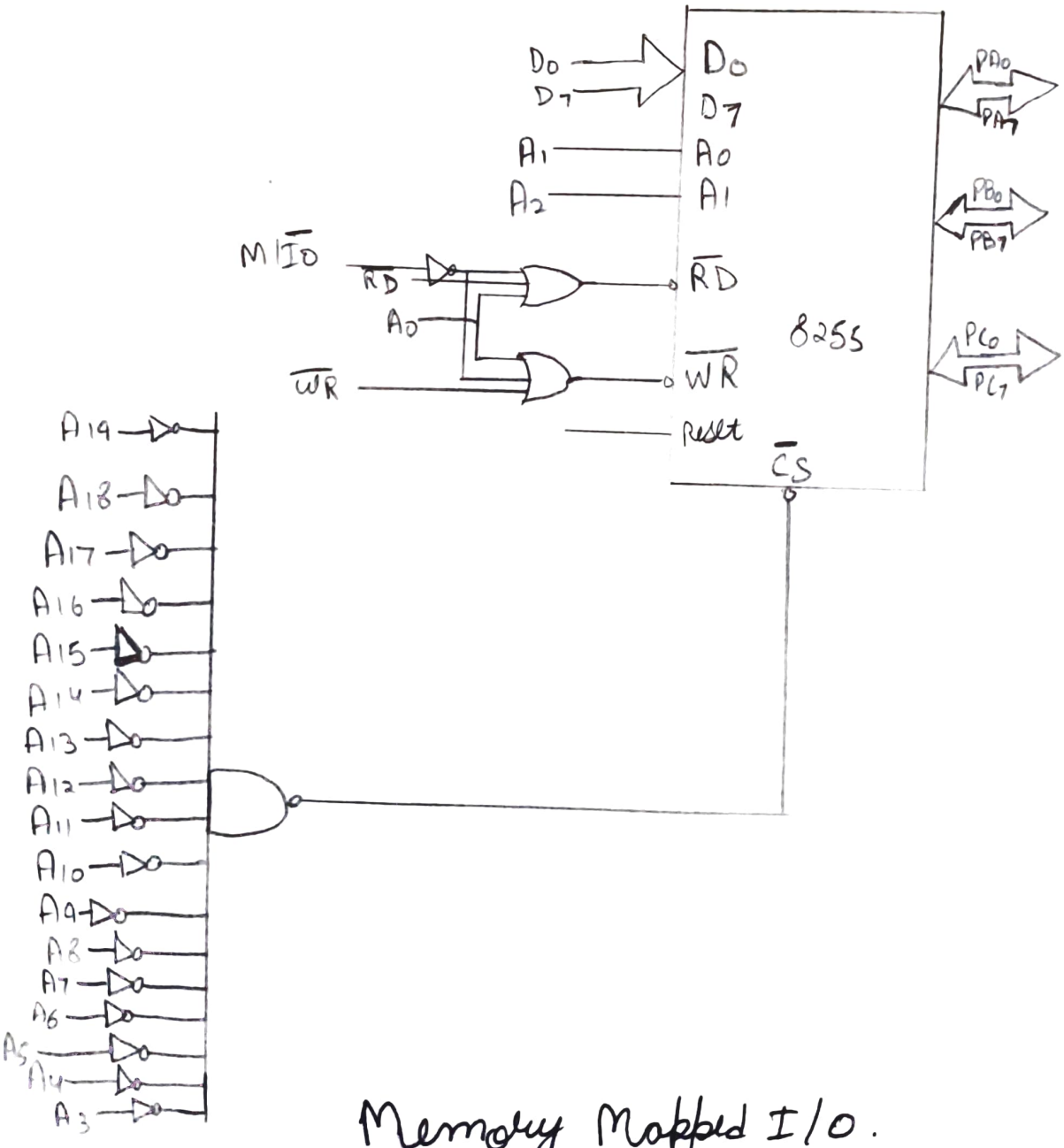
Q) Interface 8255 with 8086 in Memory Mapped I/O. Write the Port addresses.

→ In this type of I/O interfacing, the 8086 uses 20 address lines to identify an I/O device is connected as if it is a memory register. The 8086 uses same control signals and instructions to access I/O as those of memory. In the figure below, RD and WR signals are activated when M/IO signal is high, indicating memory bus cycle. Address lines $A_0 - A_1$ are used by 8255 for internal decoding. To get absolute address, all remaining Address lines ($A_3 - A_{19}$) are used to decode the address for 8255. Other signal connections are same as in I/O mapped I/O



Memory Mapped I/O.

Register	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Address
Port A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00000H
Port B	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	00002H
Port C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	00004H
Control register	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	00006H

I/O Map