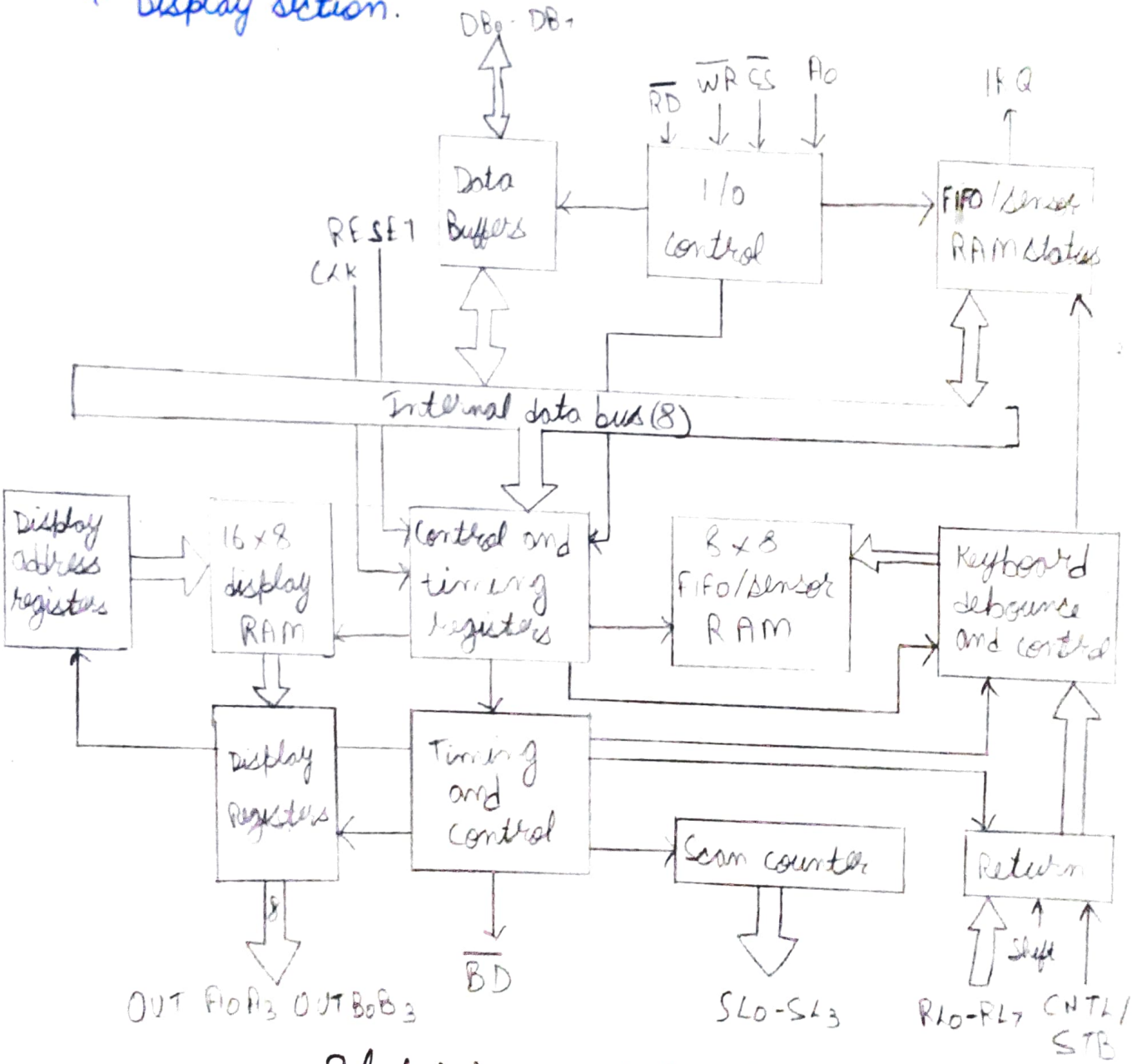
Q7 Draw and explain block diagram of 8279.

→ 8279 microprocessor consists of four main sections:-

1. CPU interface and control section.
2. Scan section.
3. 8279 keyboard section.
4. Display section.



Block Diagram of 8279

1. CPU Interface and Control Section - This section consists of data buffers, I/O control, control and timing registers and control logic.

- Data Buffer - The data buffers are 8-bit bi-directional buffer that connect the internal data bus to the external data bus.
- I/O control - The I/O control section uses the A0, CS, RD and WR signals to control data flow to and from the various internal registers and buffers. The data flow to and

from the Block Diagram of 8279 is enabled only when CS=0, otherwise the 8279 signals are in a high impedance state. The Block diagram of 8279 interprets the data given or desired by the CPU with the help of A0, RD and WR signals.

A0	$\overline{RD}$	$\overline{WR}$	Interpretation
0	1	0	Data from CPU to 8279
0	0	1	Data to CPU from 8279
1	1	0	Command word from CPU to 8279
1	0	1	Status word to CPU from 8279

- Control and Timing Registers - The control and timing registers store the keyboard and display modes and other operating conditions programmed by the CPU. The modes are programmed by sending the proper command on the data lines with A0 = 1.
- Timing Control - The timing control consists of basic timing counter chain. The first counter is divided by N prescaler that can be programmed to give an internal frequency of 100 kHz. The other counters divide down the basic internal frequency, to provide the proper keyscan, row scan, keyboard matrix scan, and display scan times.

2. **Scan Section** - The scan section has a scan counter which has 2 modes: Encoded mode and decoded mode.
   - Encoded Mode - In the encoded mode, the scan counter provides a binary count from 0000 to 1111 on the four scan lines (SC_3-SC_0) with active high outputs. The binary counter must be externally decoded to provide 16 scan lines.
   - Decoded Mode - In the decoded mode, the internal decoder decodes the least significant 2 bits of binary count and provides four possible combinations on the scan lines (SC_3-SC_0): 1110, 1101, 1011 and 0111. Thus the output of decoded scan is active low.

3. **Keyboard section** - This section consists of return buffers, keyboard debounce and control, FIFO/sensor RAM and FIFO/sensor RAM status. These functions depend on selected keyboard mode out of three keyboard input modes: scanned keyboard, sensor matrix and ~~sto~~ strobed input.

- **Return buffers** - The 8 return lines (RL7 - RL0) are buffered and latched by the return buffers during each row scan in scanned keyboard or sensor matrix mode in strobed input mode, the contents of the return lines are transferred to the FIFO RAM on the rising edge of the CNTL/STB line pulse.
- **Keyboard debounce and control** - Keyboard and debouncing control is enabled only when scanned keyboard mode is selected. In the scanned keyboard mode, return lines are scanned, looking for key closures in that row. If the debounce circuit detects a close switch, it waits about 10 msec to check if the switch remains closed.
- **FIFO/sensor RAM** - This is a dual function 8×8 RAM. In scanned keyboard and strobed input modes, it is a FIFO. Each new entry is written into successive RAM positions and then read in order of entry. In sensor matrix mode, the memory is referred to as sensor RAM.
- **FIFO/sensor RAM status** - FIFO RAM status keeps track of the number of characters in the FIFO and whether it is full or empty. The status logic also makes IRQ signal high when the FIFO is not empty, which can be used to interrupt CPU telling that key press is detected and keycode is available in FIFO RAM.

4. **Display section** - The display section consists of display RAM, display address registers and display registers.

- **Display RAM** - It is 16×8 RAM, which stores the display codes for 16 digits. It can be accessed directly by CPU. In decoded mode, 8279 uses only first four locations of display RAM. In encoded mode, Block Diagram of 8279 uses first eight locations for

8 digit display and all 16 locations for 16 digits display.

- Display address registers - The display address registers hold the address of the byte currently being written or read by the CPU and scan count value. The read/write addresses are programmed by CPU command. If set in auto increment mode, address in the address register is incremented for each read or write.
- Display registers - Display registers are two 4-bit registers A and B. They hold the bit pattern of character to be displayed. The contents of display registers A and B can be blanked and inhibited individually.