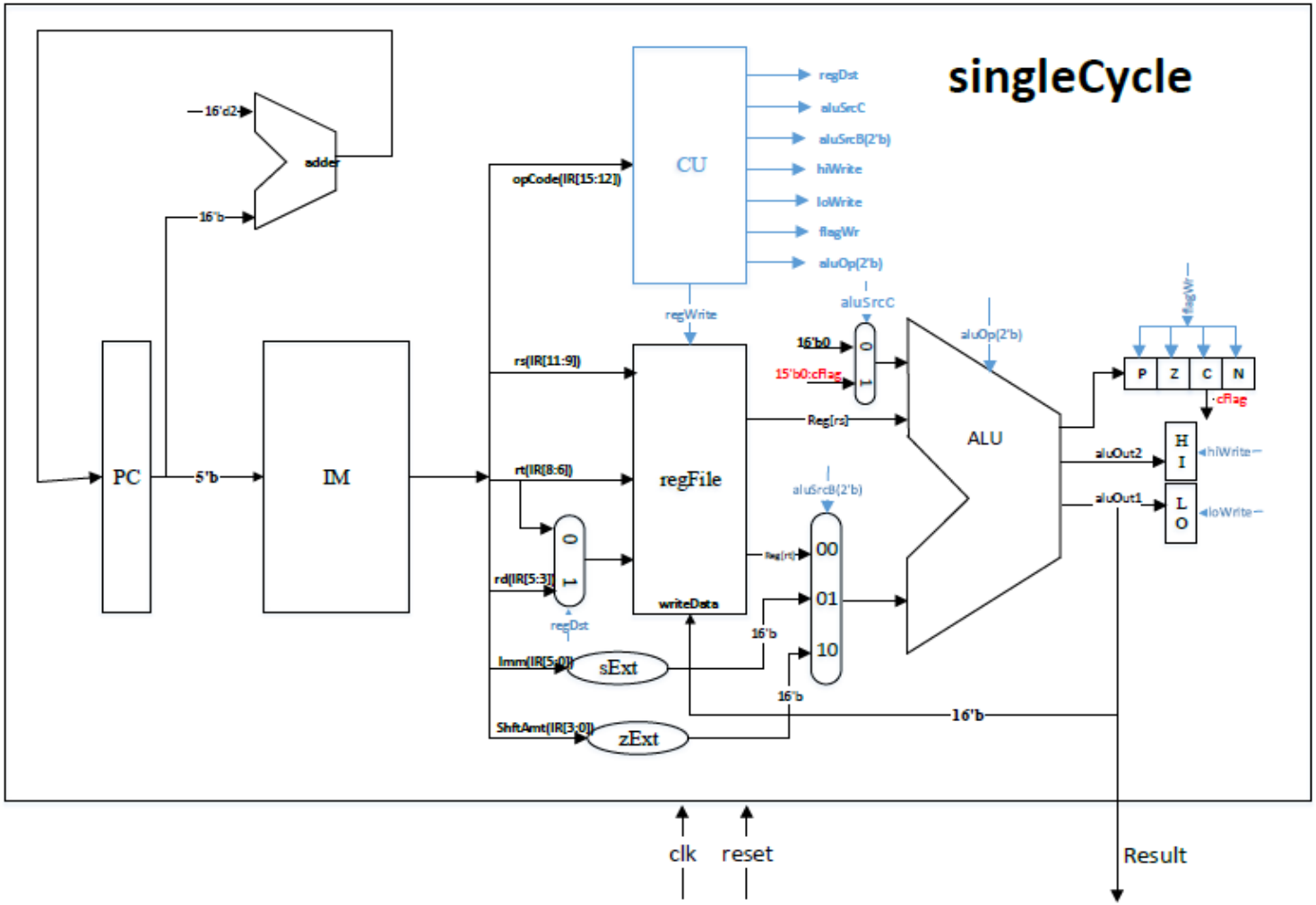
SINGLECYCLE ARCHITECTURE

The following design is implemented using verilog HDL in Xilinx 14.7 software.



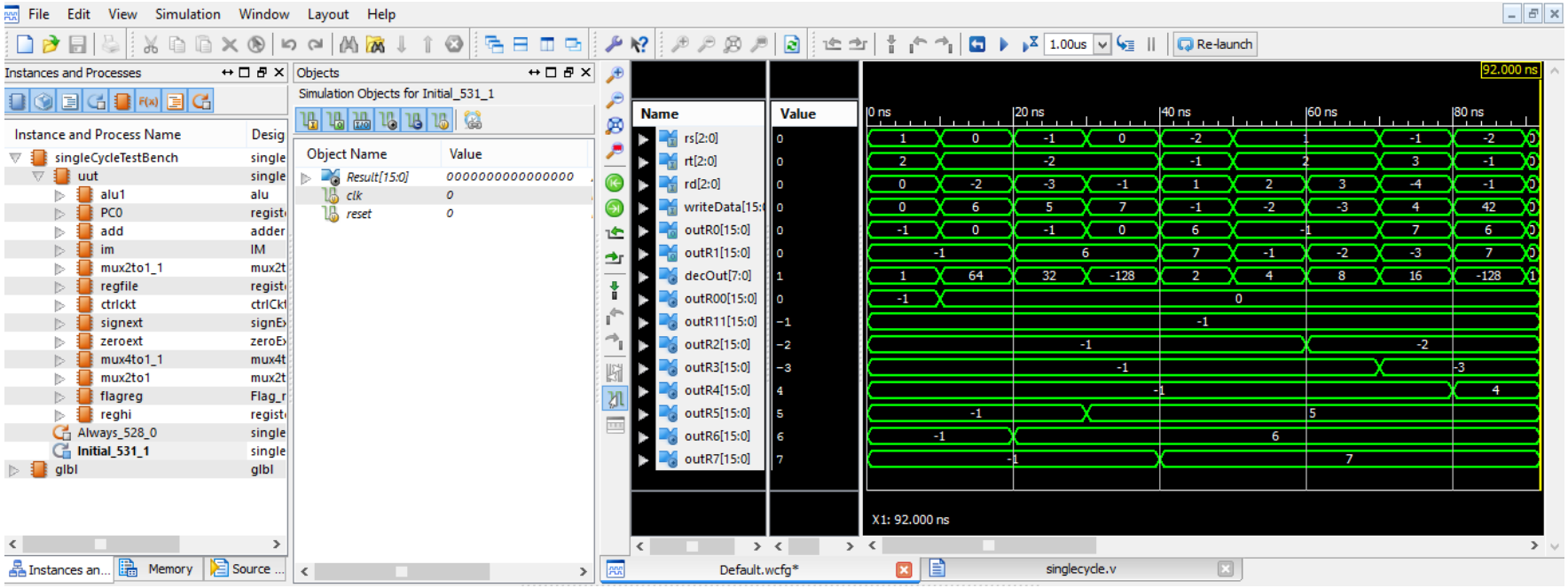
Instruction Format

Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
add	0	0	0	0	rs			rt			rd			X	X	X
sub	0	0	0	1	rs			rt			rd			X	X	X
addc	0	0	1	0	rs			rt			rd			X	X	X
addic	0	0	1	1	rs			rt			imm(6bits)					
shift	0	1	0	0	rs			rt			X	X	shiftAmt(4bits)			
mul	0	1	0	1	rs			rt			X	X	X	X	X	X

Control circuit

Instruction	Opcode				regWrite	regDst	aluSrcB(2b)	aluSrcC	aluOp(2b)	hiWrite	loWrite	flagWr
add	0	0	0	0	1	1	0	0	0	0	0	1
sub	0	0	0	1	1	1	0	0	1	0	0	1
addc	0	0	1	0	1	1	0	1	0	0	0	1
addic	0	0	1	1	1	0	1	1	0	0	0	1
shift	0	1	0	0	1	0	2	0	2	0	0	1
mul	0	1	0	1	0	0	0	0	3	1	1	0

WaveForm:


File Edit View Simulation Window Layout Help
Instances and Processes
Instance and Process Name
singleCycleTestBench
uut
alu1
PC0
add
im
mux2to1_1
regfile
ctrlckt
signext
zeroext
mux4to1_1
mux2to1
flagreg
reghi
Always_528_0
Initial_531_1
glbl
Objects
Simulation Objects for Initial_531_1
Object Name
Value
Result[15:0]
clk
reset
Name
Value
rs[2:0]
rt[2:0]
rd[2:0]
writeData[15:
outR0[15:0]
outR1[15:0]
decOut[7:0]
outR00[15:0]
outR11[15:0]
outR2[15:0]
outR3[15:0]
outR4[15:0]
outR5[15:0]
outR6[15:0]
outR7[15:0]
92.000 ns
0 ns
20 ns
40 ns
60 ns
80 ns
X1: 92.000 ns
Default.wcfg*
singlecycle.v