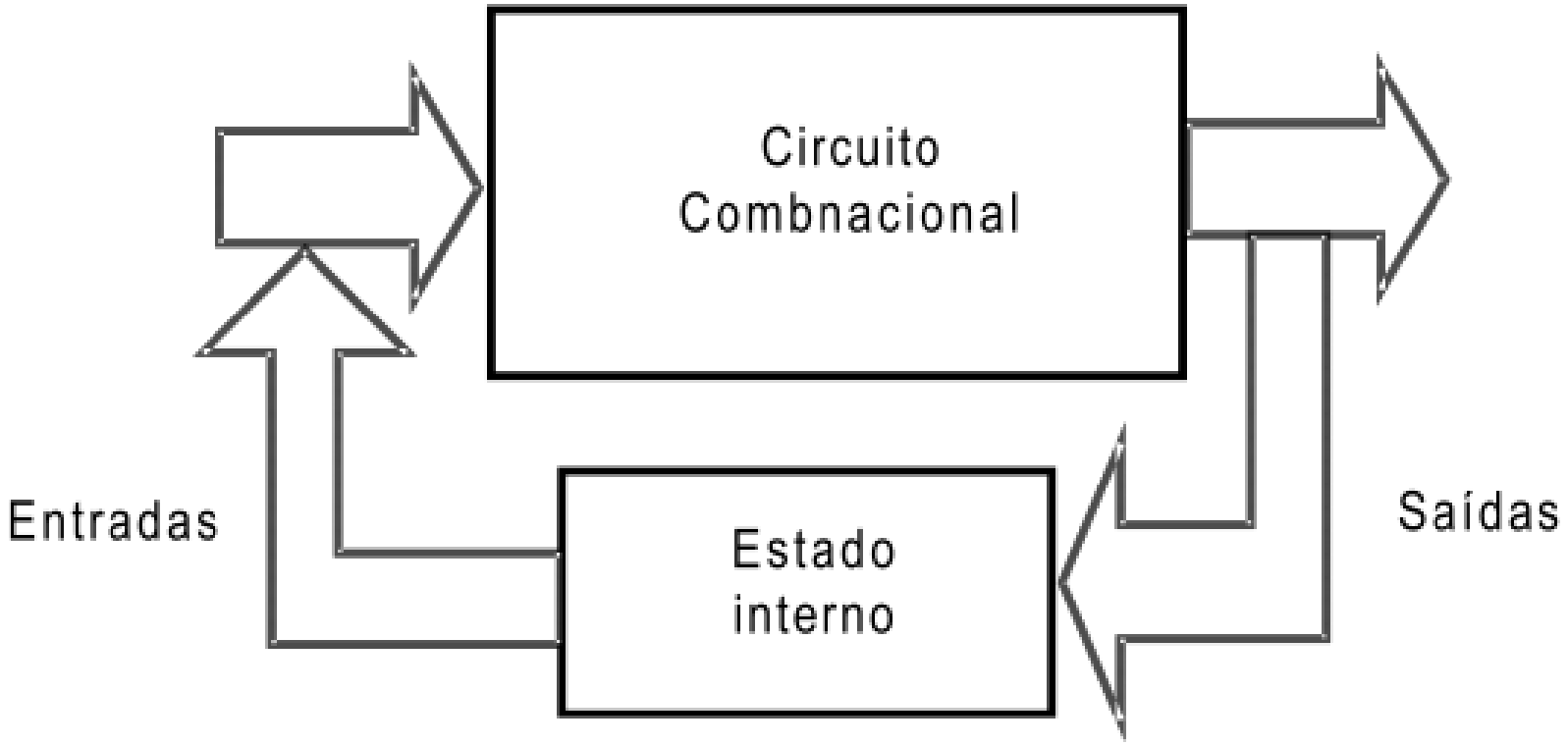
Circuitos Lógicos Sequenciais
Flip Flop

Prof. Rogério Moreira

CIRCUITO COMBINACIONAL

CIRCUITO SEQUENCIAL



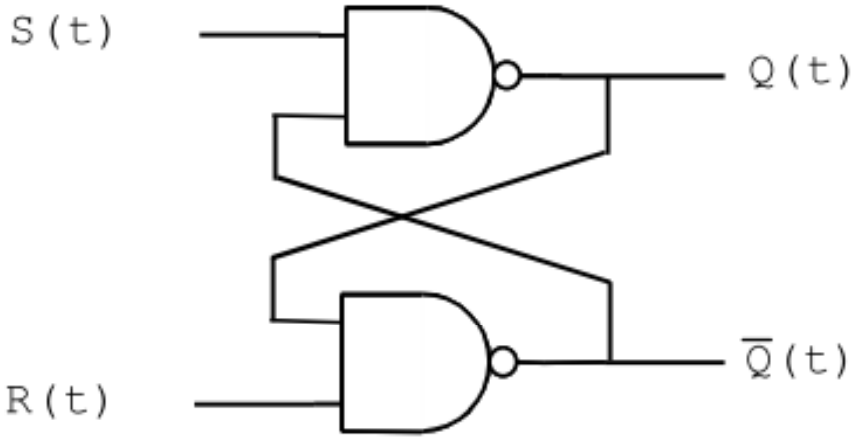
FLIP-FLOPS

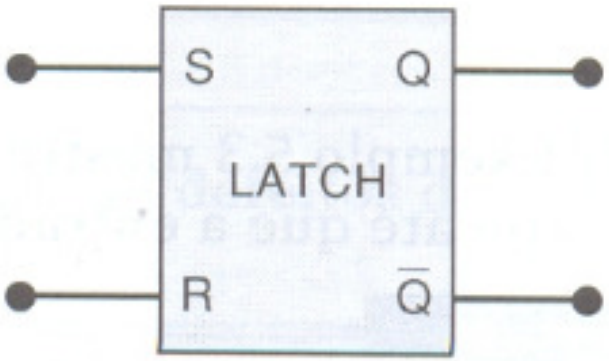
Os flip-flops são os circuitos seqüenciais mais elementares e possuem a capacidade de armazenar a informação neles contida. Representam a unidade elementar de memória de 1 bit (binary digit), ou seja, funcionam como um elemento de memória por armazenar níveis lógicos temporariamente. São chamados de biestáveis porque possuem dois estados lógicos estáveis, geralmente representados por “0” e “1”.

TIPOS DE FLIP-FLOPS

1) RS ASSÍNCRONO
2) RS SÍNCRONO
3) JK (síncrono)
4) JK com entradas assíncronas
5) JK Mestre-Escravo
6) T
7) D

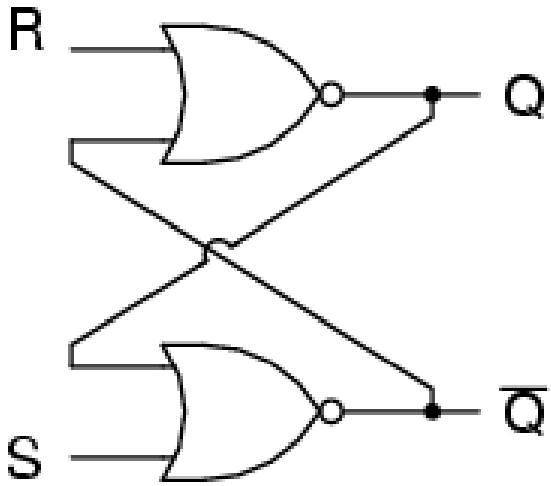
FLIP-FLOP RS ASSÍNCRONO



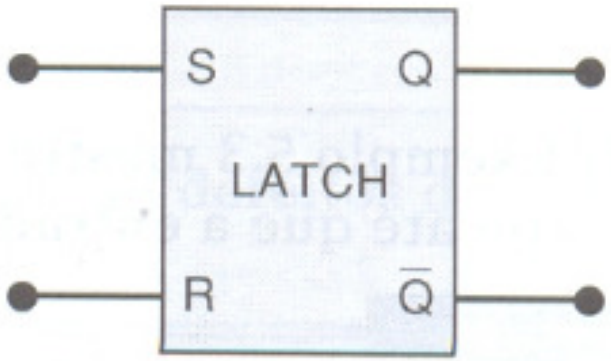


S	R	Q
0	0	Qa
0	1	0
1	0	1
1	1	X

FLIP-FLOP RS ASSÍNCRONO



S	R	Q
0	0	Qa
0	1	0
1	0	1
1	1	X



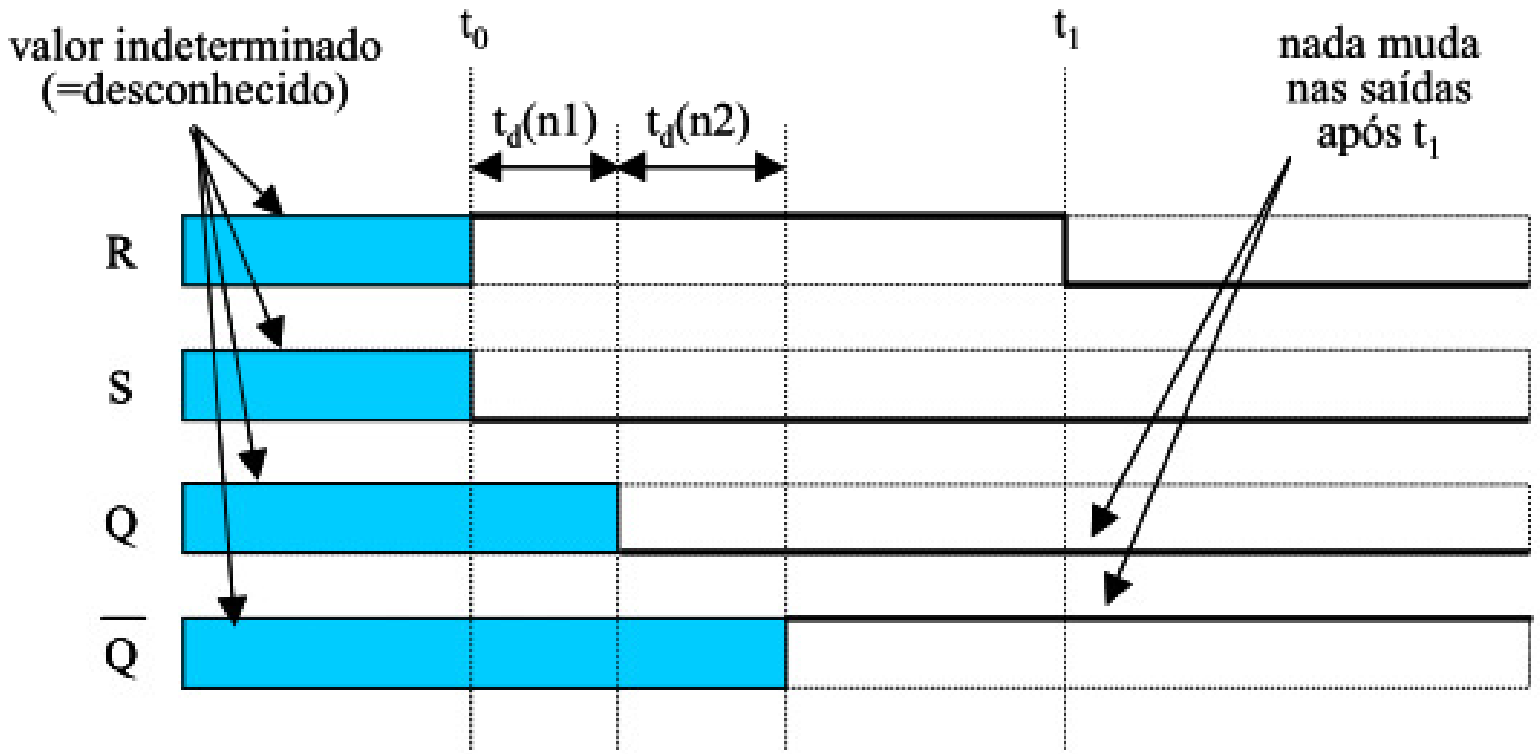


Figura 4.5 -Formas de onda para aplicação do vetor de entrada (R=1;S=0) seguido do vetor (R=0;S=0) no latch RS.

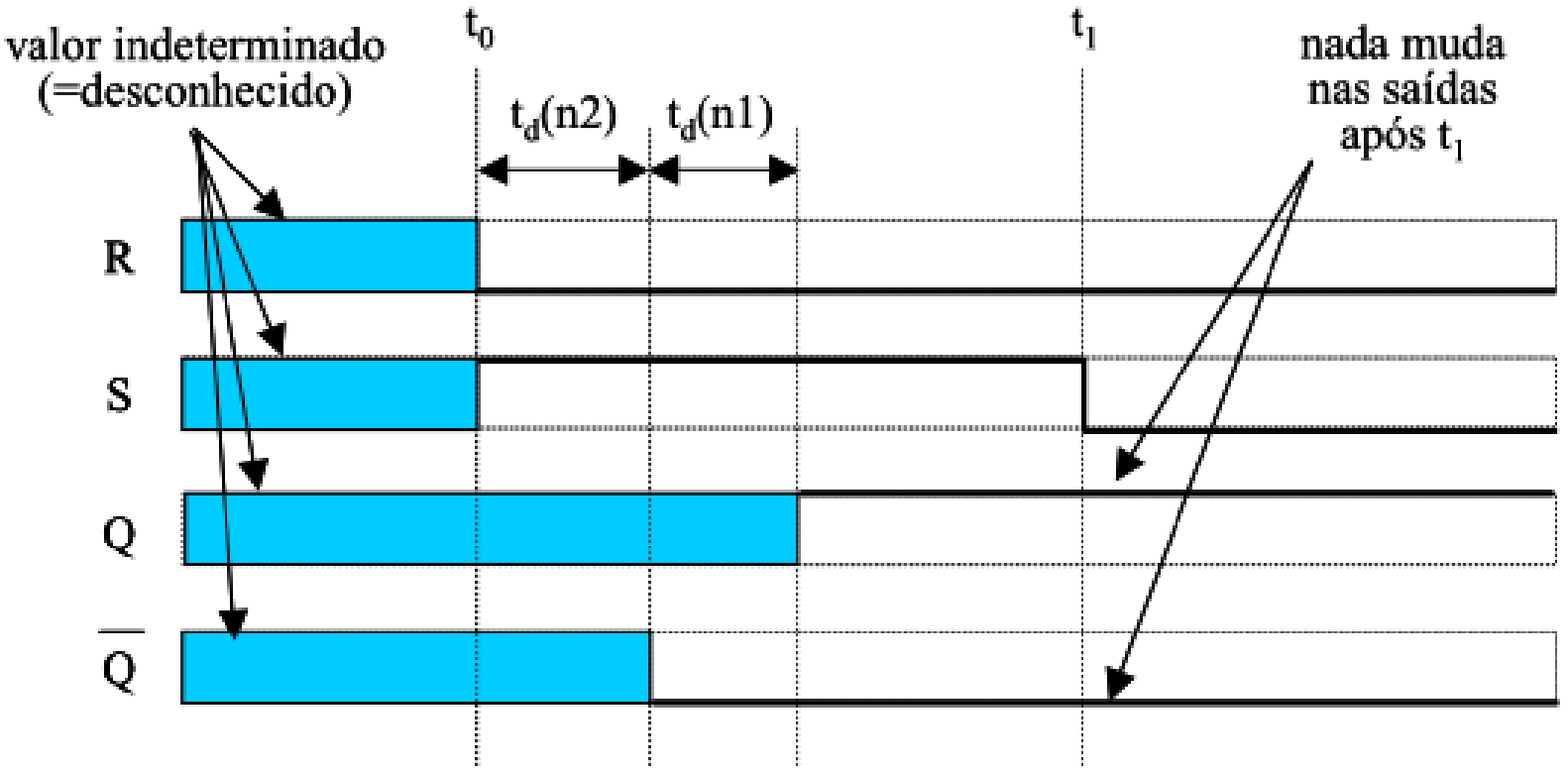


Figura 4.6 -Formas de onda para aplicação do vetor de entrada (R=0;S=1) seguido do vetor (R=0;S=0) no latch RS.

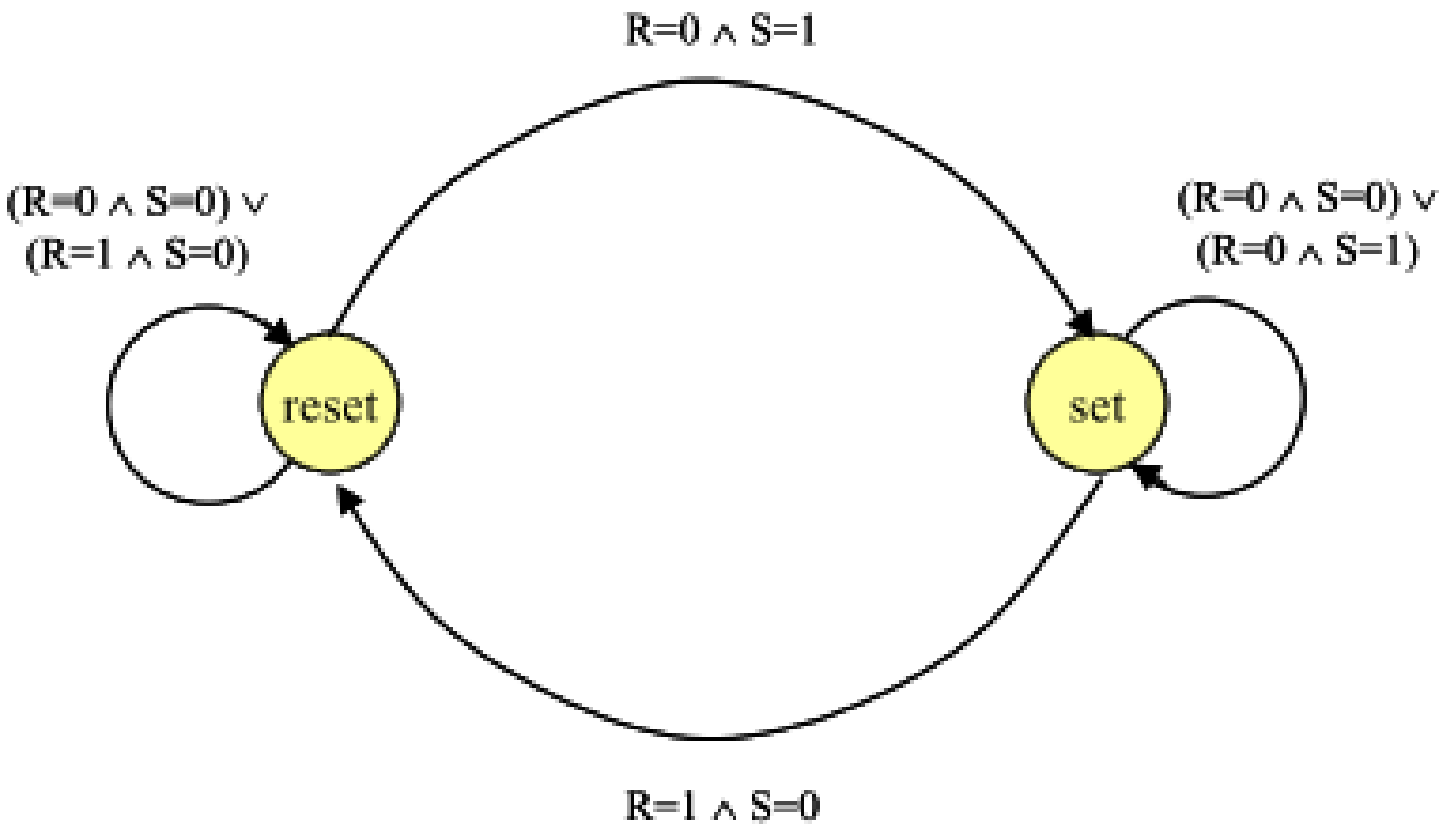
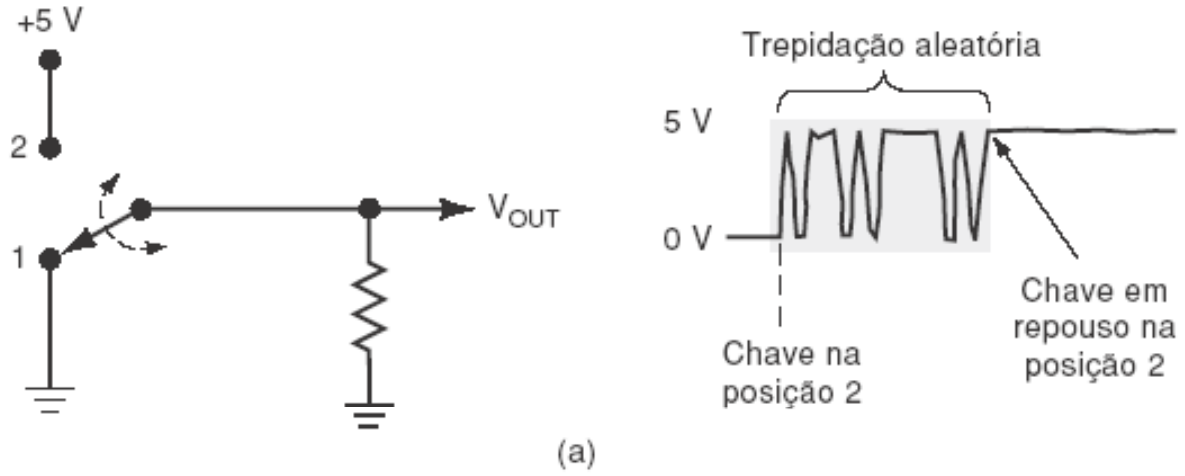


Figura 4.7 - Diagrama de estados para o latch RS.

Exemplo de aplicação



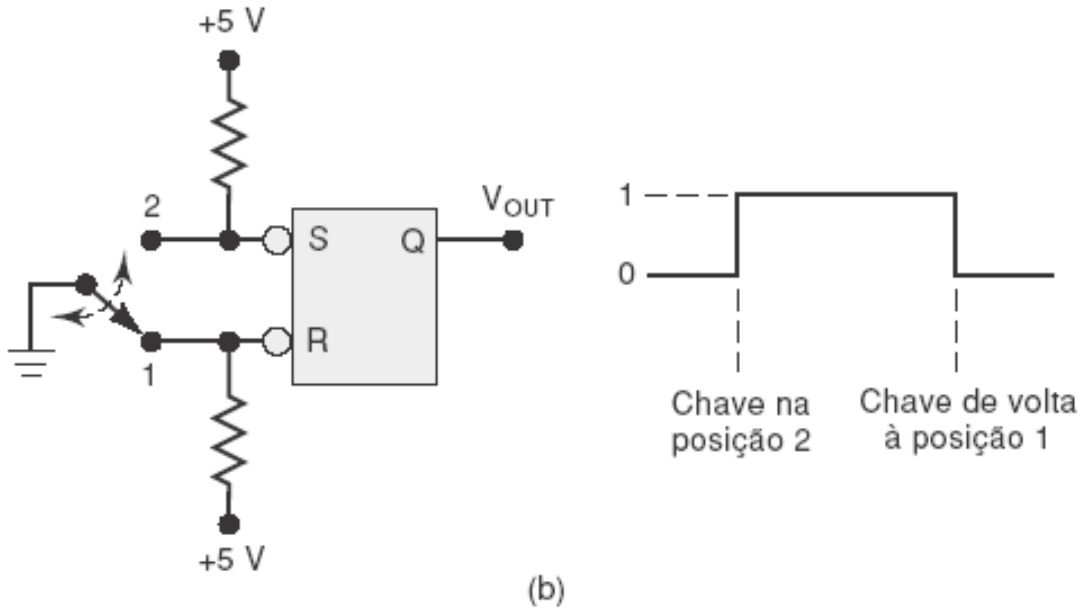
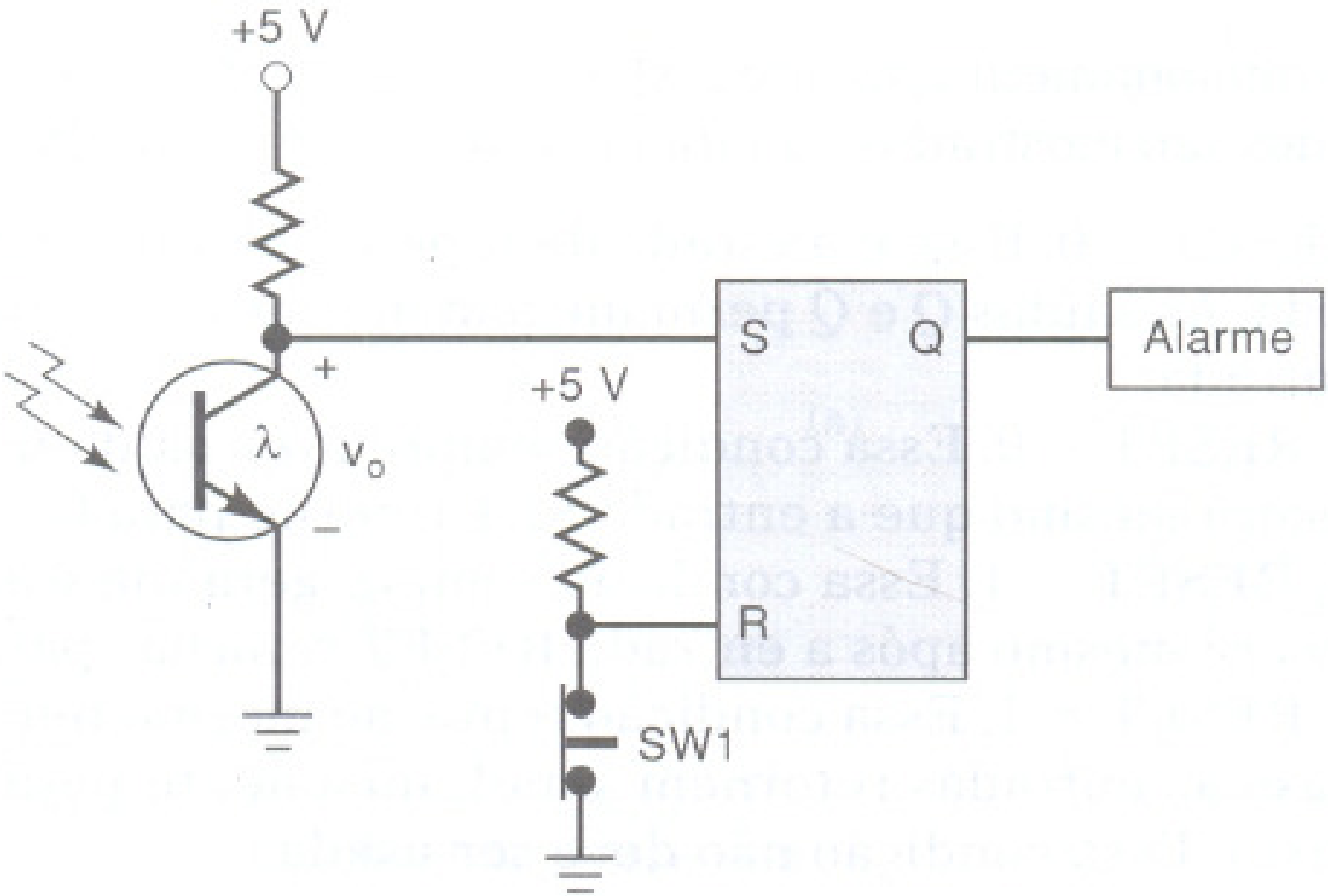
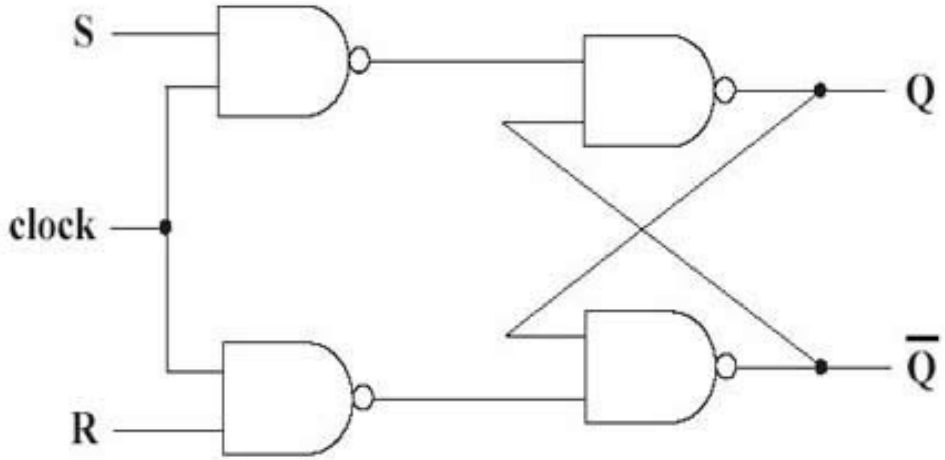


FIGURA 5.9
(a) A trepidação de um contato mecânico gera múltiplas transições na tensão; (b) latch NAND usado para eliminar as múltiplas transições na tensão.

Exemplo de aplicação



FLIP-FLOP RS SÍNCRONO



C	R	S	Q_{t+1}	comentário
0	X	X	Q_t	mantém estado anterior
1	0	0	Q_t	mantém estado anterior
1	0	1	1	estado set
1	1	0	0	estado reset
1	1	1	-	proibido

FLIP-FLOP RS SÍNCRONO

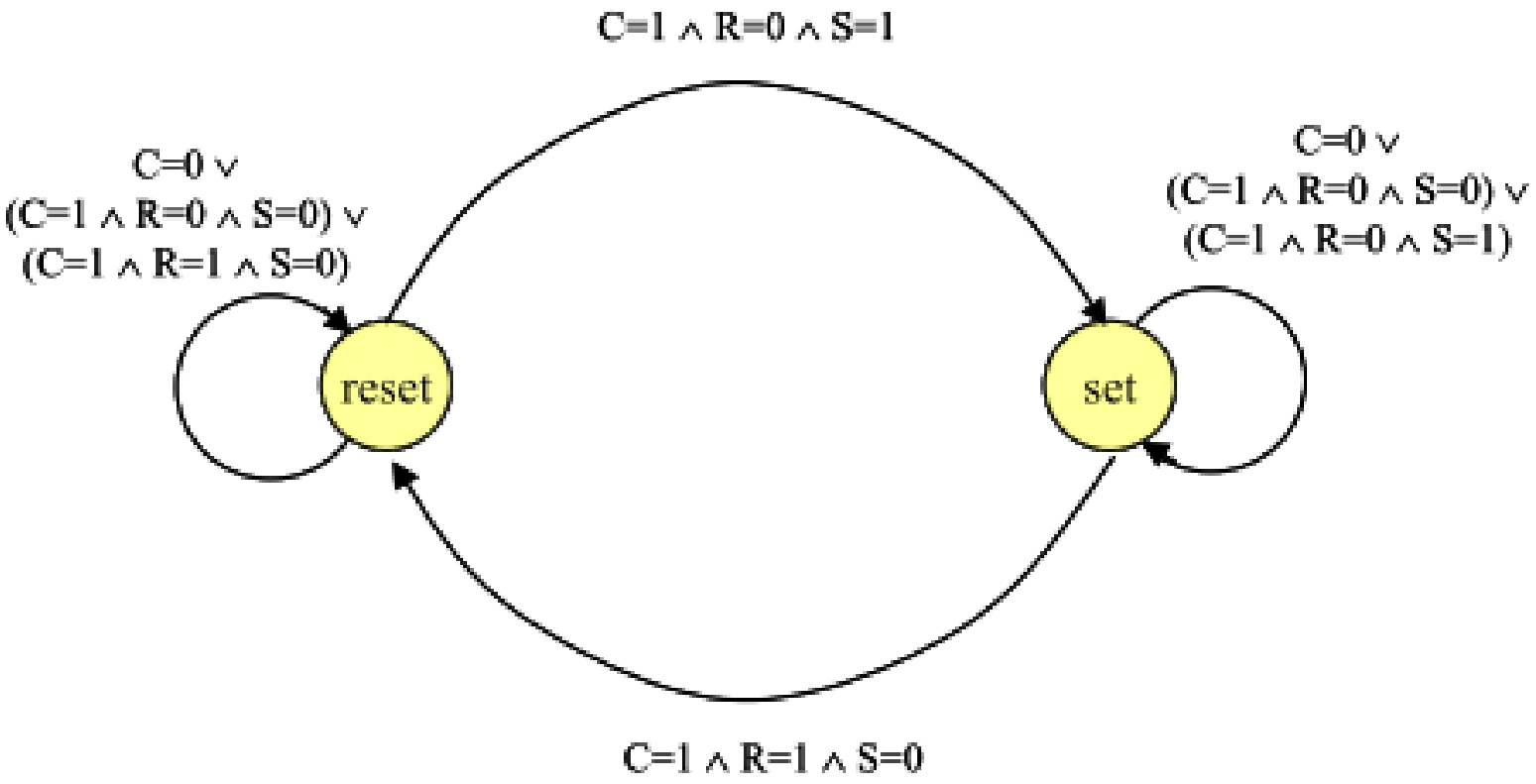
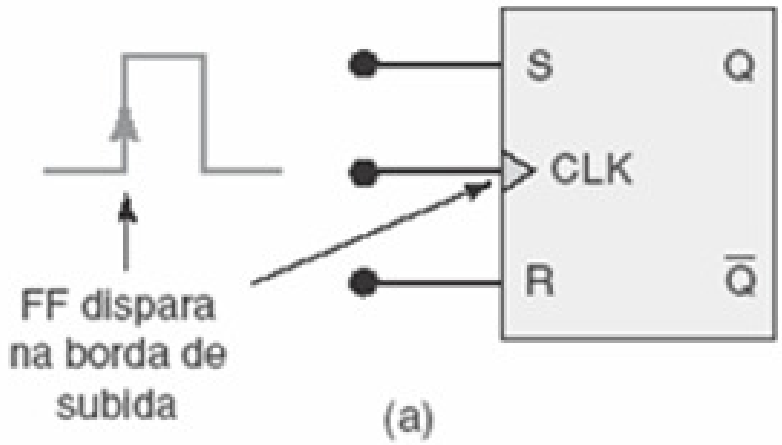


Figura 4.10 -Diagrama de estados para o latch RS controlado.

FLIP-FLOP RS SÍNCRONO



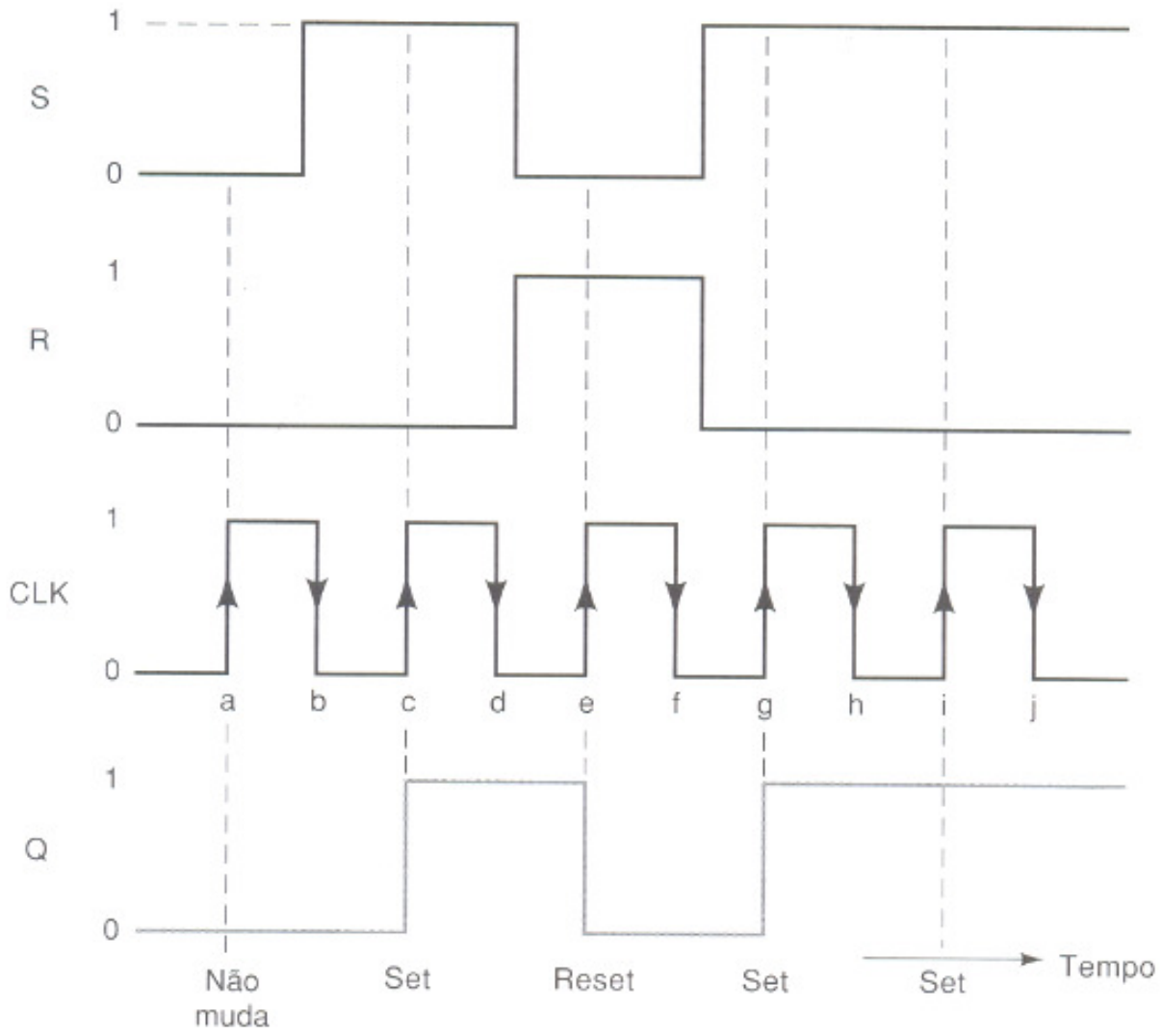
(a)

Entradas			Saída
S	R	CLK	Q
0	0	↑	Q_0 (Não muda)
1	0	↑	1
0	1	↑	0
1	1	↑	Ambíguo

Q_0 é o nível de saída anterior a ↑ de CLK.
↓ de CLK não produz mudança em Q.

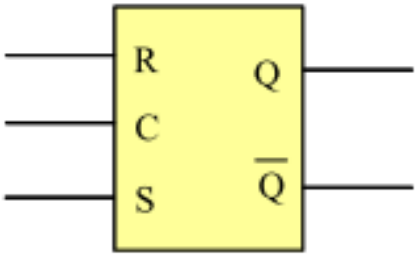
(b)

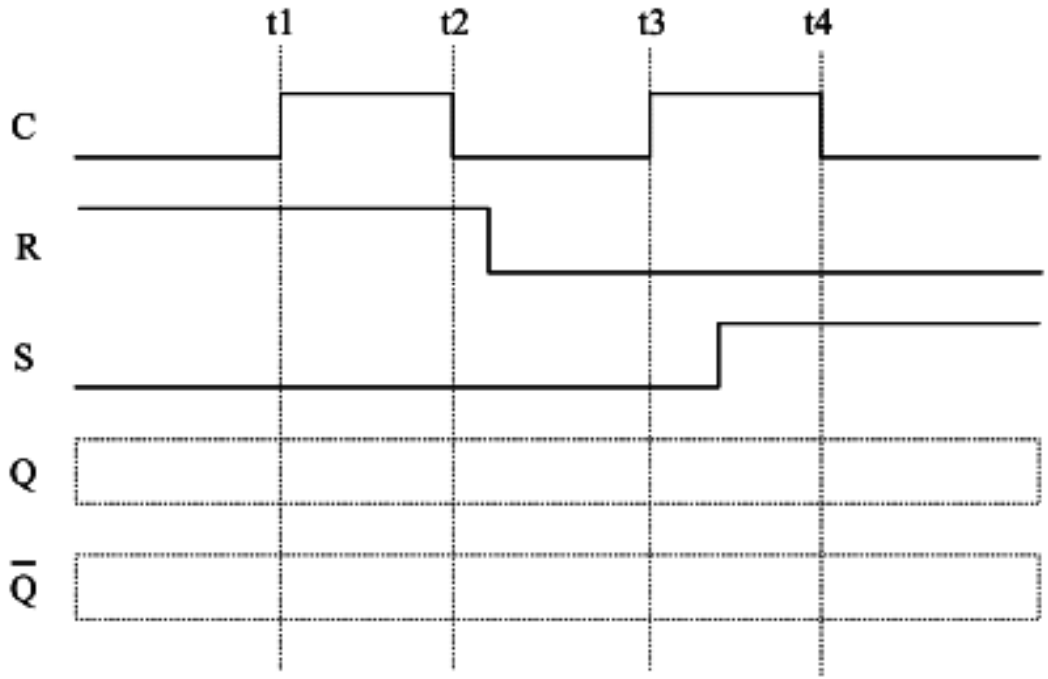
FLIP-FLOP RS SÍNCRONO



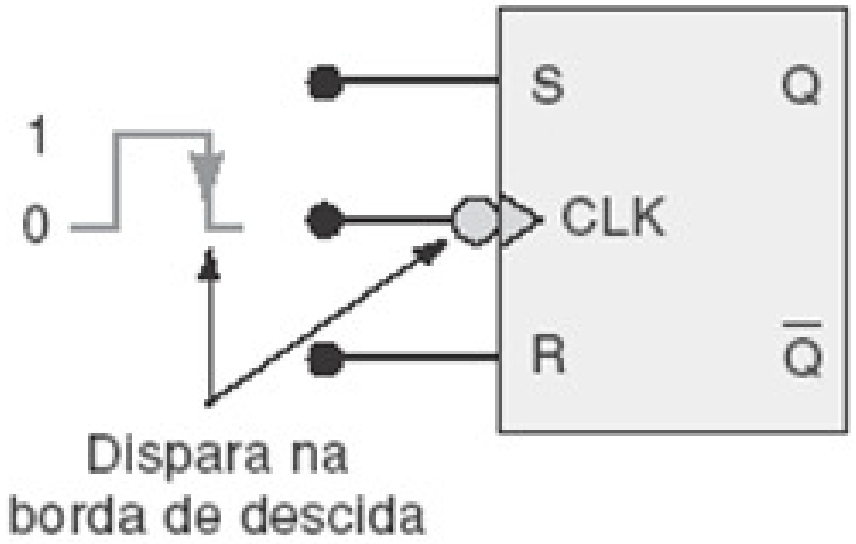
FLIP-FLOP RS SÍNCRONO

Exemplo 4.3: desenhar as formas de onda para as saídas do latch RS abaixo, a partir das formas de onda fornecidas para as entradas C, R e S.



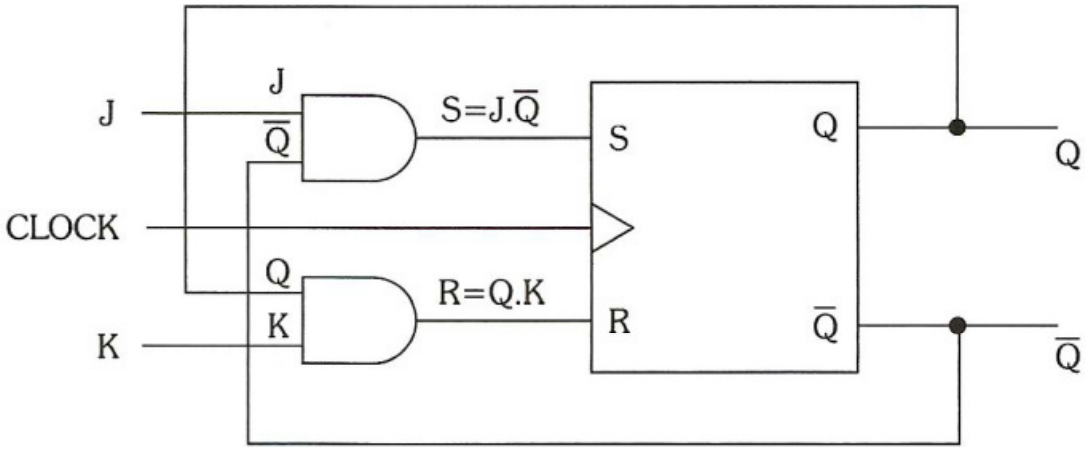


FLIP-FLOP RS SÍNCRONO



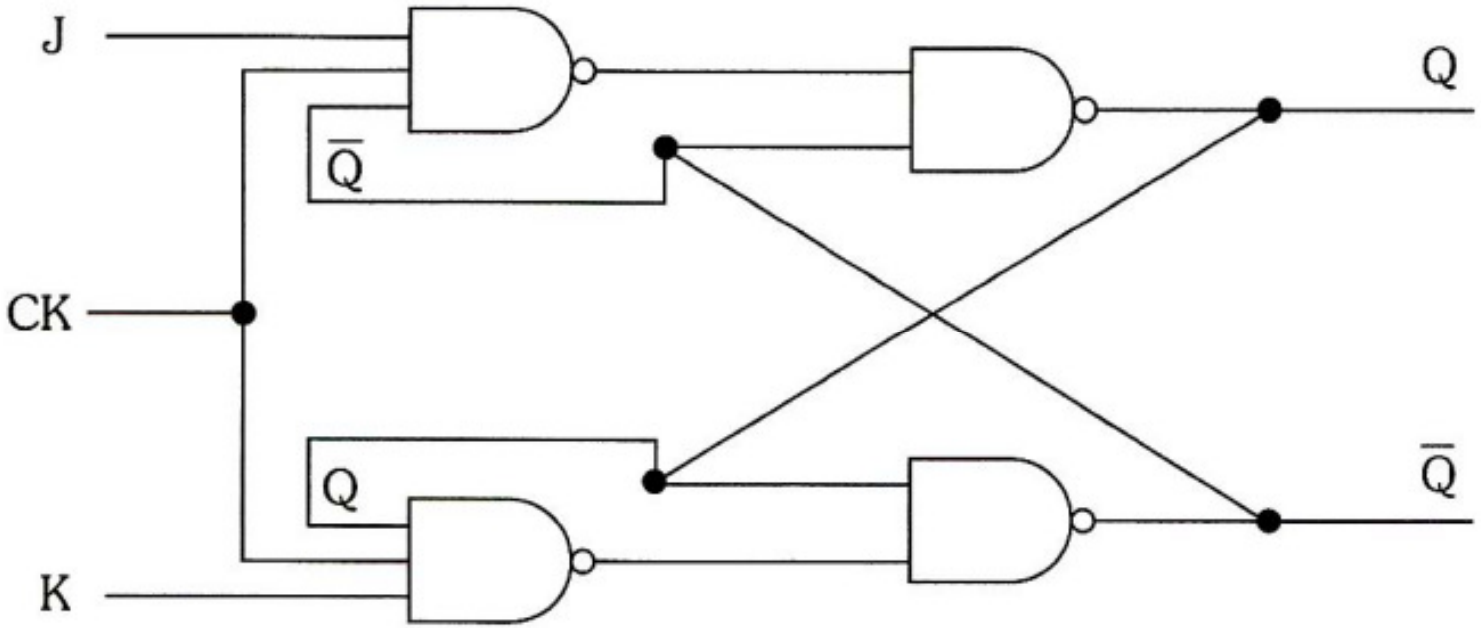
Entradas			Saída
S	R	CLK	Q
0	0	↓	Q_0 (não muda)
1	0	↓	1
0	1	↓	0
1	1	↓	Ambíguo

FLIP-FLOP JK

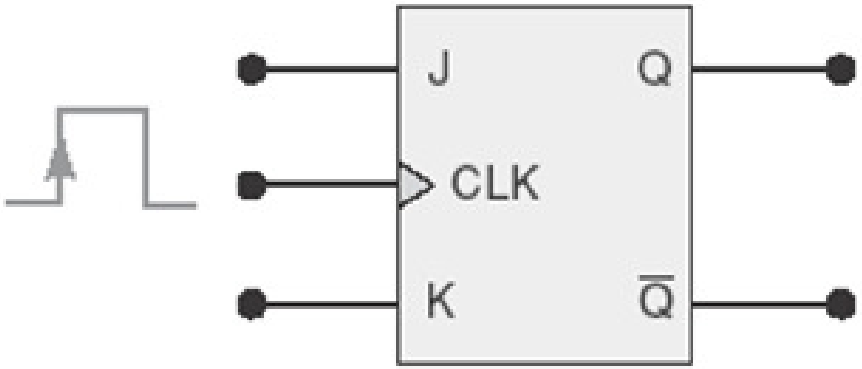


J	K	Qf
0	0	Qa
0	1	0
1	0	1
1	1	$\overline{Q}$a

FLIP-FLOP JK



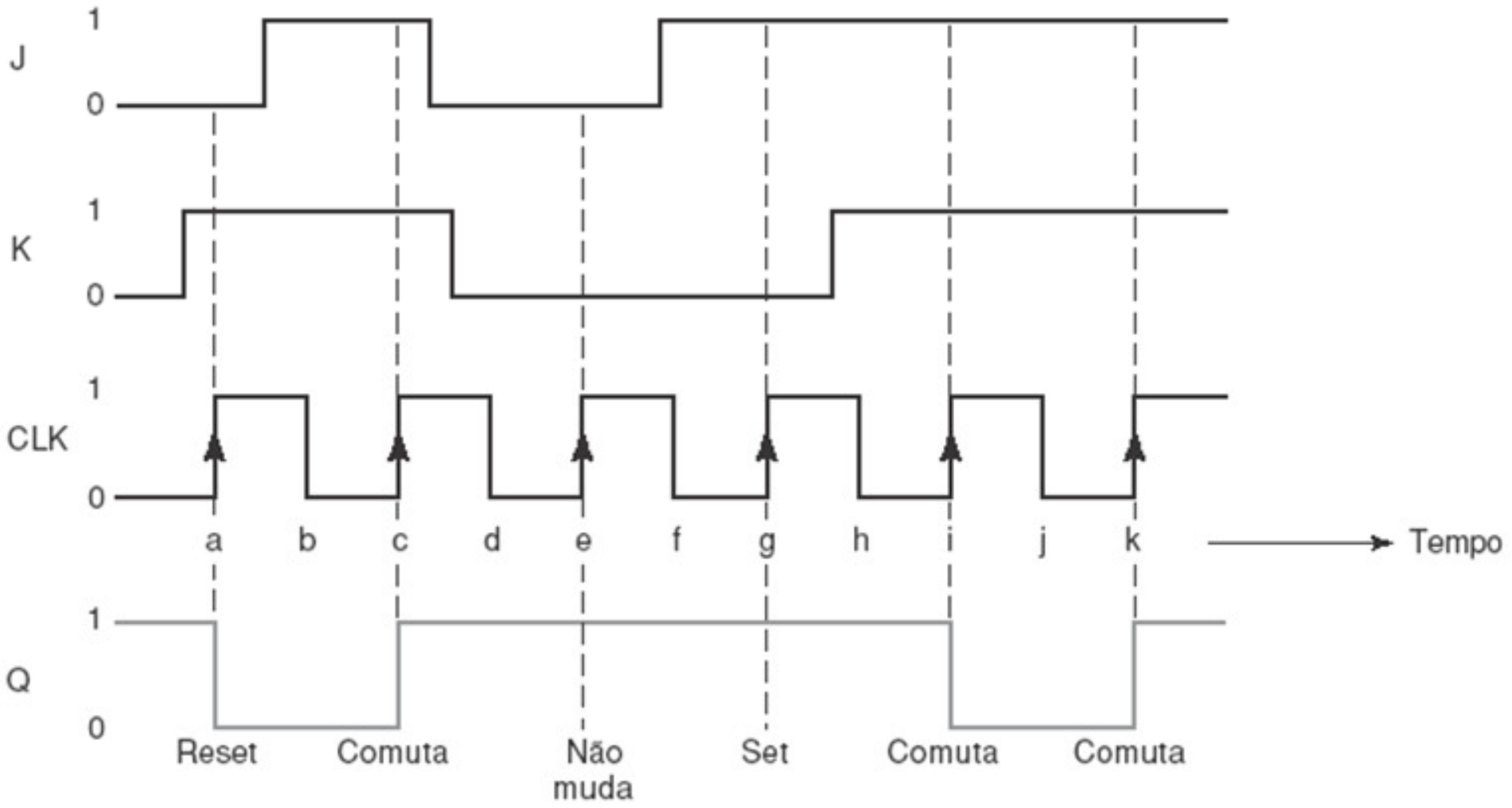
FLIP-FLOP JK



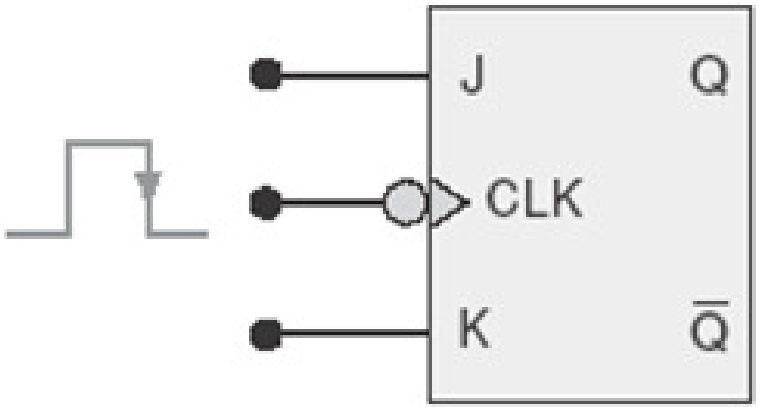
J	K	CLK	Q
0	0	↑	Q_0 (não muda)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q_0}$ (comuta)

(a)

FLIP-FLOP JK

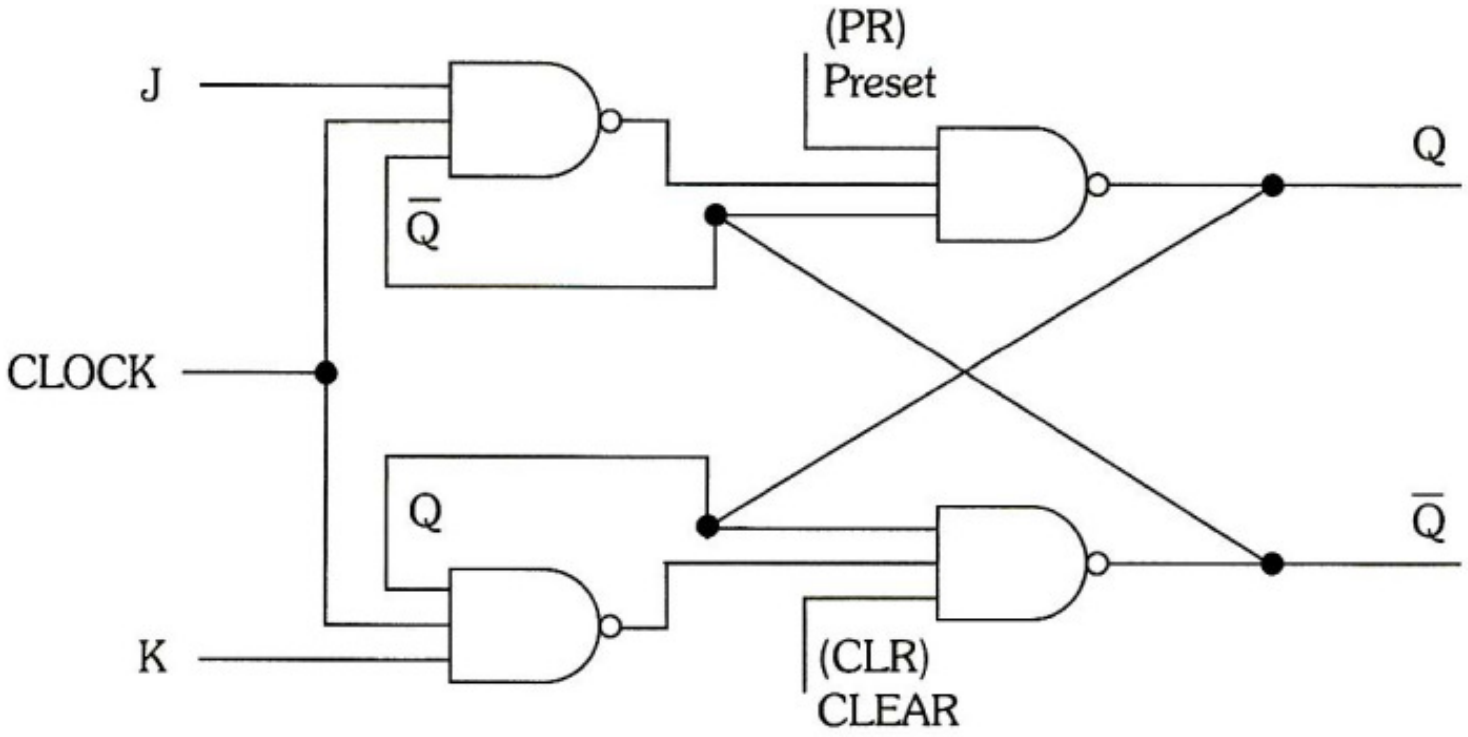

J
K
CLK
Q
1
0
a
b
c
d
e
f
g
h
i
j
k
Tempo
Reset
Comuta
Não muda
Set
Comuta
Comuta

FLIP-FLOP JK

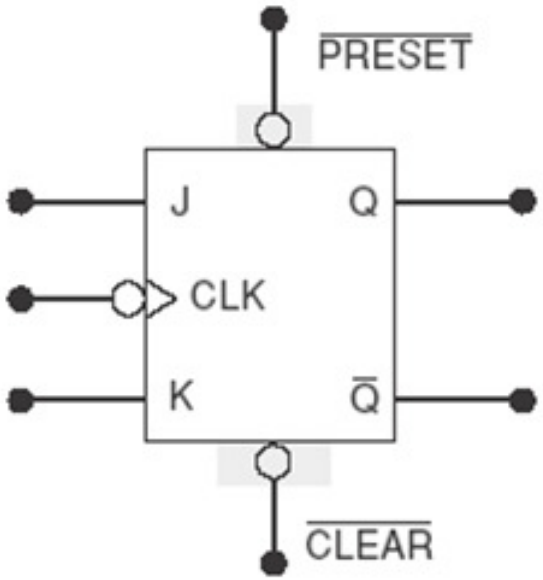


J	K	CLK	Q
0	0	↓	Q_0 (não muda)
1	0	↓	1
0	1	↓	0
1	1	↓	$\overline{Q_0}$ (comuta)

FLIP-FLOP JK com Entradas Assíncronas

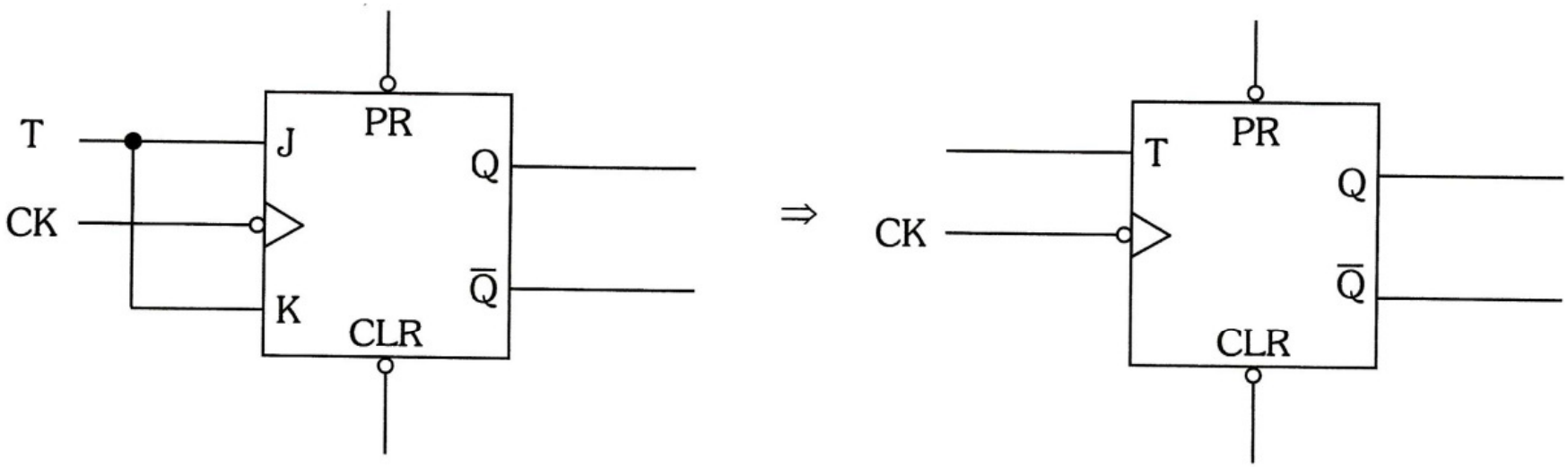


FLIP-FLOP JK com Entradas Assíncronas



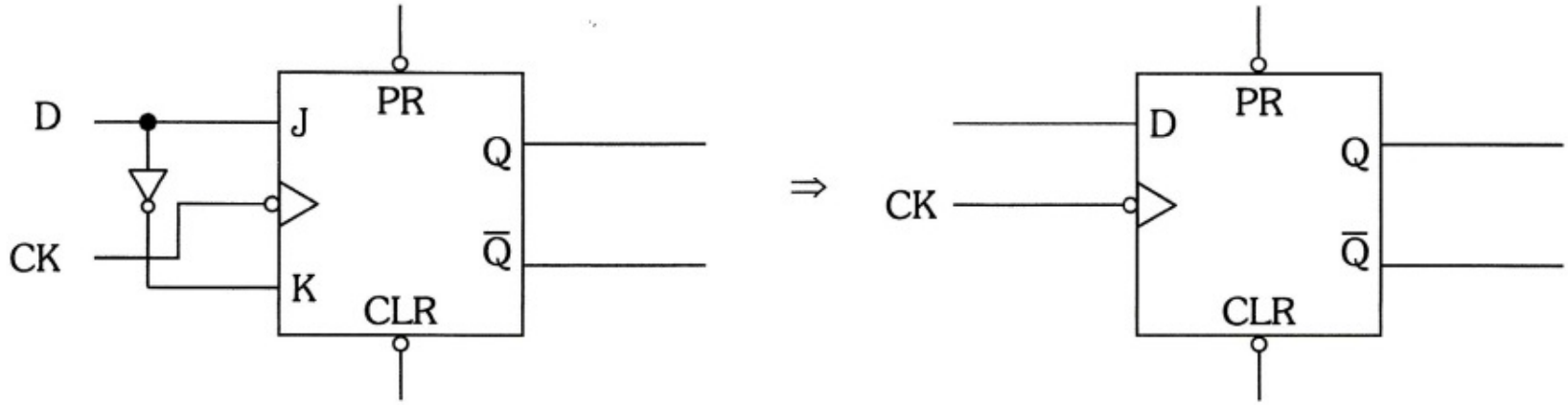
J	K	CLK	$\overline{PRE}$	$\overline{CLR}$	Q
0	0	↓	1	1	Q (não muda)
0	1	↓	1	1	0 (reset síncrono)
1	0	↓	1	1	1 (set síncrono)
1	1	↓	1	1	$\overline{Q}$ (toggle síncrono ou comutação síncrona)
x	x	x	1	1	Q (não muda)
x	x	x	1	0	0 (clear assíncrono)
x	x	x	0	1	1 (preset assíncrono)
x	x	x	0	0	(Inválido)

FLIP-FLOP TIPO T (TOGGLE)



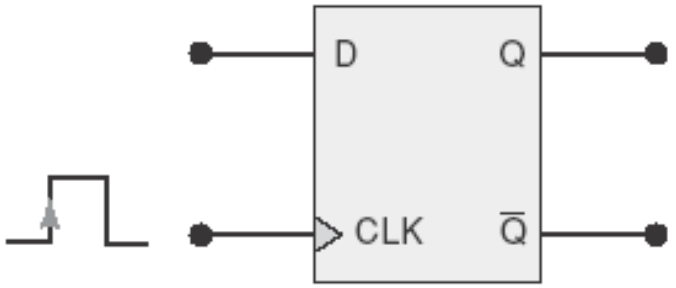
J	K	T	Qf
0	0	0	Qa
0	1	não existe	/
1	0	não existe	/
1	1	1	$\overline{Q}$a

FLIP-FLOP TIPO D (DATA ou DELAY)



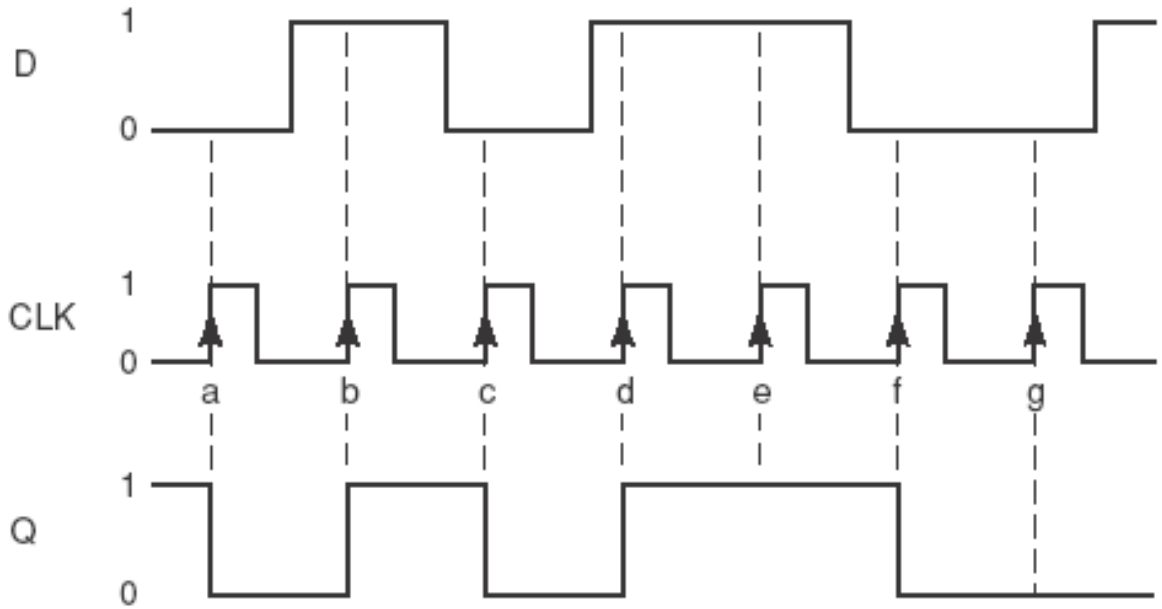
J	K	D	Qf
0	0	não existe	/
0	1	0	0
1	0	1	1
1	1	não existe	/

FLIP-FLOP TIPO D



(a)

D	CLK	Q
0	↑	0
1	↑	1

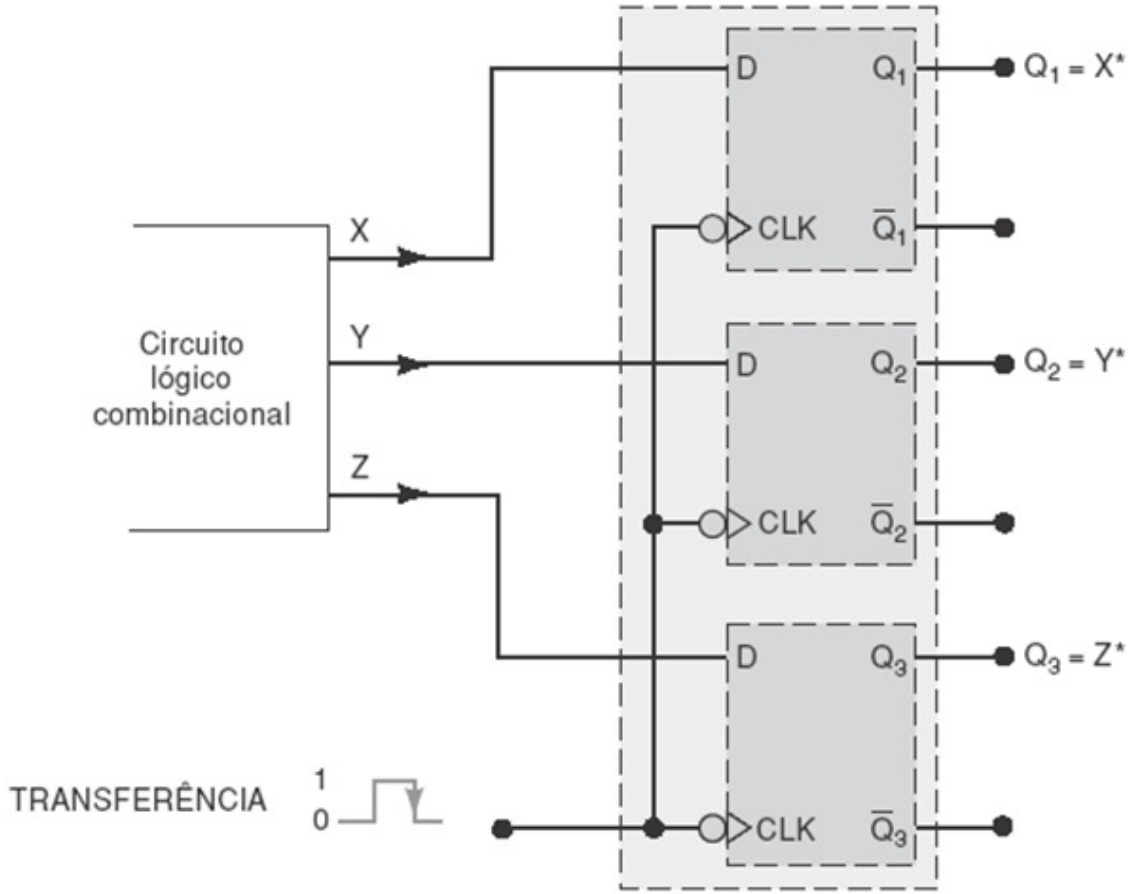


(b)

FIGURA 5.26
(a) Flip-flop *D* disparado apenas nas bordas de subida do clock; (b) Formas de onda.

Aplicações

- Transferência simultânea de dados em paralelo



Aplicações

- Garantia de pulsos completos

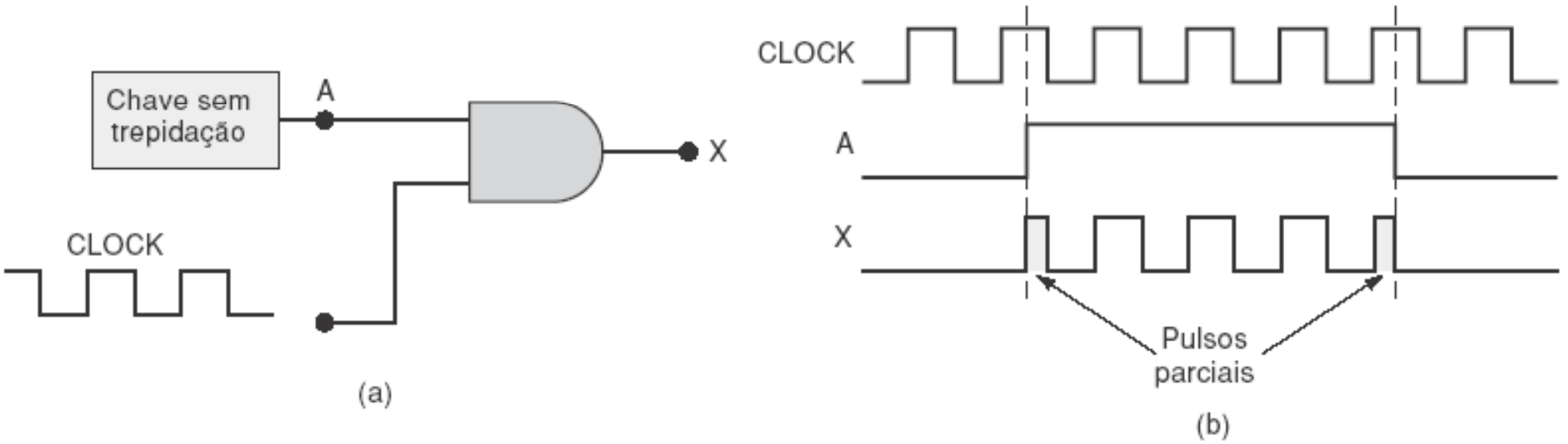


FIGURA 5.39
Um sinal assíncrono em *A* pode produzir pulsos parciais em *X*.

Aplicações

- Garantia de pulsos completos

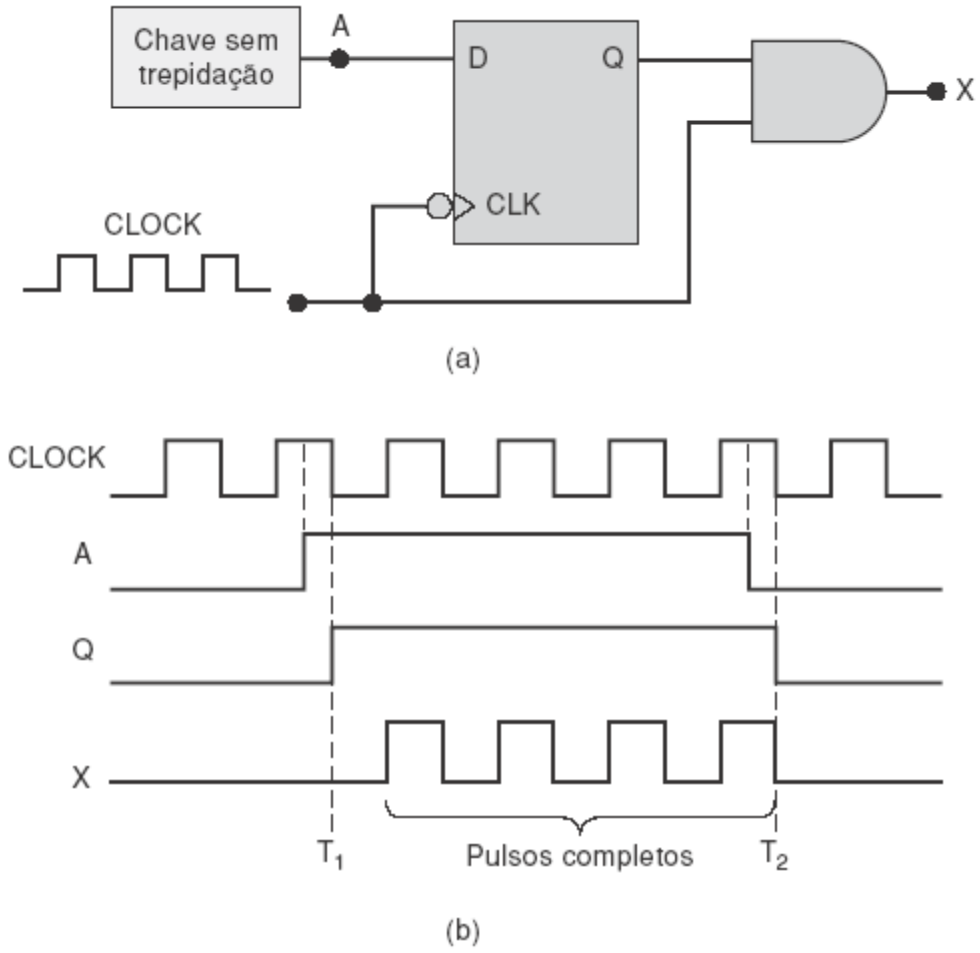
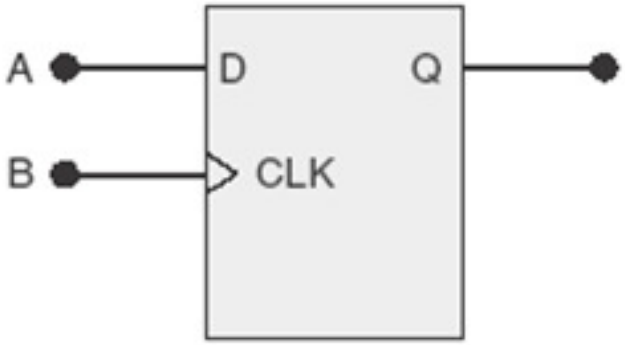


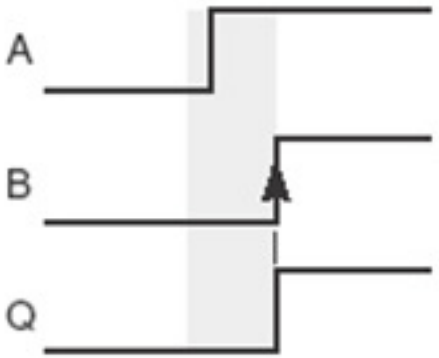
FIGURA 5.40
Um flip-flop *D* disparado por borda é usado para sincronizar a habilitação da porta AND com a borda de descida do clock.

Aplicações

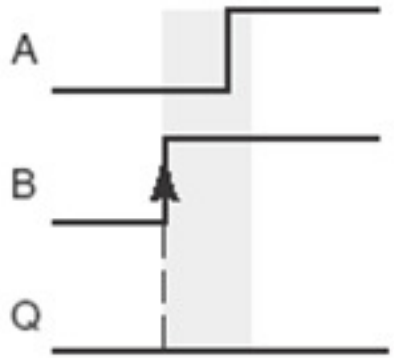
- Detectando sequencia de entrada
  - Garantindo que saída Y só irá para nível lógico alto se A for acionado antes de B.



(a)



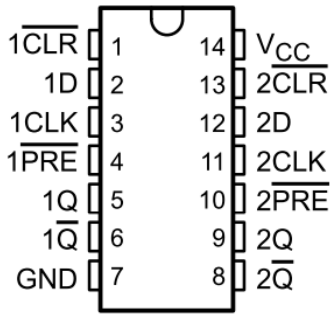
(b) chega no nível ALTO antes de B



(c) B chega no nível ALTO antes de A

FLIP-FLOP TIPO D EM CI

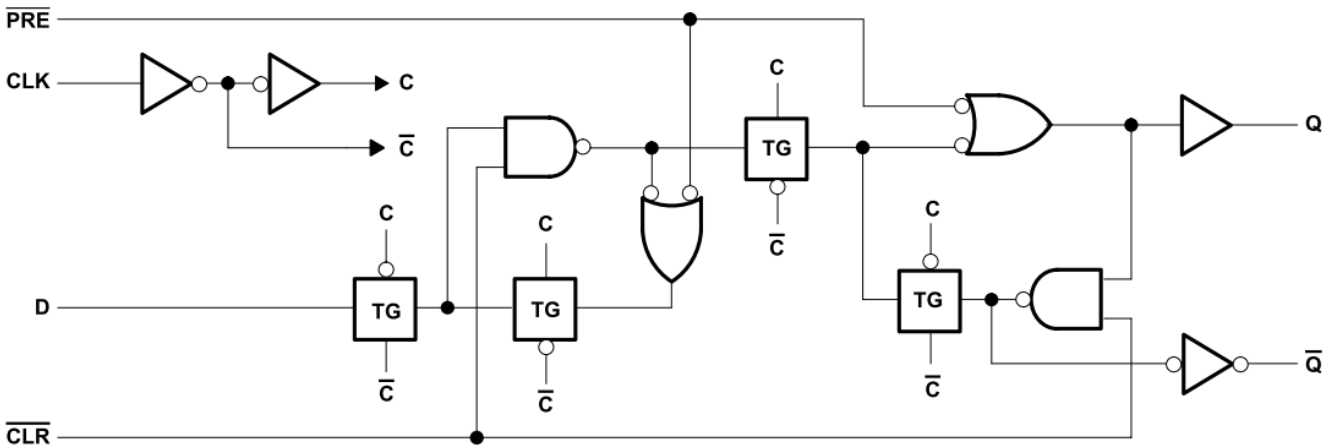
SN54HC74 . . . J OR W PACKAGE
SN74HC74 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



FUNCTION TABLE

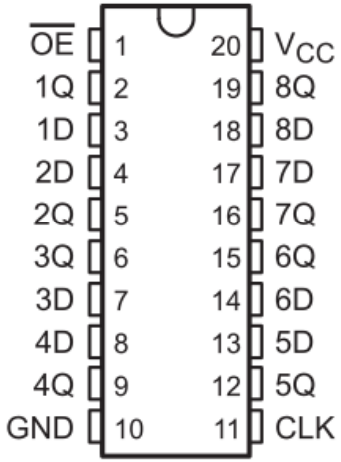
INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.



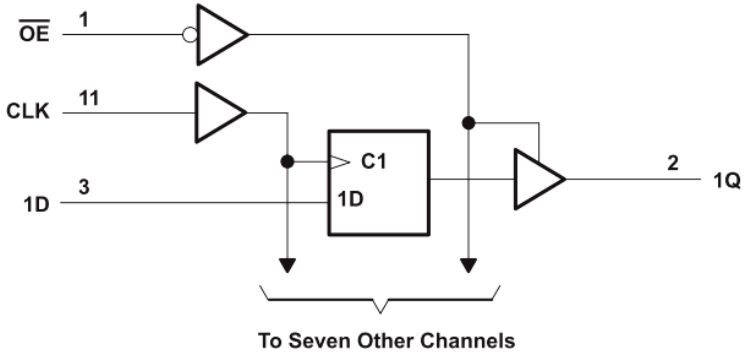
FLIP-FLOP TIPO D EM CI

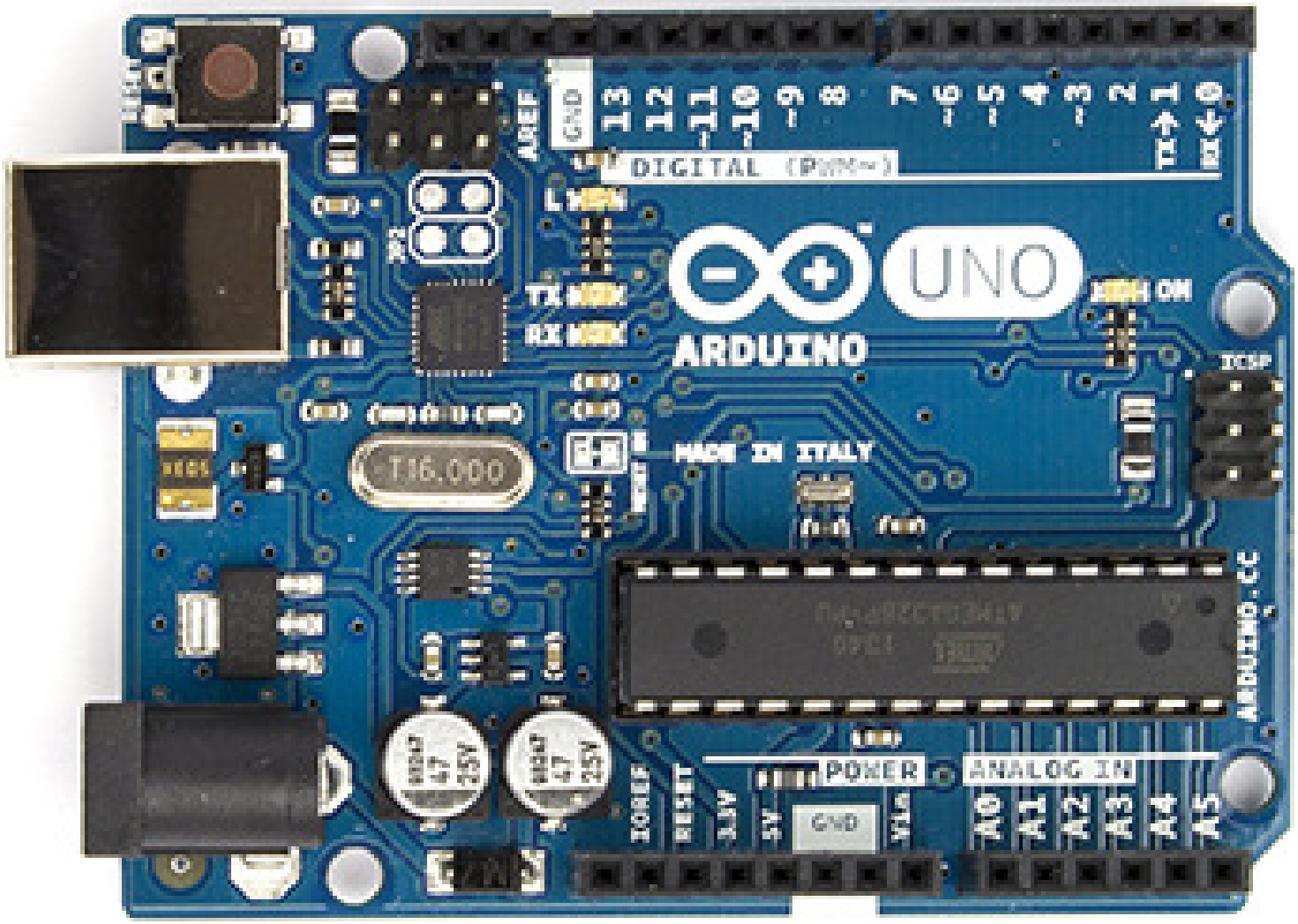
SN54HC374 . . . J OR W PACKAGE
SN74HC374 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

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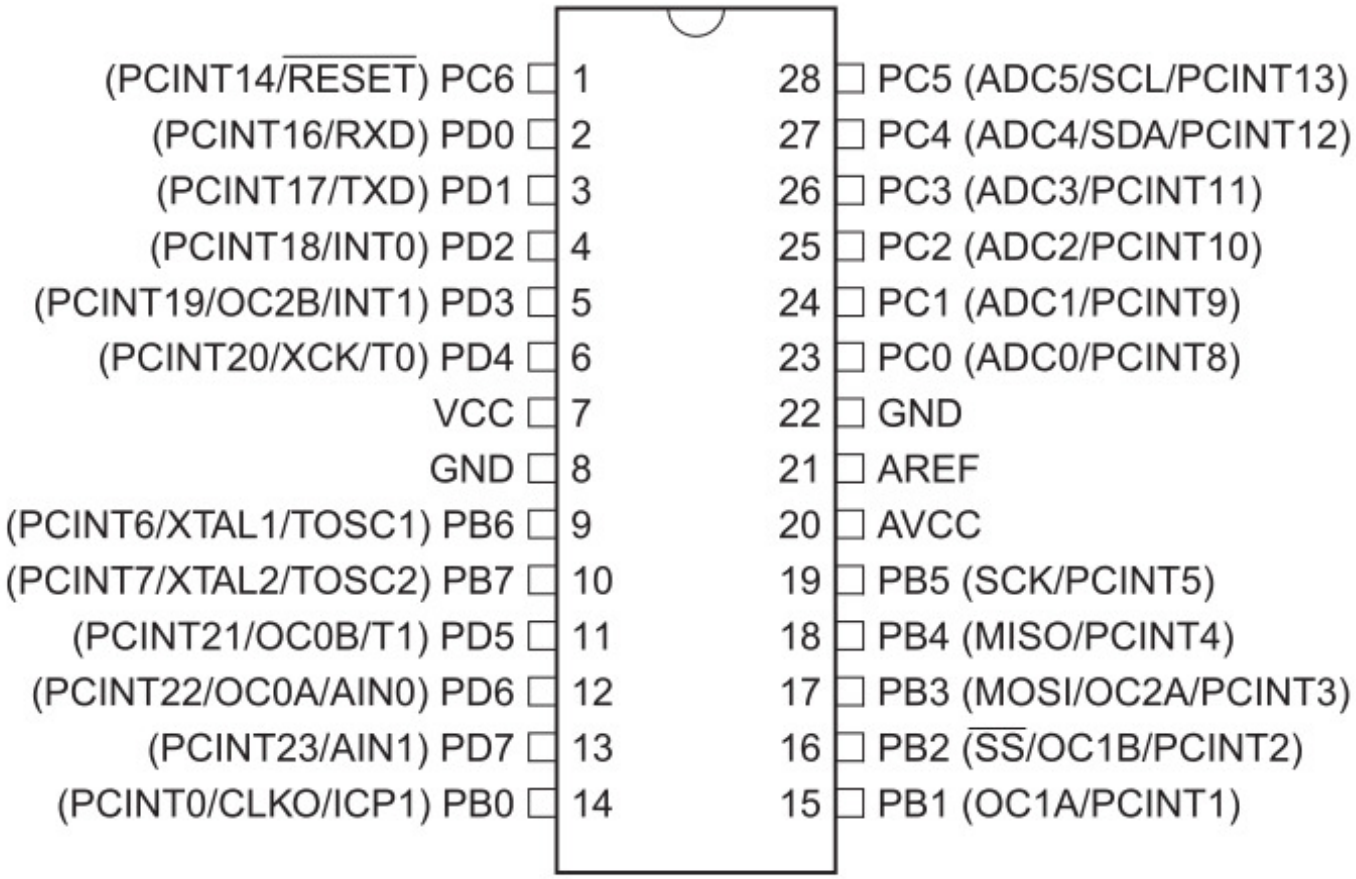
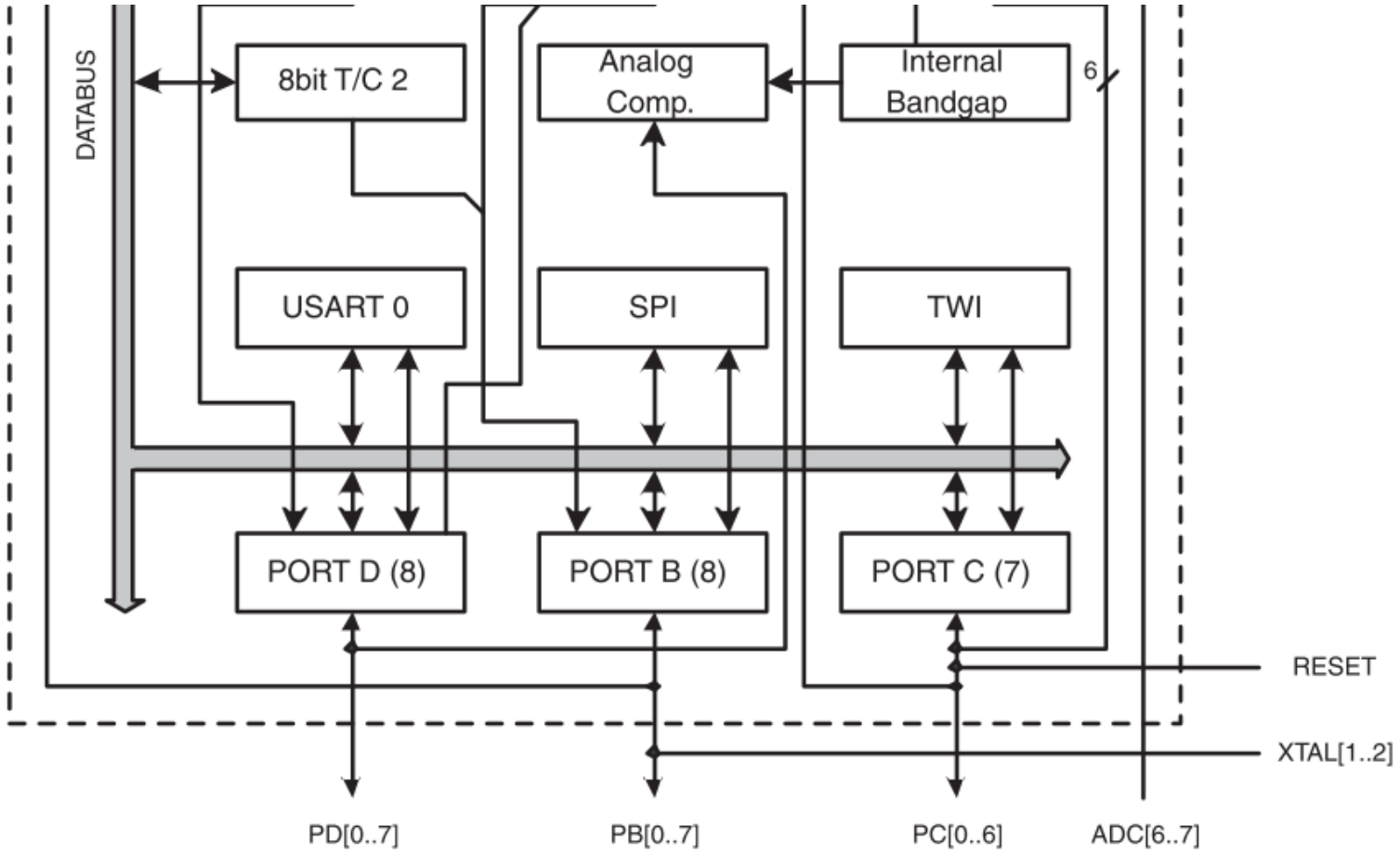
ARDUINO.CC

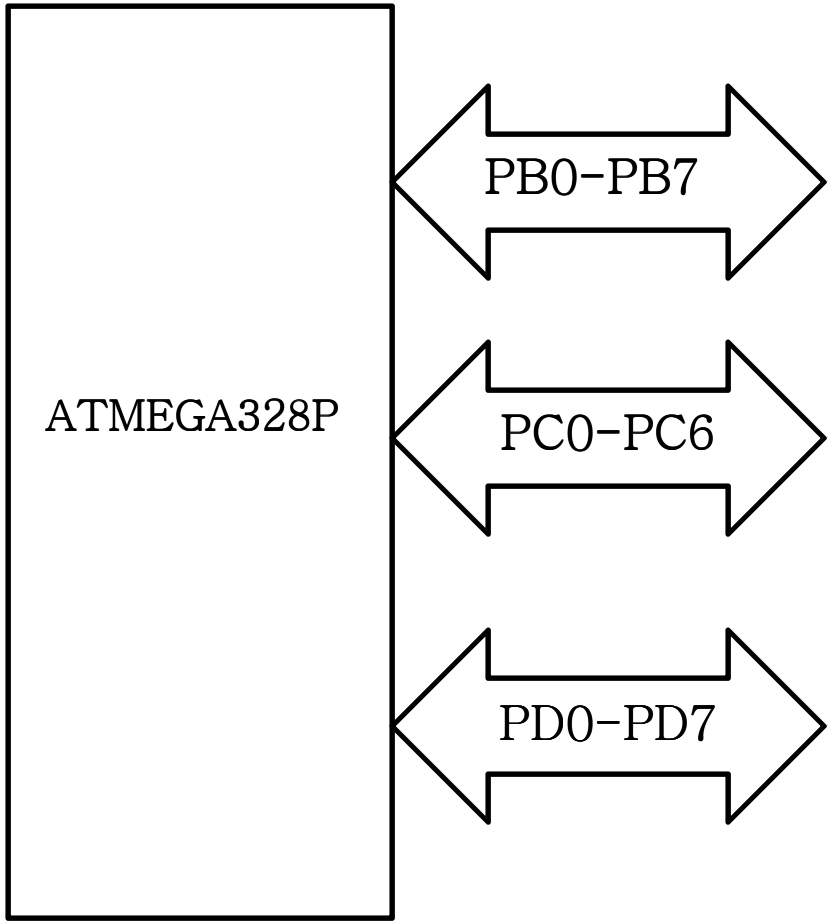
ATMEGA328 – PINAGEM



ATMEGA328 – PINAGEM

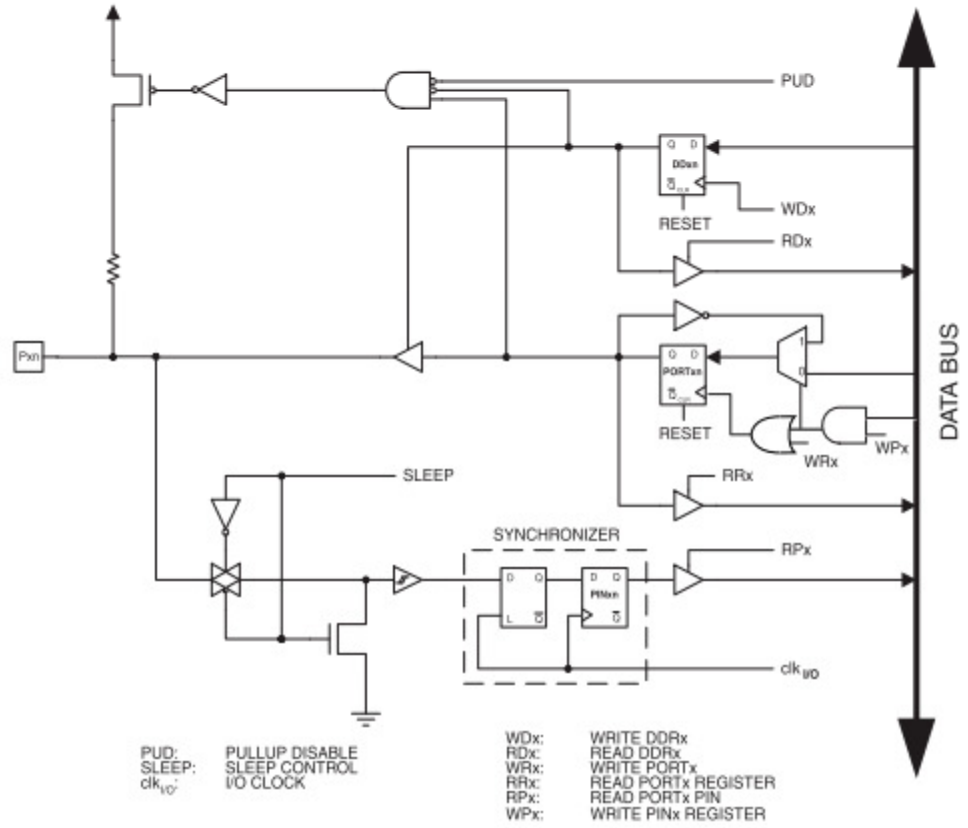


ATMEGA328 – PINAGEM



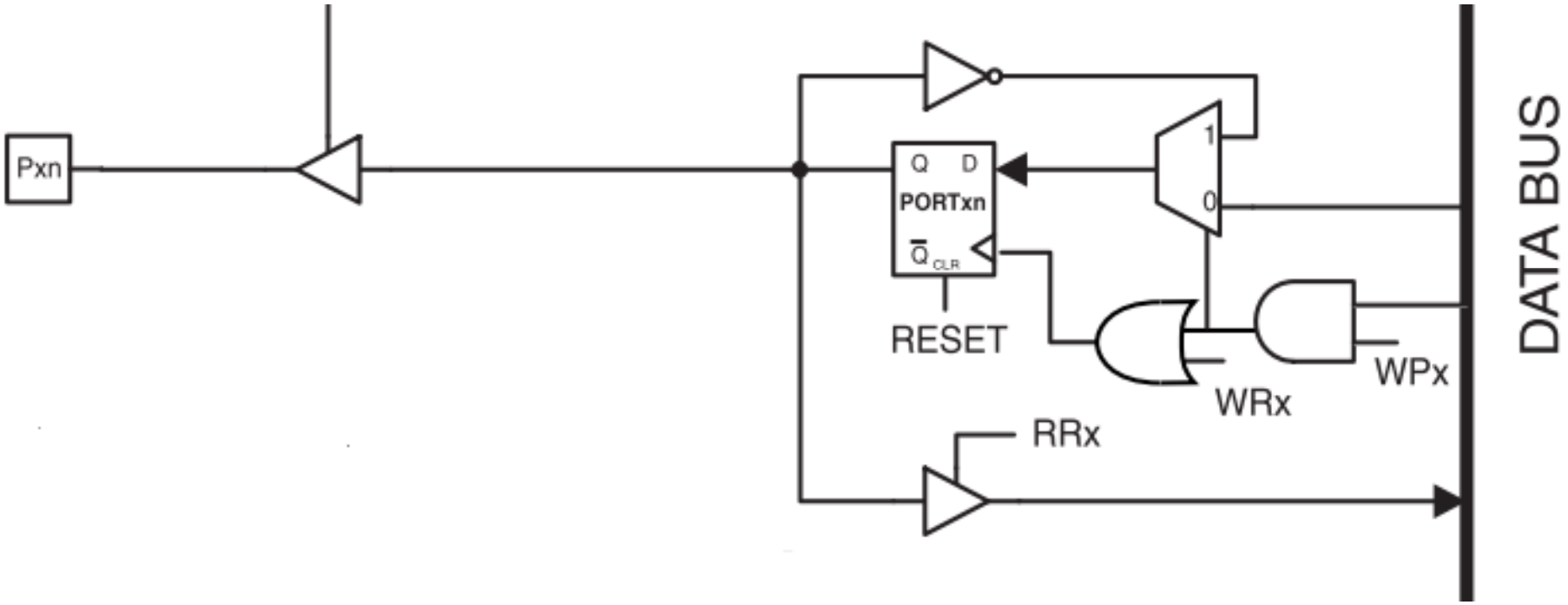
ATMEGA328 – I/O DIGITAL

Figure 14-2. General Digital I/O[1]

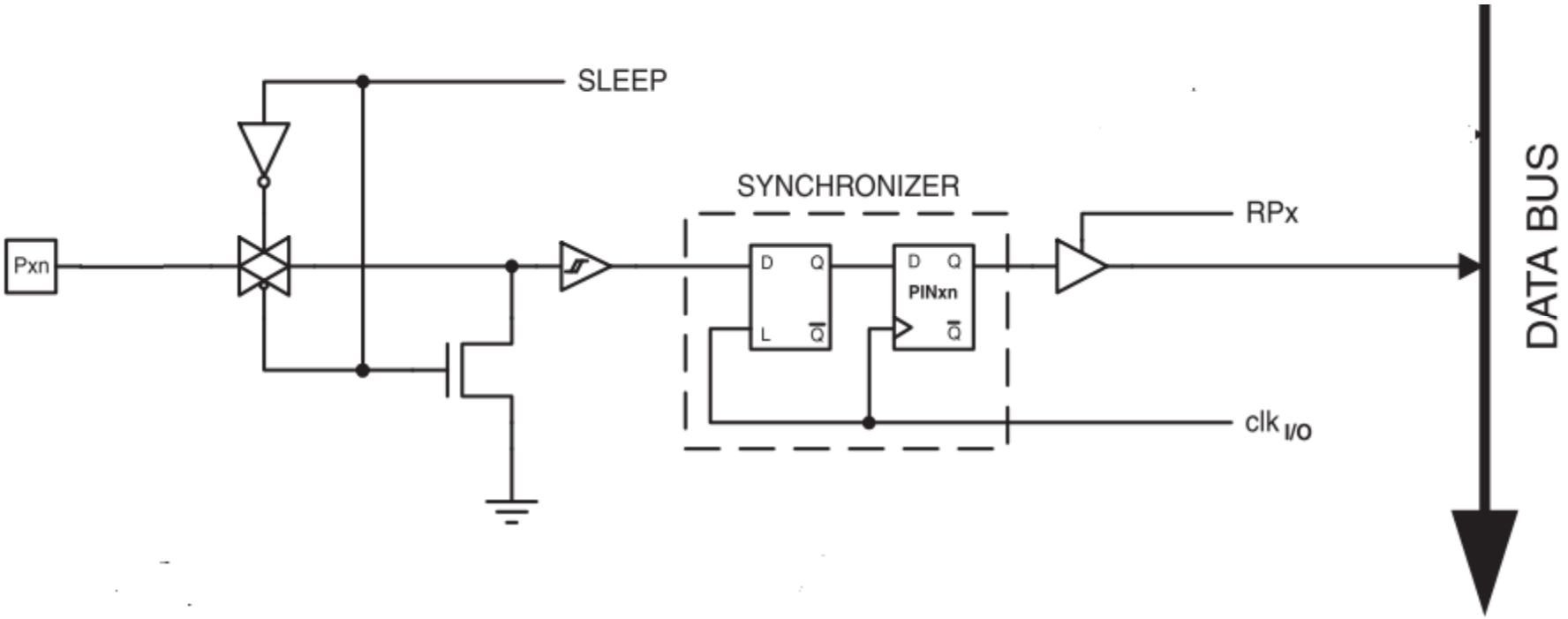


Note: 1. WRx, WPx, WDx, RRx, RPx, and RDx are common to all pins within the same port. $clk_{I/O}$, SLEEP, and PUD are common to all ports.

ATMEGA328 – I/O DIGITAL



ATMEGA328 – I/O DIGITAL



ATMEGA328 – I/O DIGITAL

Figure 14-3. Synchronization when Reading an Externally Applied Pin value