EE5320 Analog IC Design

Fully Differential Op-Amp Design

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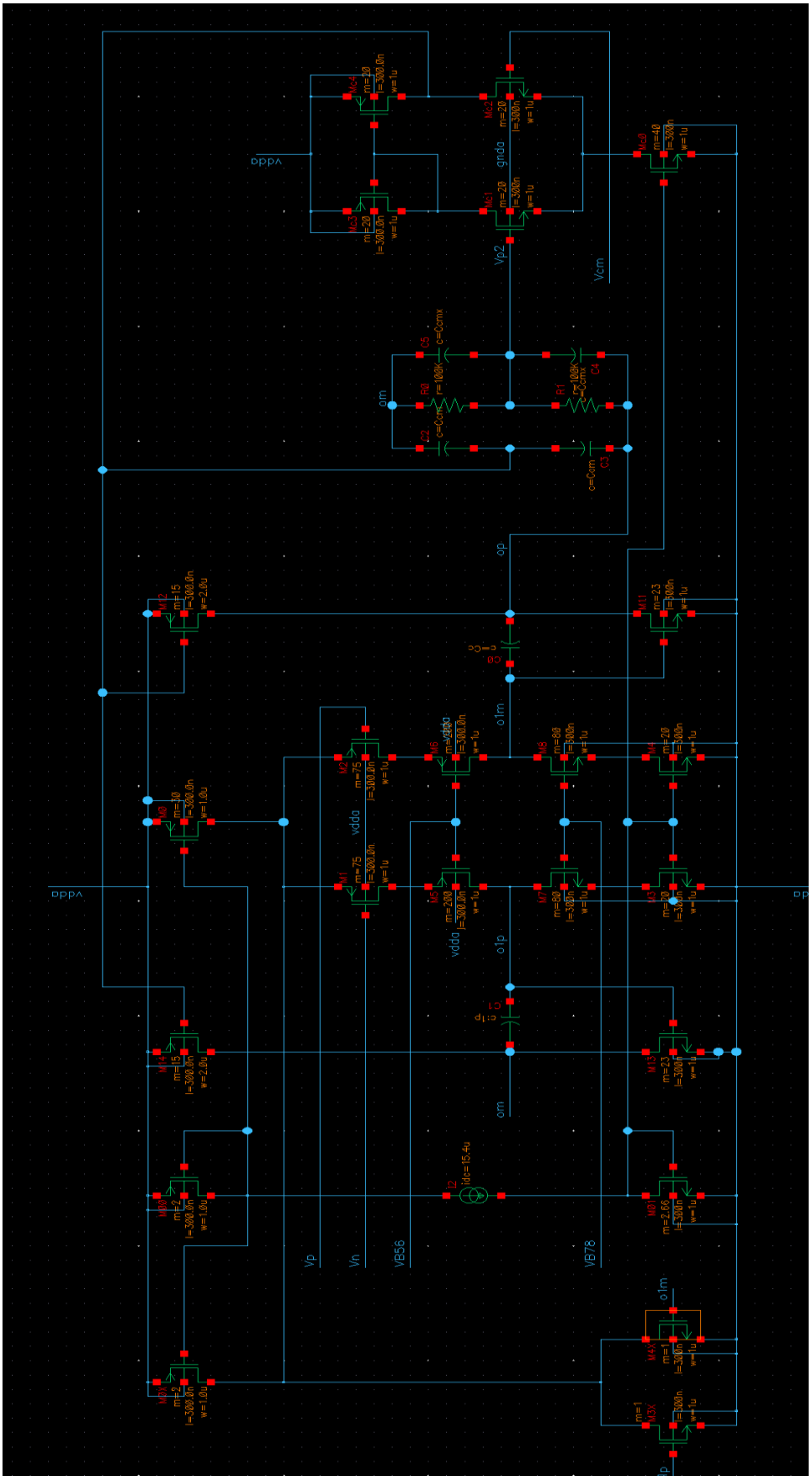
OpAmp Schematic:



Test Bench:

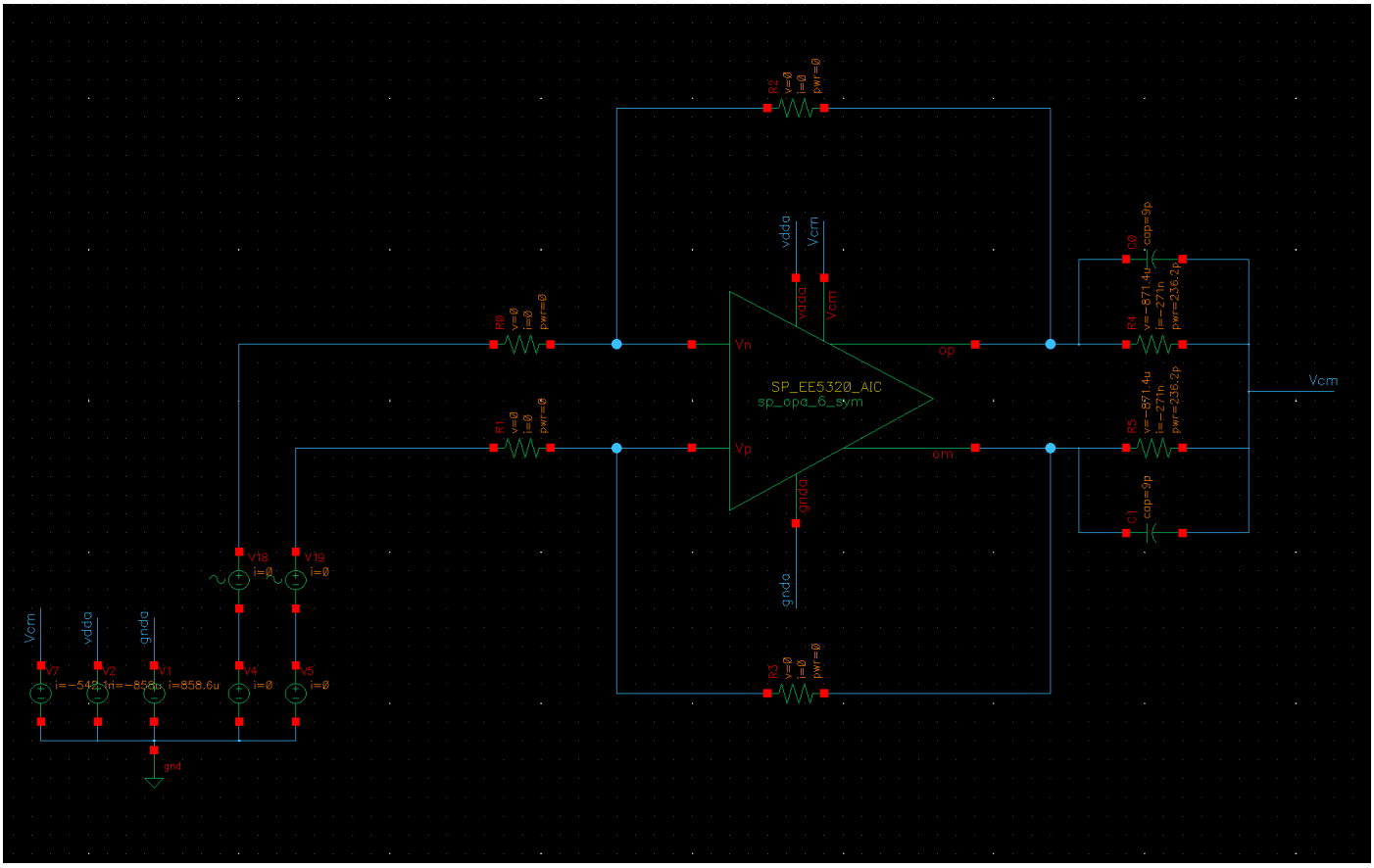
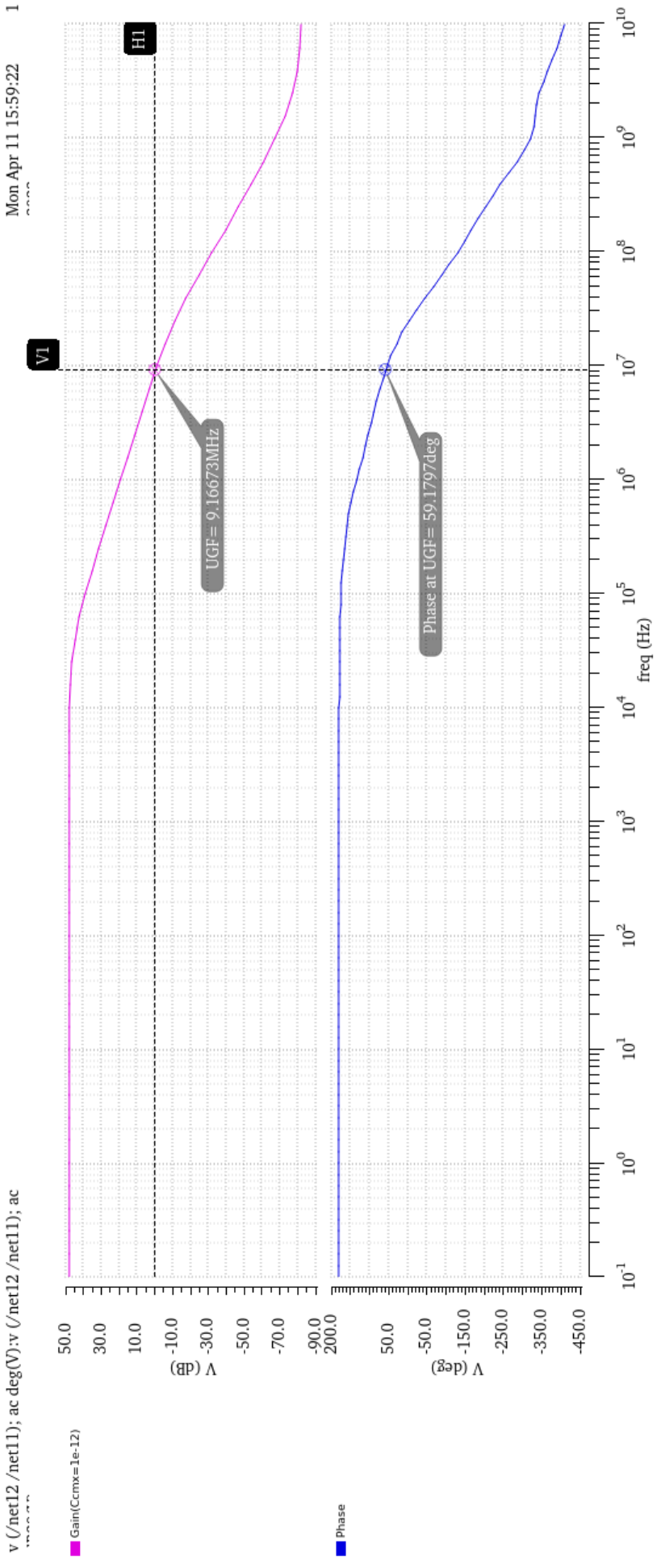


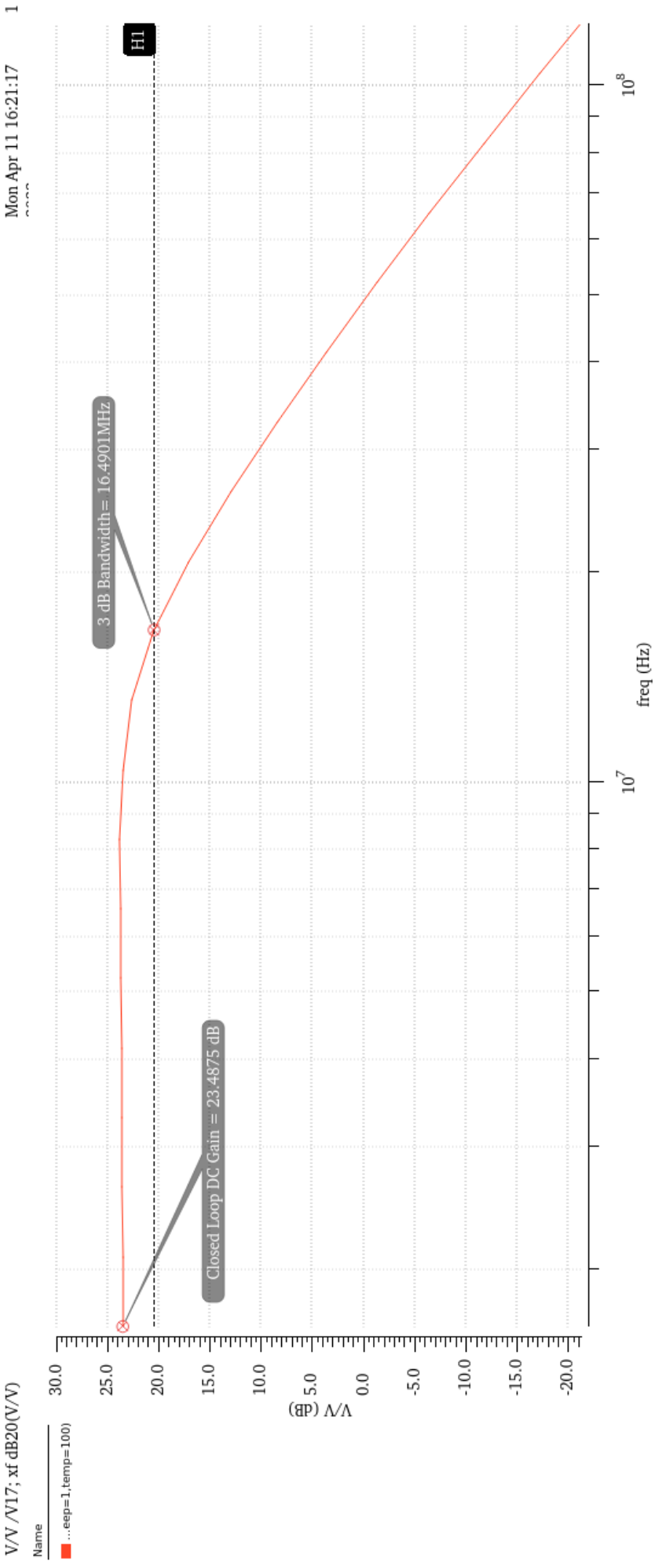
Table 1: Specifications	
Closed loop dc gain	15
Closed loop bandwidth	11 MHz
Load capacitor CL	9 pF
Load resistor RL	3.215 $K\Omega$
Input resistance Ri	19 $K\Omega$
Rf	285 $K\Omega$
Gm1	1.1058 mS
Gm2	2.527 mS
Cc	1 pF
Ccm	4 pF
Ccmx	4 pF

Plots:

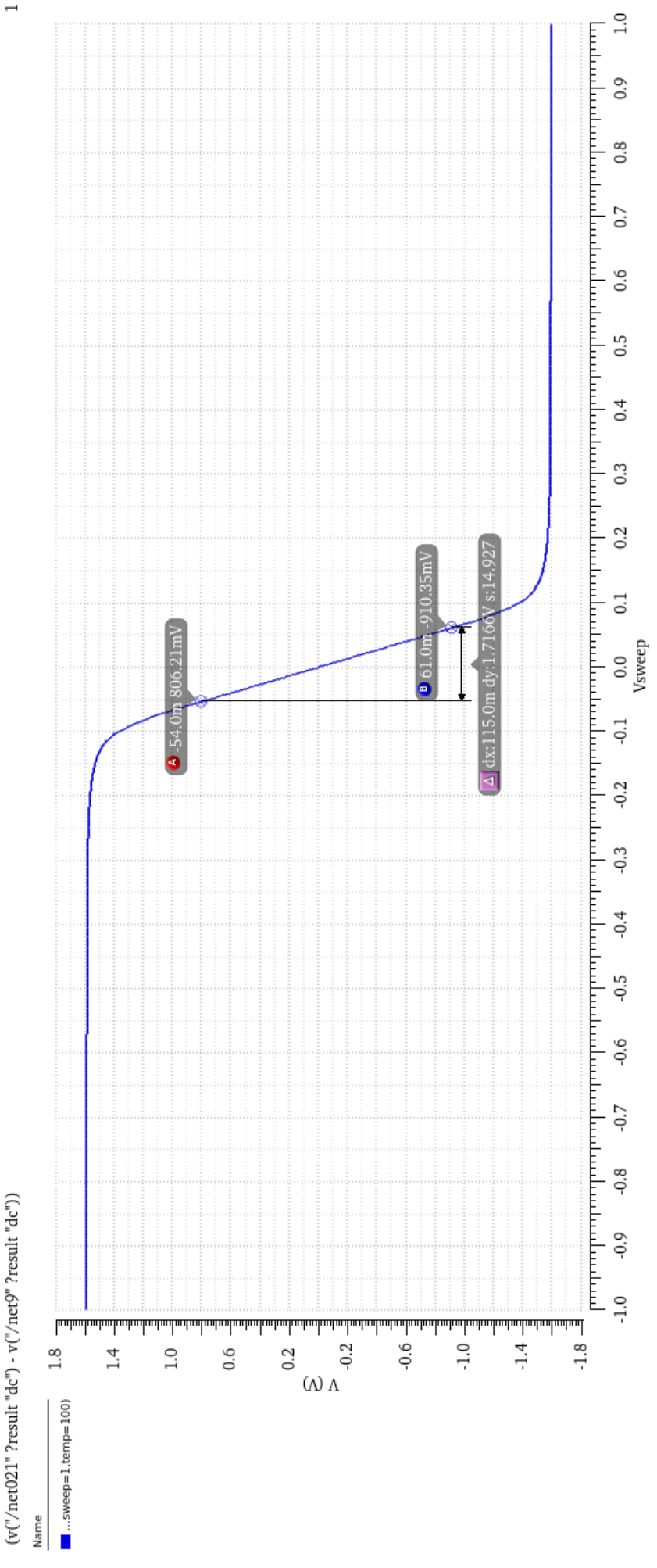
1. Loop Gain:



2. Closed Loop Transfer Function:

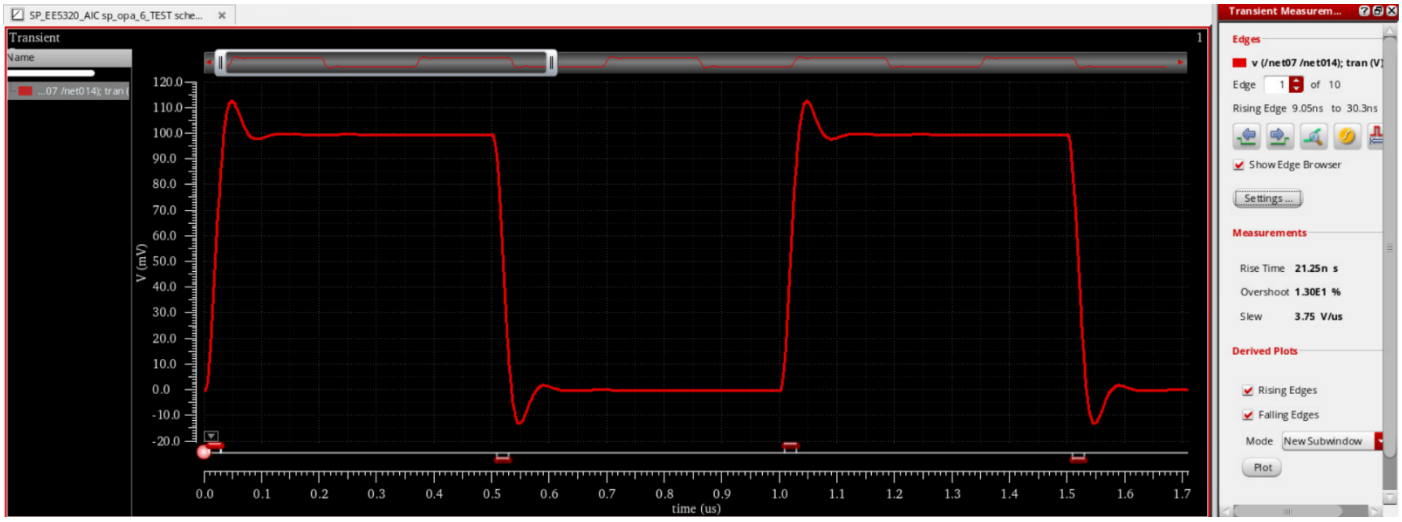


3. *DC V_o vs V_i Transfer Curve*:

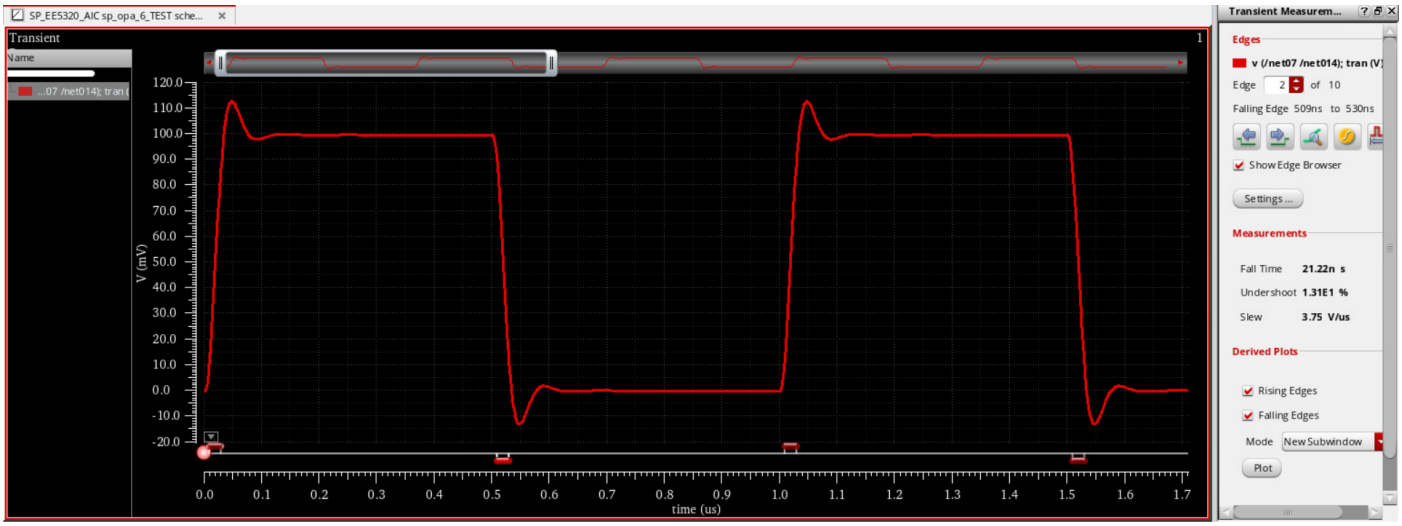


4. Small Signal Step Response:

Rise Time = 21.25 nS

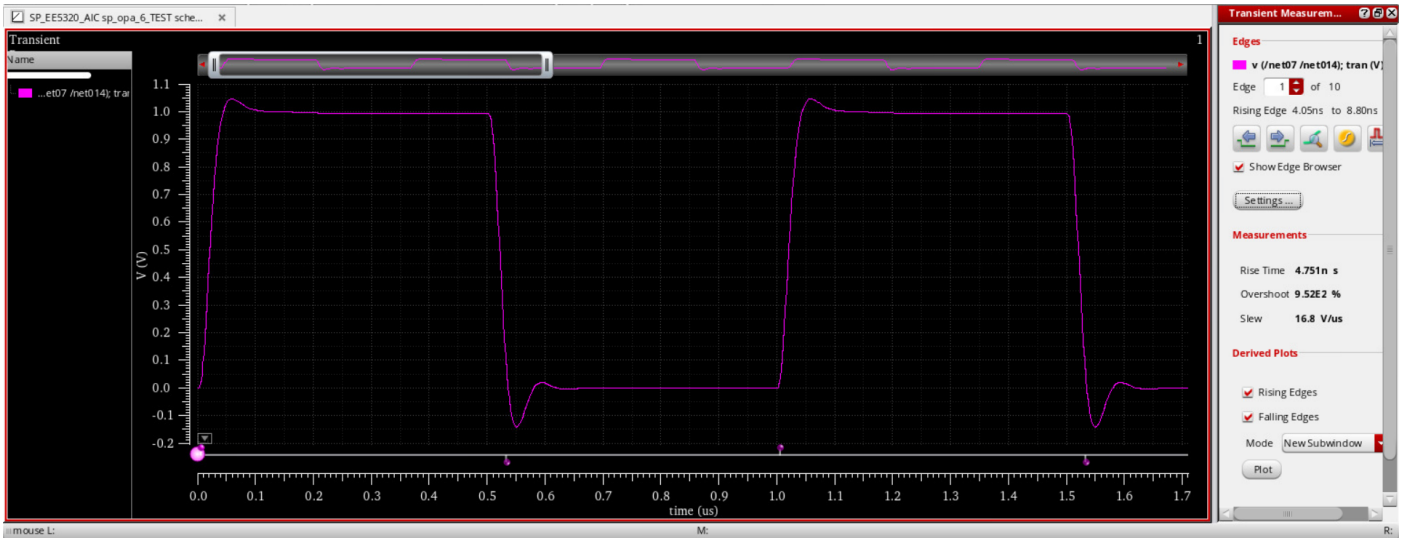


Fall Time = 21.22 ns

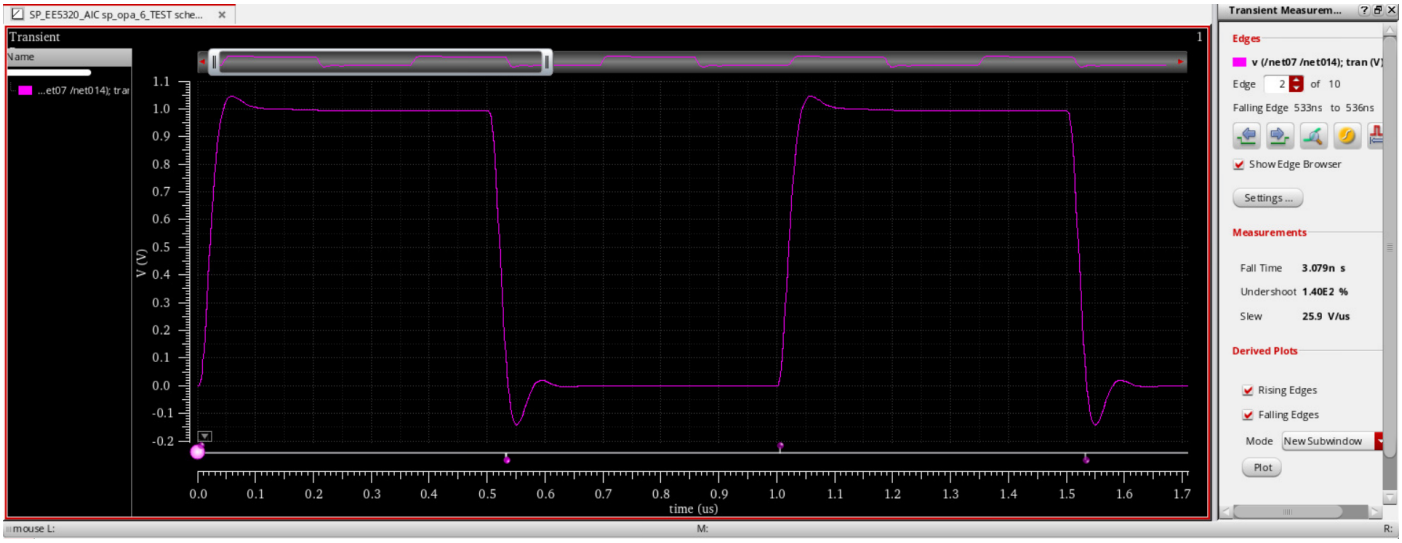


5. Large Signal Step Response:

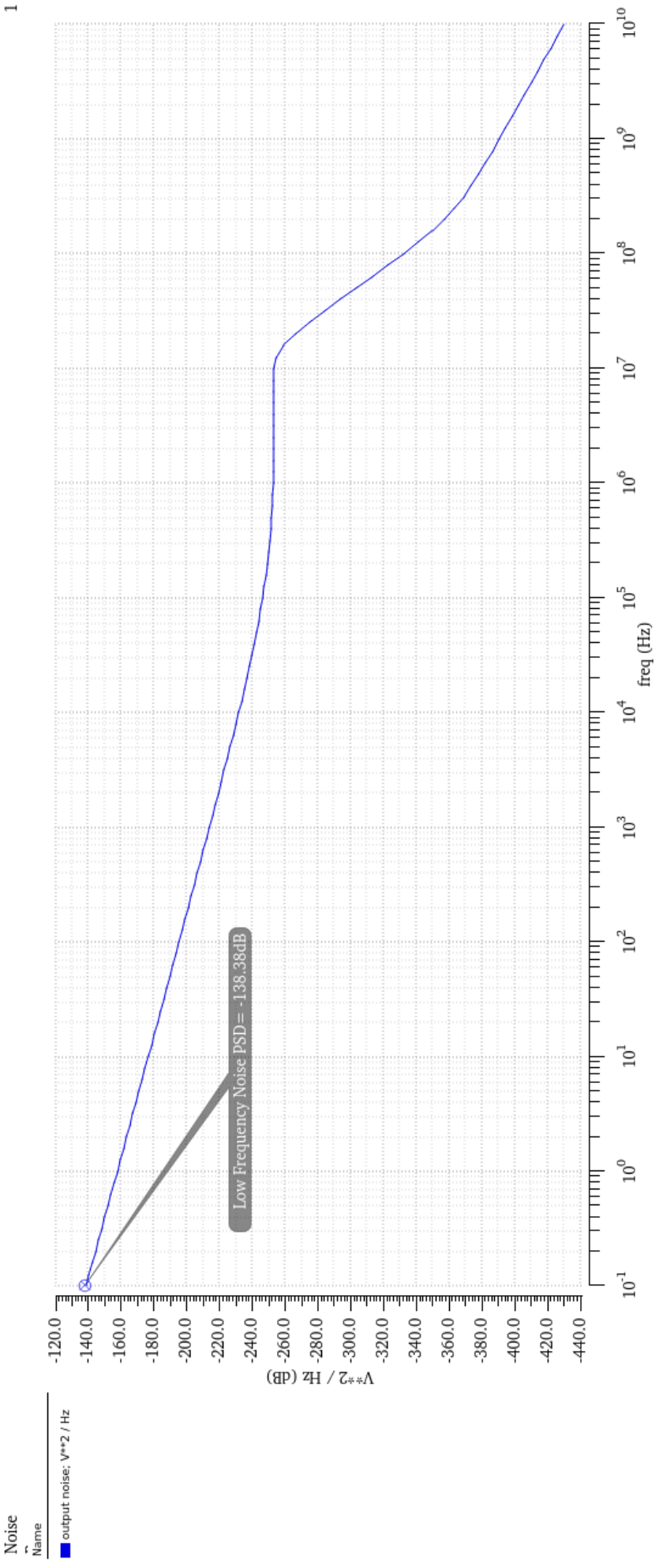
Rise Time = 4.751 ns



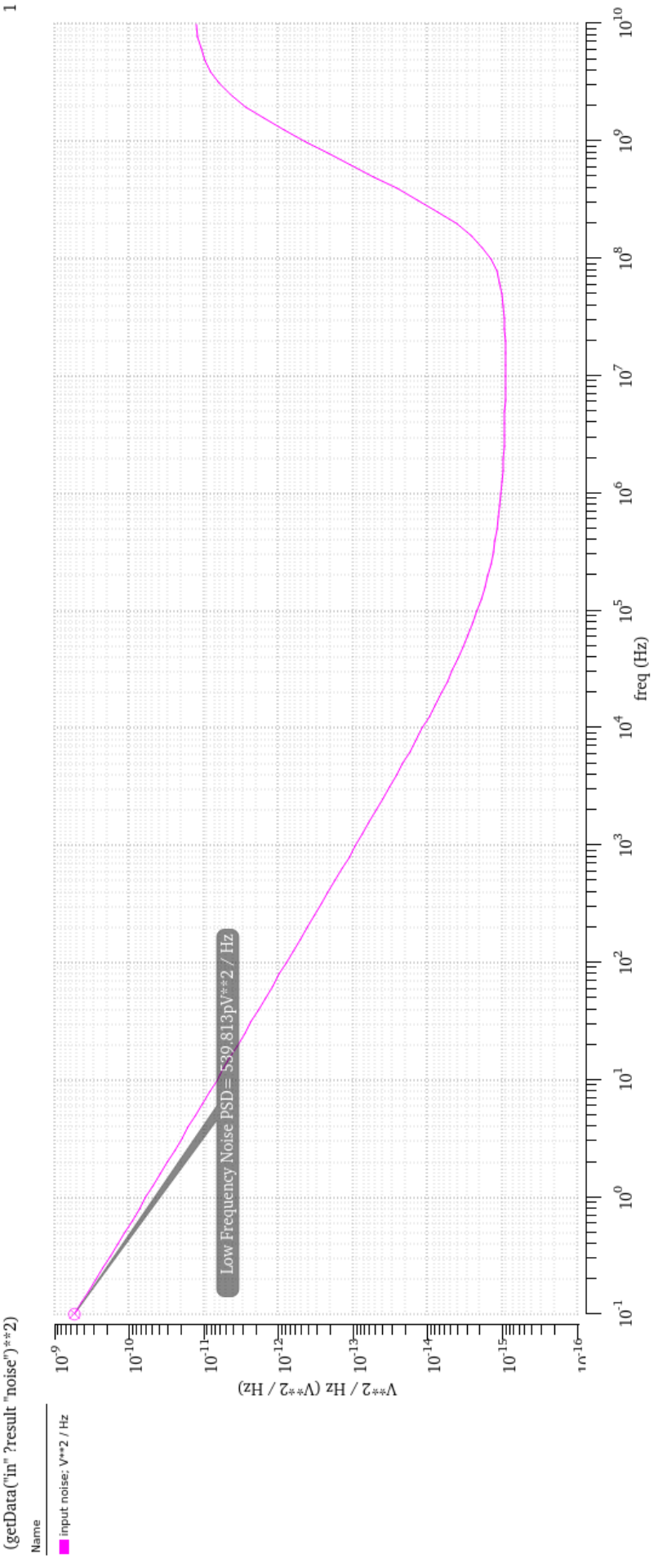
Fall Time = 3.079 ns



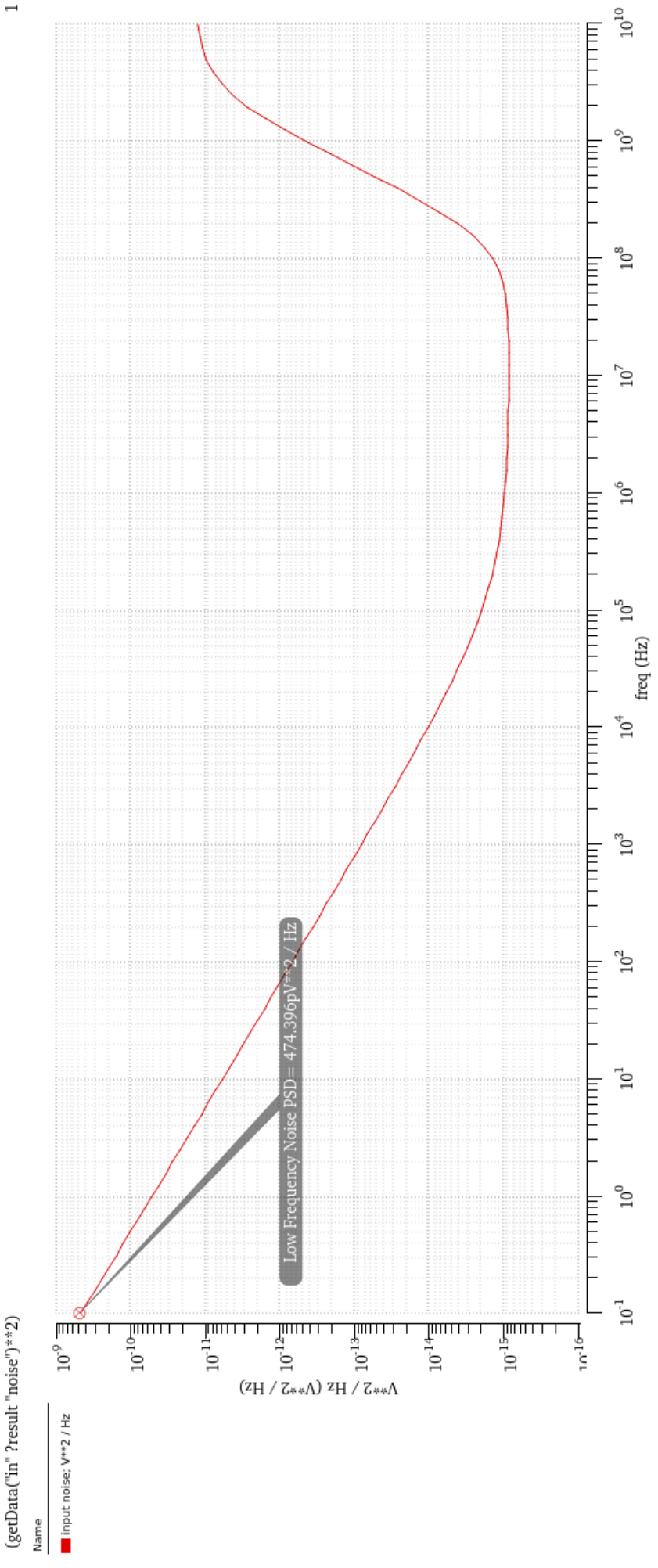
6. Output noise PSD:



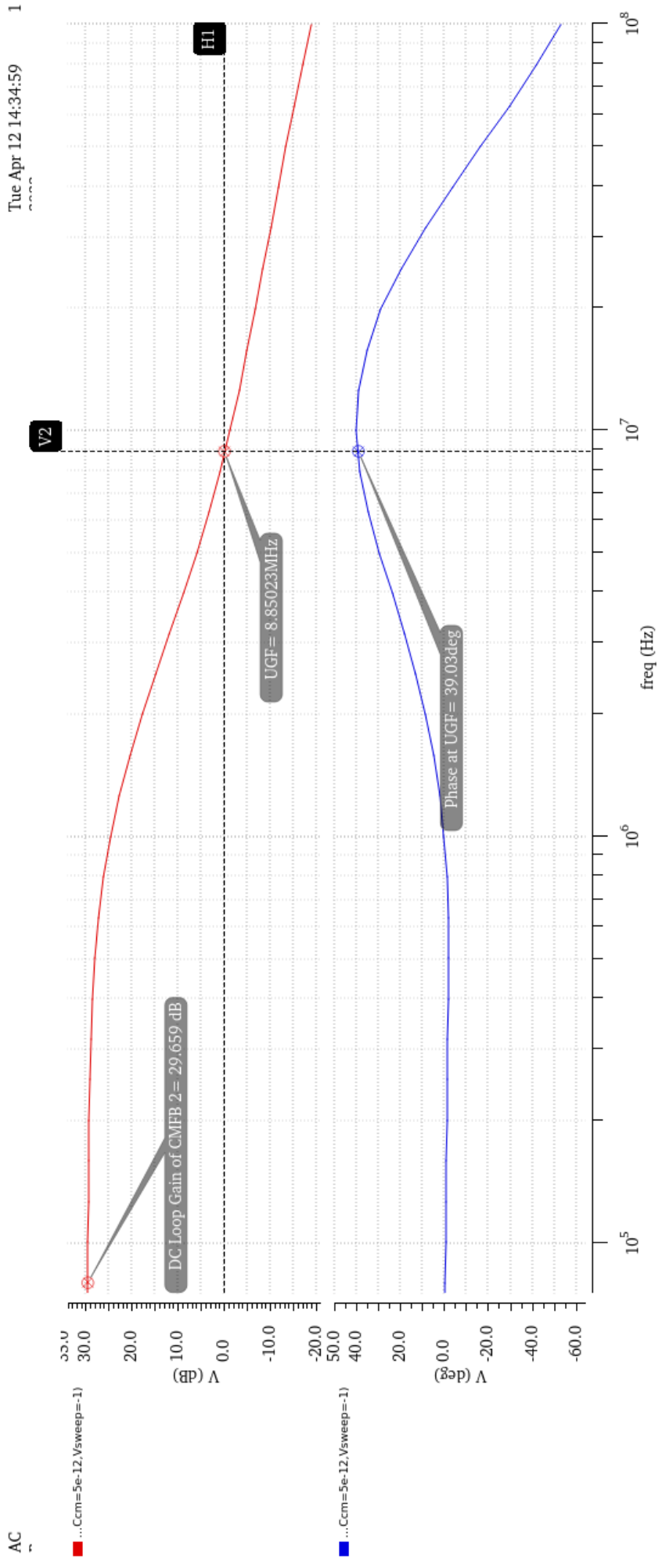
7. Input Referred noise PSD:



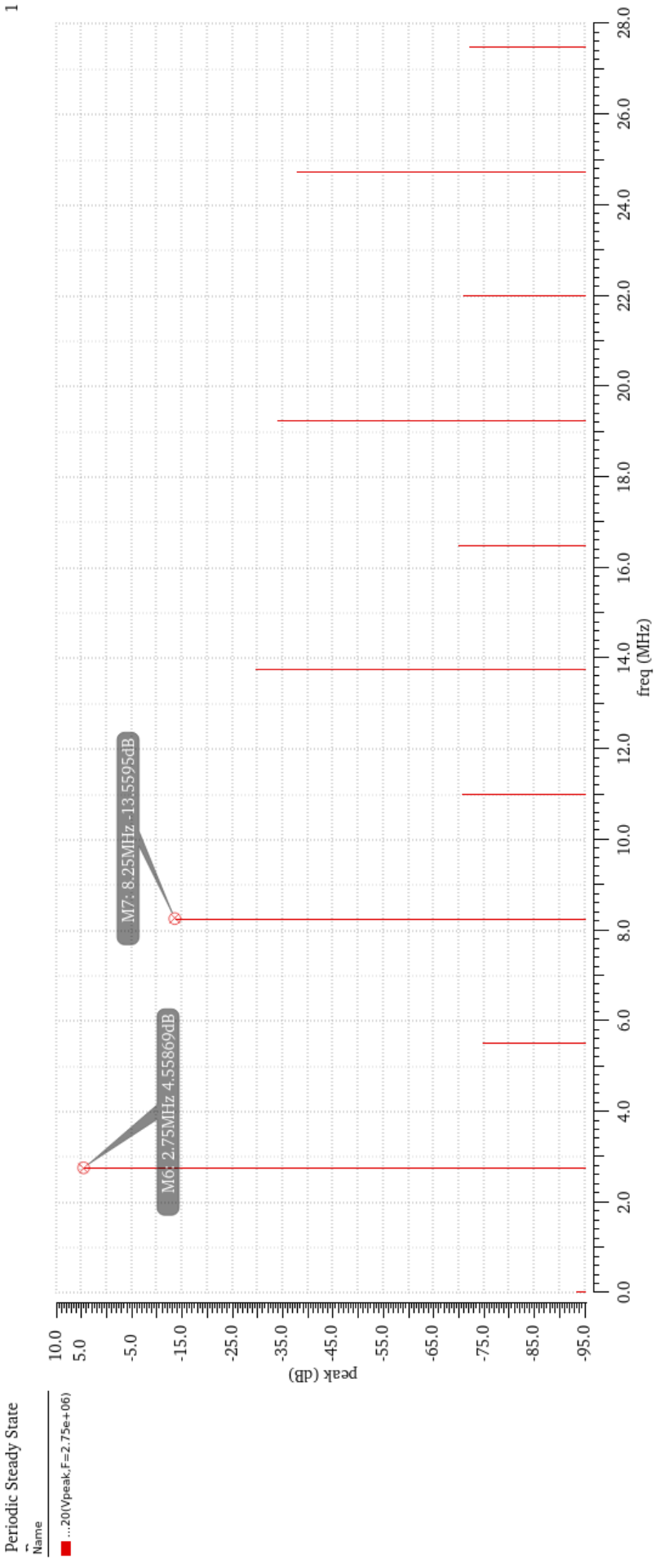
8. Input Referred Noise PSD of OpAmp:



9. CMFB2 Loop gain:



10. HD3:



HD3 = -18.118 dB

Table 2: Transistor sizes and operating points					
Transistor	**nMOS/pMOS**	**W/L**	**Bias current**	**gm**	**gds**
M00	pMOS	2u/0.3u	15.4uA	96.19 uS	21.29 uS
M0	pMOS	30u/0.3u	204.6uA	1.211 mS	164.5 uS
M01	nMOS	3u/0.3u	15.4uA	203.2 uS	3.311 uS
M1,2	pMOS	75u/0.3u	99.28uA	1.265 mS	73.79 uS
M3,4	nMOS	20u/0.3u	99.28uA	1.292 mS	99.88 uS
M5,6	pMOS	200u/0.3u	99.28uA	1.796 mS	17.5 us
M7,8	nMOS	80u/0.3u	99.28uA	1.796 mS	30.52 uS
M11	nMOS	23u/0.3u	206.5uA	2.36 mS	32.8 us
M12	pMOS	30u/0.3u	206.8uA	1.39 mS	2129 uS
M0x	pMOS	2u/0.3u	13.64uA	80.74 uS	10.97 uS
M3x,M4x	nMOS	1u/0.3u	9.874uA	109.1 uS	1.33 uS
Mc0	nMOS	40u/0.3u	211.1uA	2.797 mS	96.889 uS
Mc1,c2	nMOS	20u/0.3u	105.3 uA	1.46 mS	20.02 uS
Mc3,c4	pMOS	20u/0.3u	105.3 uA	813.1 uS	14.36 uS

Table 3: Simulation results	
Supply voltage	1.8 V
Power consumption	1.358 mW
Closed loop dc gain	14.94
Closed loop 3dB frequency	16.49 MHz
Opamp dc gain	72.2 dB
DC loop gain	48.05 dB
Unity loop gain frequency	9.166 MHz
Phase margin	59.1797 deg
Positive slew rate	28.6 V/us
Negative slew rate	29.04 V/us
Low frequency input noise PSD	-185.355 dBc/Hz
CMFB2 DC loop gain	29.66 dB
CMFB2 Unity loop gain frequency	8.85023 MHz
CMFB2 phase margin	39.03 deg
HD3	-18.118 dB
Percentage noise contributions from:	
Ri	0.82%
Rf	0.03%
RL	0%
M1,2	3.29%
M3,4	95.9%
M5,6,7,8	0.08%
M11,12	0%
M0,M00	0%