

PROJECT GROUP - 37

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Problem Statement

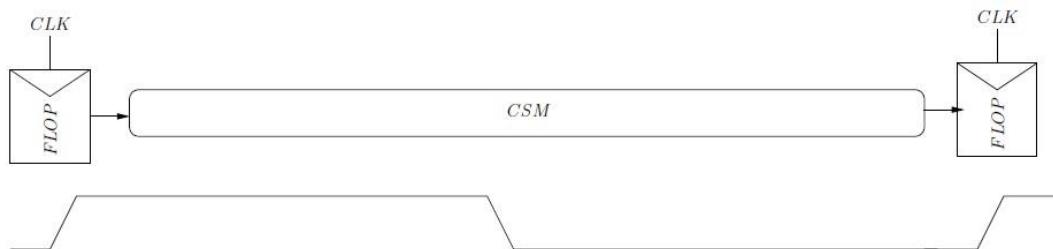
Design a signed 8-bit carry save multiplier with a single stage pipeline. The idea is to show that the frequency of operation can be doubled and data can be fed to the multiplier at twice the rate through pipelining. This would require the following components

- NAND2/ AND2 gate
- Full adder
- Carry out generation circuit
- Sum generation circuit
- Flip flop for pipelining

You have built your library with the above components and submitted each one as an assignment. Now you need to put them together and make the top-level circuit.

Points to be noted- ***We have used Inverting SUM, NAND2 and AND2 gates for schematic.**

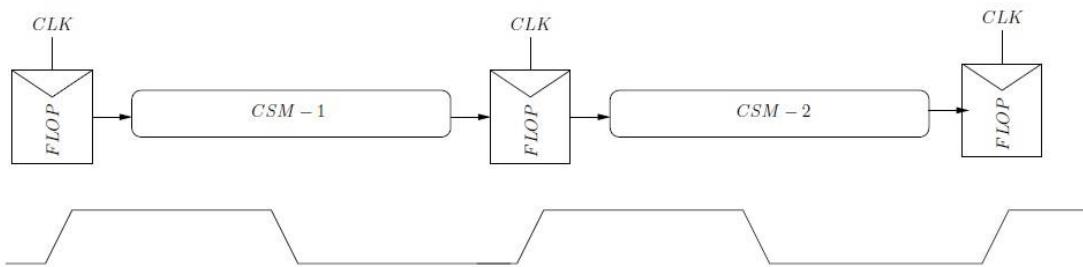
- For **Signed** Carry save multiplier **without** Pipeline circuit as shown below-



Here, Total delay of CSM is sum of Inherent CSM delay and 2 times CLK-Q delay. To work CSM without pipeline normally

$$\text{Max. clock frequency} = \frac{1}{\text{critical path Delay of } CSM + 2 \times \text{CLK-Q Delay}}$$

- For **Signed** Carry save multiplier **with** Pipeline circuit as shown below-

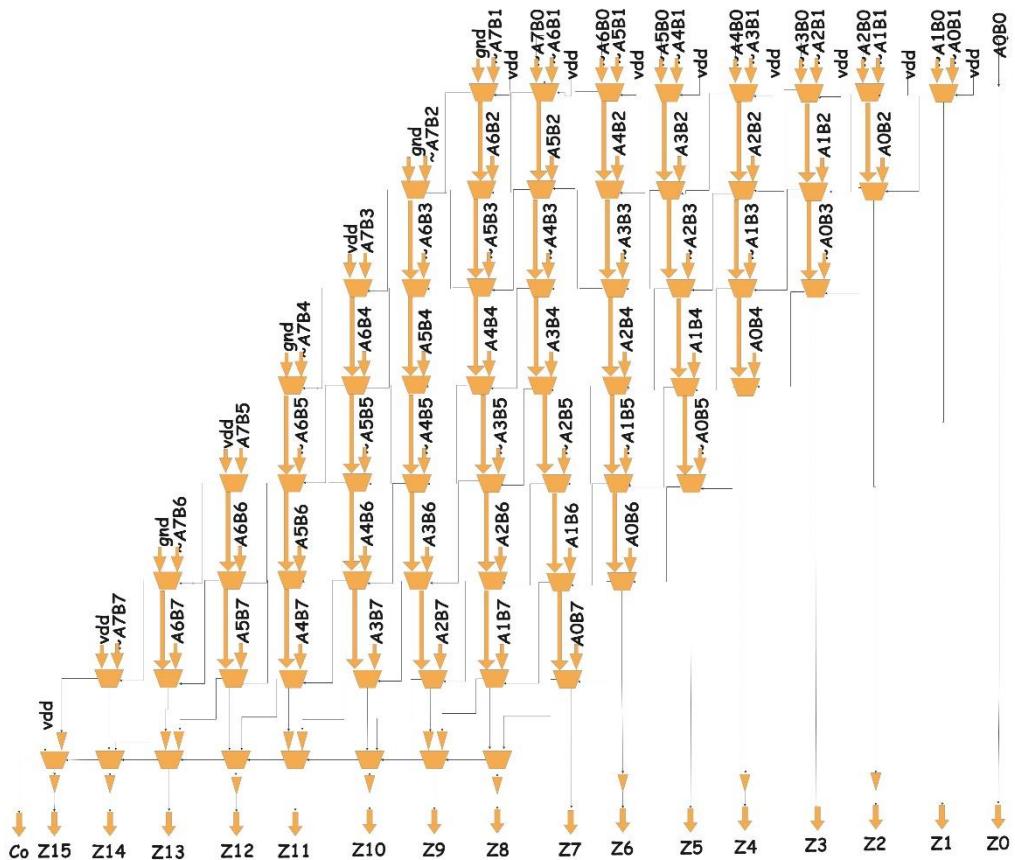


Here, Total delay of CSM is sum of Inherent CSM delay and 3 times CLK-Q delay. To work CSM with pipeline normally

Maximum clock frequency =

$$\frac{1}{(\text{Critical path Delay of } \max(CSM1, CSM2) + 2 \times \text{CLK-Q Delay})}$$

➤ BLOCK DIAGRAM of Signed CSM-

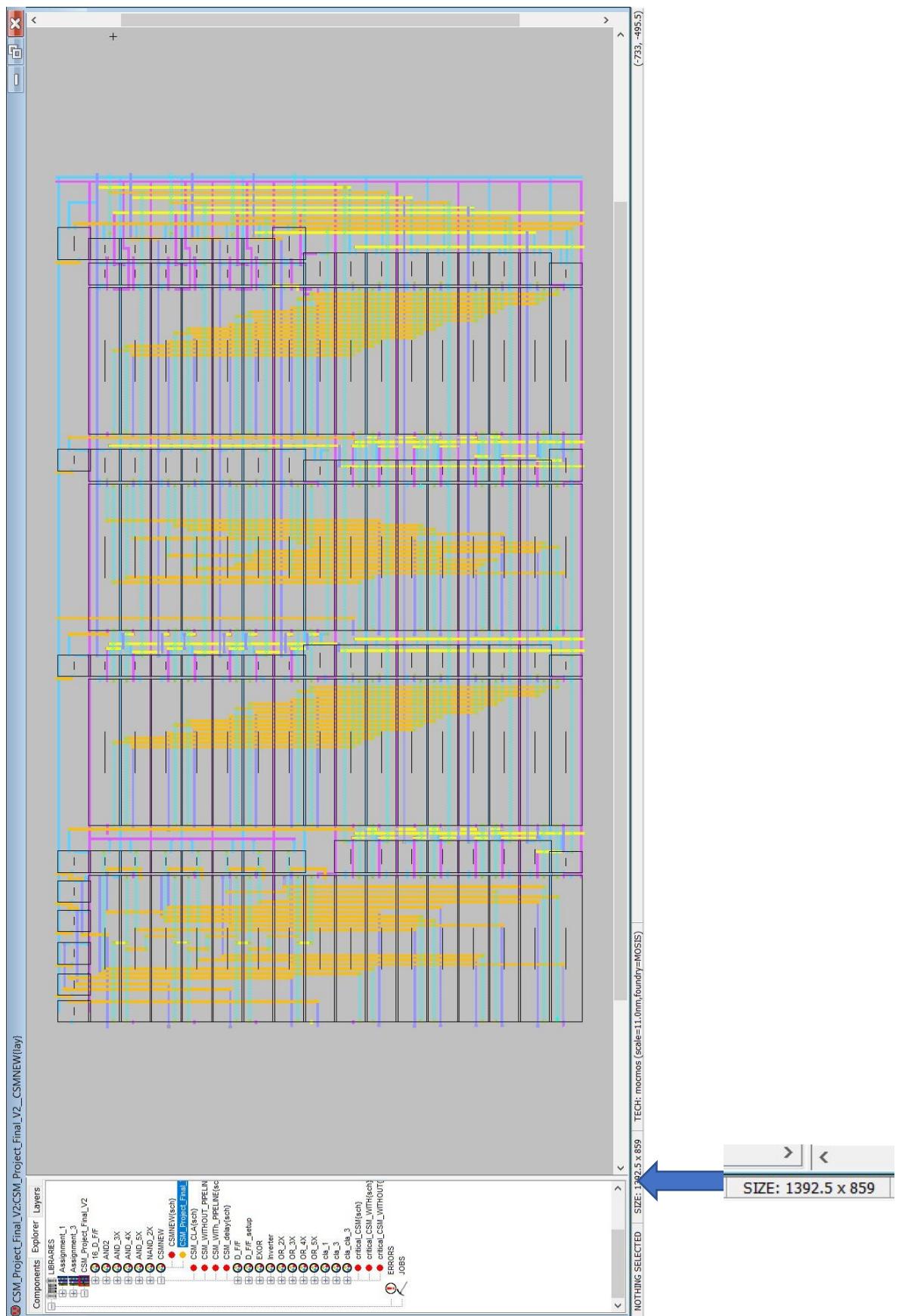


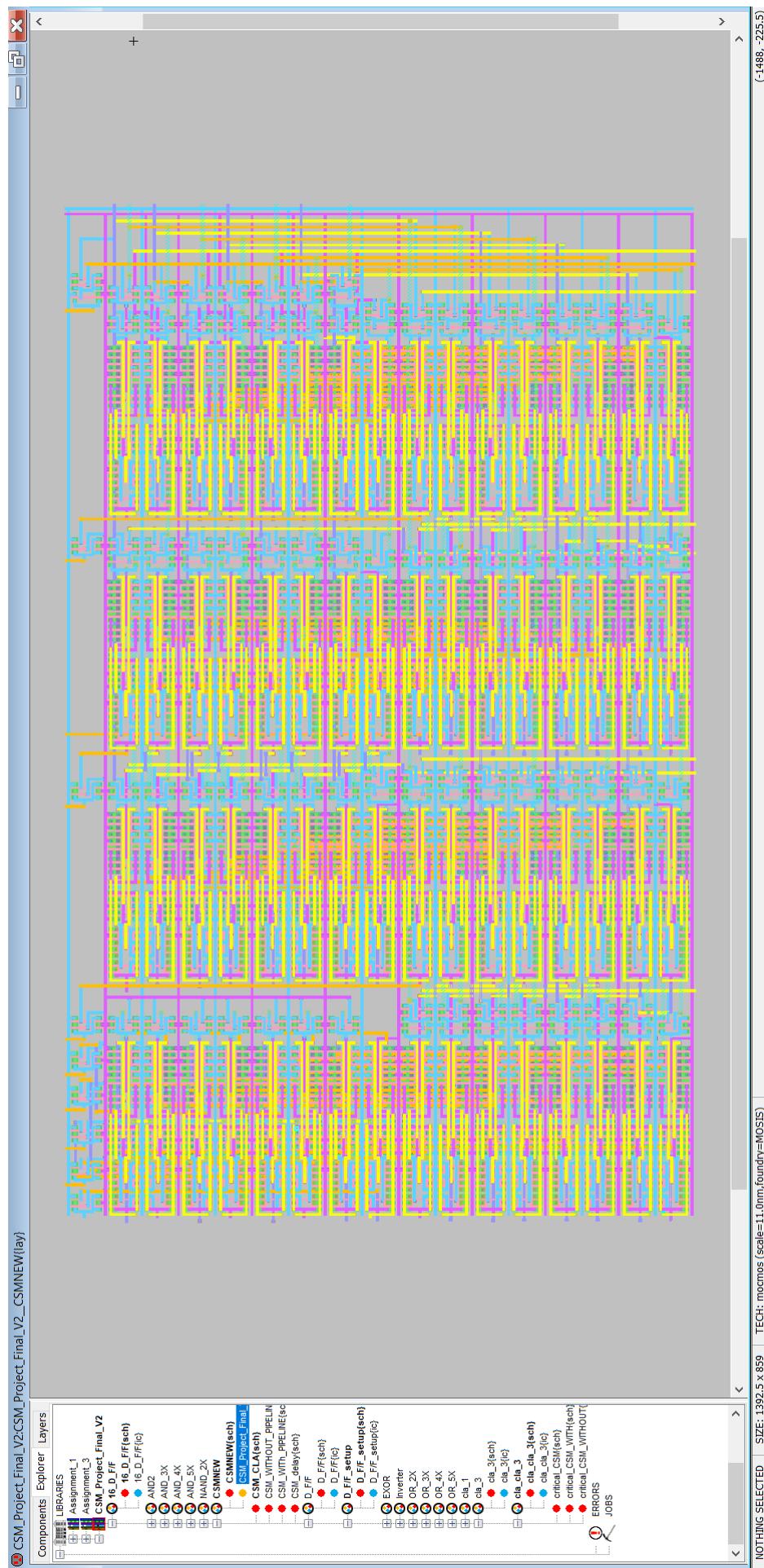
INVERTING SUM

Inverter

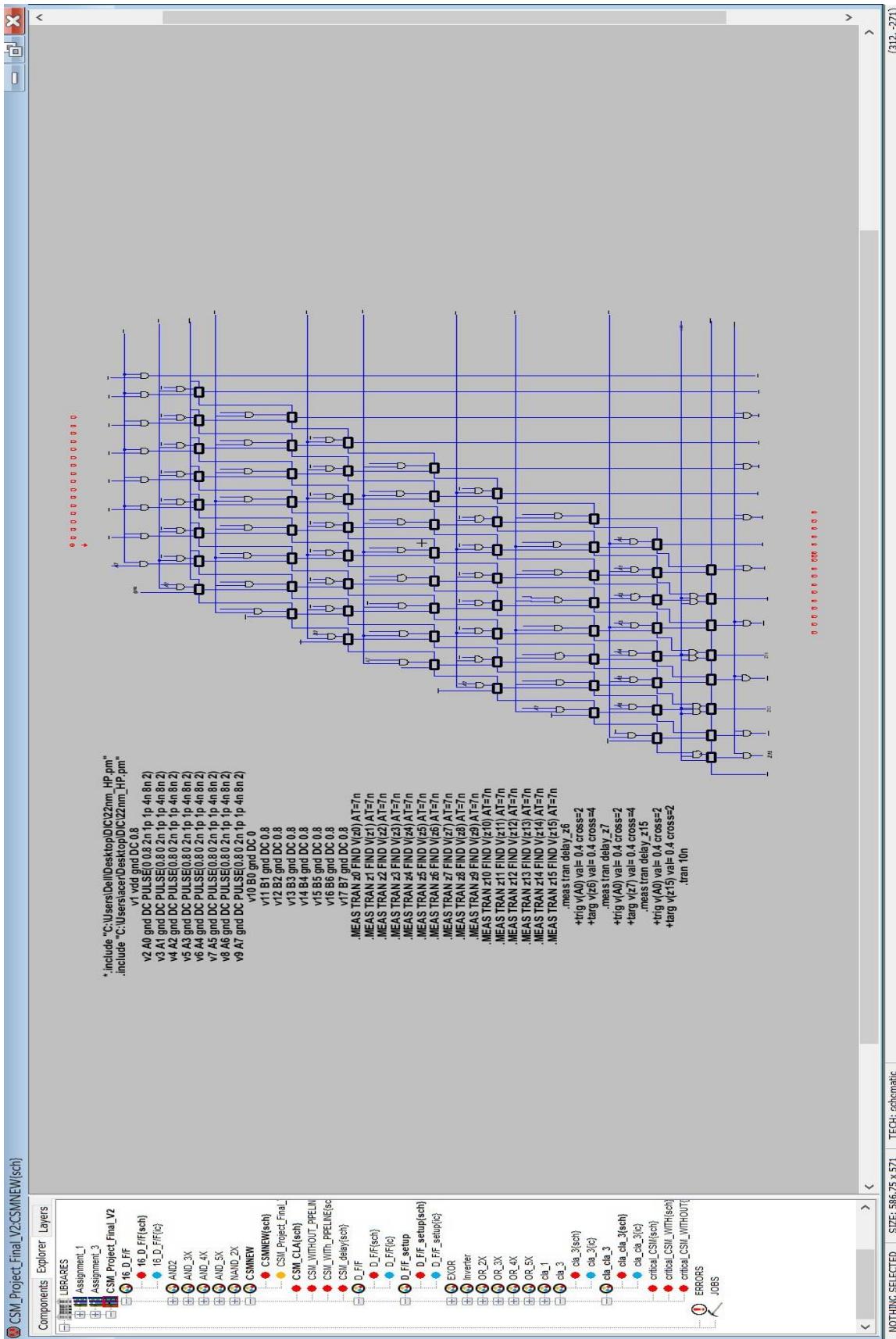
\sim = Inverting

➤ **Area of Signed CSM layout- (Area-: 1392.5*859)**





➤ Schematic of Signed CSM



➤ **DRS & LVS CLEAN:-**

```

Electric Messages
Found 226 networks
0 errors and 0 warnings found (took 0.052 secs)
=====
Hierarchical NCC every cell in the design: cell 'CSMNEW{sch}' cell 'CSM_Project_Final_V2__CSMNEW{lay}'
Comparing: Assignment_1:AND_1X_SP{sch} with: Assignment_1:Assignment_1__AND_1X_SP{lay}
    exports match, topologies match, sizes not checked in 0.002 seconds.
Comparing: Assignment_3:FA{sch} with: Assignment_3:Assignment_3__FA{lay}
    exports match, topologies match, sizes not checked in 0.003 seconds.
Comparing: Assignment_1:NAND_1X_SP{sch} with: Assignment_1:Assignment_1__NAND_1X_SP{lay}
    exports match, topologies match, sizes not checked in 0.001 seconds.
Comparing: CSM_Project_Final_V2:CSMNEW{sch} with: CSM_Project_Final_V2:CSM_Project_Final_V2__CSMNEW{lay}
    exports match, topologies match, sizes not checked in 0.024 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.037 seconds.
  
```

➤ **Functionality check:-**

❖ **Input -**

Case 1- A= 5, B =-5

A=	0	0	0	0	0	1	0	1
----	---	---	---	---	---	---	---	---

B=	1	1	1	1	1	1	0	1	1
----	---	---	---	---	---	---	---	---	---

Case 2- A= -2, B = -2

A=	1	1	1	1	1	1	1	1	0
----	---	---	---	---	---	---	---	---	---

B=	1	1	1	1	1	1	1	1	0
----	---	---	---	---	---	---	---	---	---

❖ **Output -**

Case 1 - Z = -25

Co	Z15	Z14	Z13	Z12	Z11	Z10	Z9	Z8	Z7	Z6	Z5	Z4	Z3	Z2	Z1	Z0
0	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1

Case 2 - Z = 4

Co	Z15	Z14	Z13	Z12	Z11	Z10	Z9	Z8	Z7	Z6	Z5	Z4	Z3	Z2	Z1	Z0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

❖ Recorded output using LTSPICE:-

Case 1 –

```

* Spice Code nodes in cell cell 'CSM_Project_Final_V2:CSMNEW{sch}'
*.include "C:\Users\DELL\Desktop\DISC22mm_HP.pm"
*.include "C:\Users\acer\Desktop\DISC22mm_HP.pm"
v1 vdd1 gnd DC 0.8
v2 A0 gnd DC 0.8
v3 A1 gnd DC 0
v4 A2 gnd DC 0.8
v5 A3 gnd DC 0
v6 A4 gnd DC 0
v7 A5 gnd DC 0
v8 A6 gnd DC 0
v9 A7 gnd DC 0
v10 B0 gnd DC 0.8
v11 B1 gnd DC 0.8
v12 B2 gnd DC 0
v13 B3 gnd DC 0.8
v14 B4 gnd DC 0.8
v15 B5 gnd DC 0.8
v16 B6 gnd DC 0.8
v17 B7 gnd DC 0.8
.tran 10n uic
.MEAS TRAN Z0 FIND V(z0) AT=7n
.MEAS TRAN Z1 FIND V(z1) AT=7n
.MEAS TRAN Z2 FIND V(z2) AT=7n
.MEAS TRAN Z3 FIND V(z3) AT=7n
.MEAS TRAN Z4 FIND V(z4) AT=7n
.MEAS TRAN Z5 FIND V(z5) AT=7n
.MEAS TRAN Z6 FIND V(z6) AT=7n
.MEAS TRAN Z7 FIND V(z7) AT=7n
.MEAS TRAN Z8 FIND V(z8) AT=7n
.MEAS TRAN Z9 FIND V(z9) AT=7n
.MEAS TRAN Z10 FIND V(z10) AT=7n
.MEAS TRAN Z11 FIND V(z11) AT=7n
.MEAS TRAN Z12 FIND V(z12) AT=7n
.MEAS TRAN Z13 FIND V(z13) AT=7n
.MEAS TRAN Z14 FIND V(z14) AT=7n
.MEAS TRAN Z15 FIND V(z15) AT=7n
.MEAS TRAN ZCo FIND V(Co) AT=7n
.END

```

SPICE Error Log: C:\Users\acer\Desktop\DISC22mm_HP.pm

Circuit: *** SPICE deck for cell CSMNEW{sch} from library CSM_Project_Final_V2

Per .tran options, skipping operating point for transient analysis.

z0: v(z0)=0.799975 at 7e-009
z1: v(z1)=0.799928 at 7e-009
z2: v(z2)=0.799987 at 7e-009
z3: v(z3)=0.000136488 at 7e-009
z4: v(z4)=0.000102614 at 7e-009
z5: v(z5)=0.799961 at 7e-009
z6: v(z6)=0.799987 at 7e-009
z7: v(z7)=0.799925 at 7e-009
z8: v(z8)=0.799987 at 7e-009
z9: v(z9)=0.799869 at 7e-009
z10: v(z10)=0.799987 at 7e-009
z11: v(z11)=0.799868 at 7e-009
z12: v(z12)=0.799987 at 7e-009
z13: v(z13)=0.799869 at 7e-009
z14: v(z14)=0.799987 at 7e-009
z15: v(z15)=0.799986 at 7e-009
co: v(co)=7.83281e-006 at 7e-009

Date: Fri Dec 10 18:41:42 2021

Case 2 -

* Spice Code nodes in cell cell 'CSM_Project_Final_V2:CSMNEW[sch]'

* .include "C:\Users\Dee\Desktop\DIS\22nm_HP.pm"

.include "C:\Users\acer\Desktop\DIS\22nm_HP.pm"

```

v1 vdd gnd DC 0.8
v2 A0 gnd DC 0
v3 A1 gnd DC 0.8
v4 A2 gnd DC 0.8
v5 A3 gnd DC 0.8
v6 A4 gnd DC 0.8
v7 A5 gnd DC 0.8
v8 A6 gnd DC 0.8
v9 A7 gnd DC 0.8
v10 B0 gnd DC 0
v11 B1 gnd DC 0.8
v12 B2 gnd DC 0.8
v13 B3 gnd DC 0.8
v14 B4 gnd DC 0.8
v15 B5 gnd DC 0.8
v16 B6 gnd DC 0.8
v17 B7 gnd DC 0.8
.tran 10n uic
.MEAS TRAN Z0 FIND V(z0) AT=7n
.MEAS TRAN Z1 FIND V(z1) AT=7n
.MEAS TRAN Z2 FIND V(z2) AT=7n
.MEAS TRAN Z3 FIND V(z3) AT=7n
.MEAS TRAN Z4 FIND V(z4) AT=7n
.MEAS TRAN Z5 FIND V(z5) AT=7n
.MEAS TRAN Z6 FIND V(z6) AT=7n
.MEAS TRAN Z7 FIND V(z7) AT=7n
.MEAS TRAN Z8 FIND V(z8) AT=7n
.MEAS TRAN Z9 FIND V(z9) AT=7n
.MEAS TRAN Z10 FIND V(z10) AT=7n
.MEAS TRAN Z11 FIND V(z11) AT=7n
.MEAS TRAN Z12 FIND V(z12) AT=7n
.MEAS TRAN Z13 FIND V(z13) AT=7n
.MEAS TRAN Z14 FIND V(z14) AT=7n
.MEAS TRAN Z15 FIND V(z15) AT=7n
.MEAS TRAN CO FIND V(co) AT=7n
.END

```

SPICE Error Log: C:\Users\acer\Desktop\DIS\PROJECTSAP\CSMNEW\log

Circuit: *** SPICE deck for cell CSMNEW[sch] from library CSM_Project_Final_V2

Per .tran options, skipping operating point for transient analysis.

```

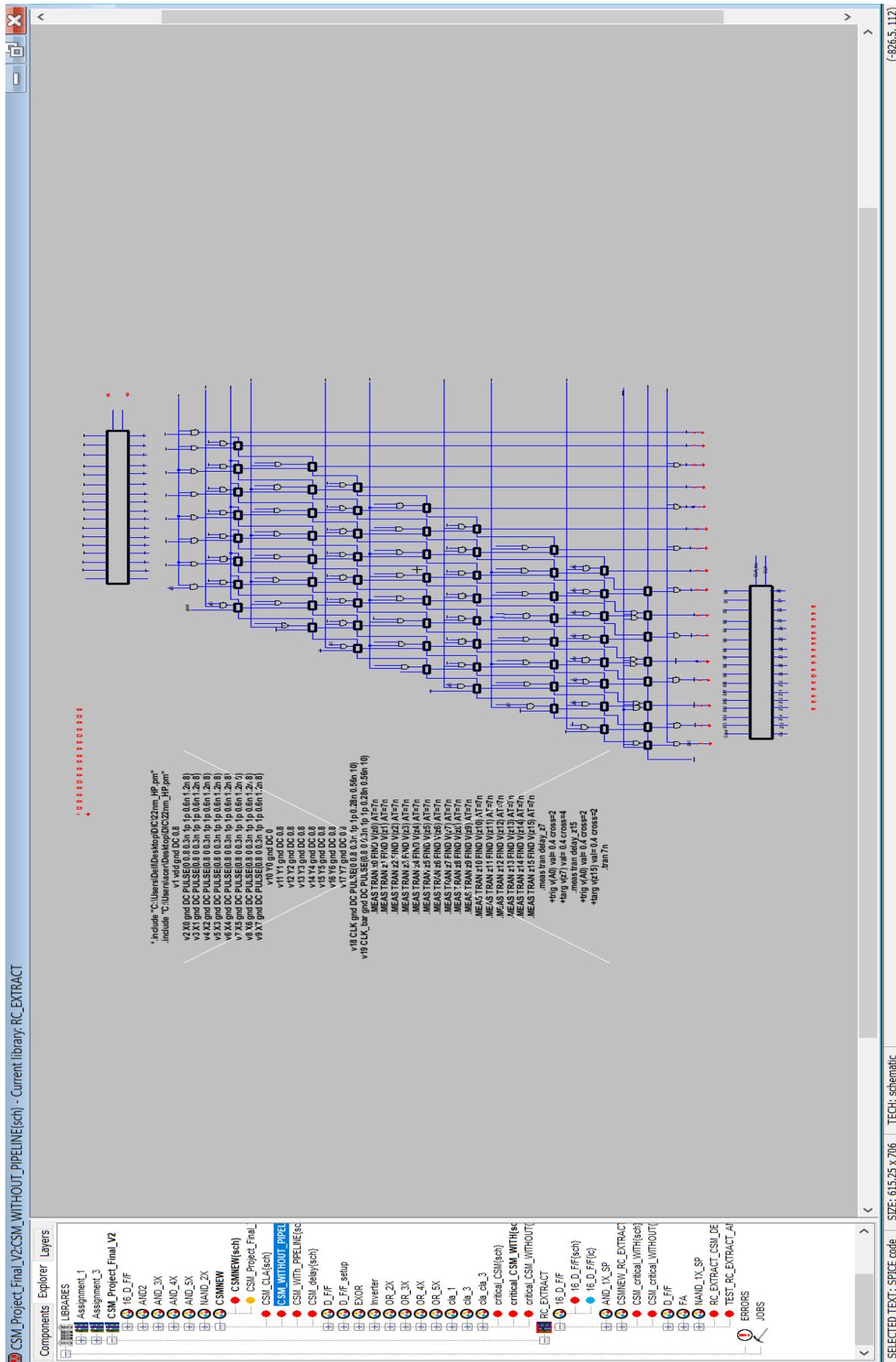
z0: v(z0)=7.01978e-005 at 7e-009
z1: v(z1)=4.94961e-005 at 7e-009
z2: v(z2)=0.799987 at 7e-009
z3: v(z3)=5.11325e-005 at 7e-009
z4: v(z4)=0.000102782 at 7e-009
z5: v(z5)=5.03365e-005 at 7e-009
z6: v(z6)=0.000102771 at 7e-009
z7: v(z7)=0.000137823 at 7e-009
z8: v(z8)=0.000103429 at 7e-009
z9: v(z9)=0.000135249 at 7e-009
z10: v(z10)=-0.000102333 at 7e-009
z11: v(z11)=0.00013532 at 7e-009
z12: v(z12)=0.000102336 at 7e-009
z13: v(z13)=0.000135465 at 7e-009
z14: v(z14)=0.000102865 at 7e-009
z15: v(z15)=0.000103728 at 7e-009
co: v(co)=0.00017094 at 7e-009

```

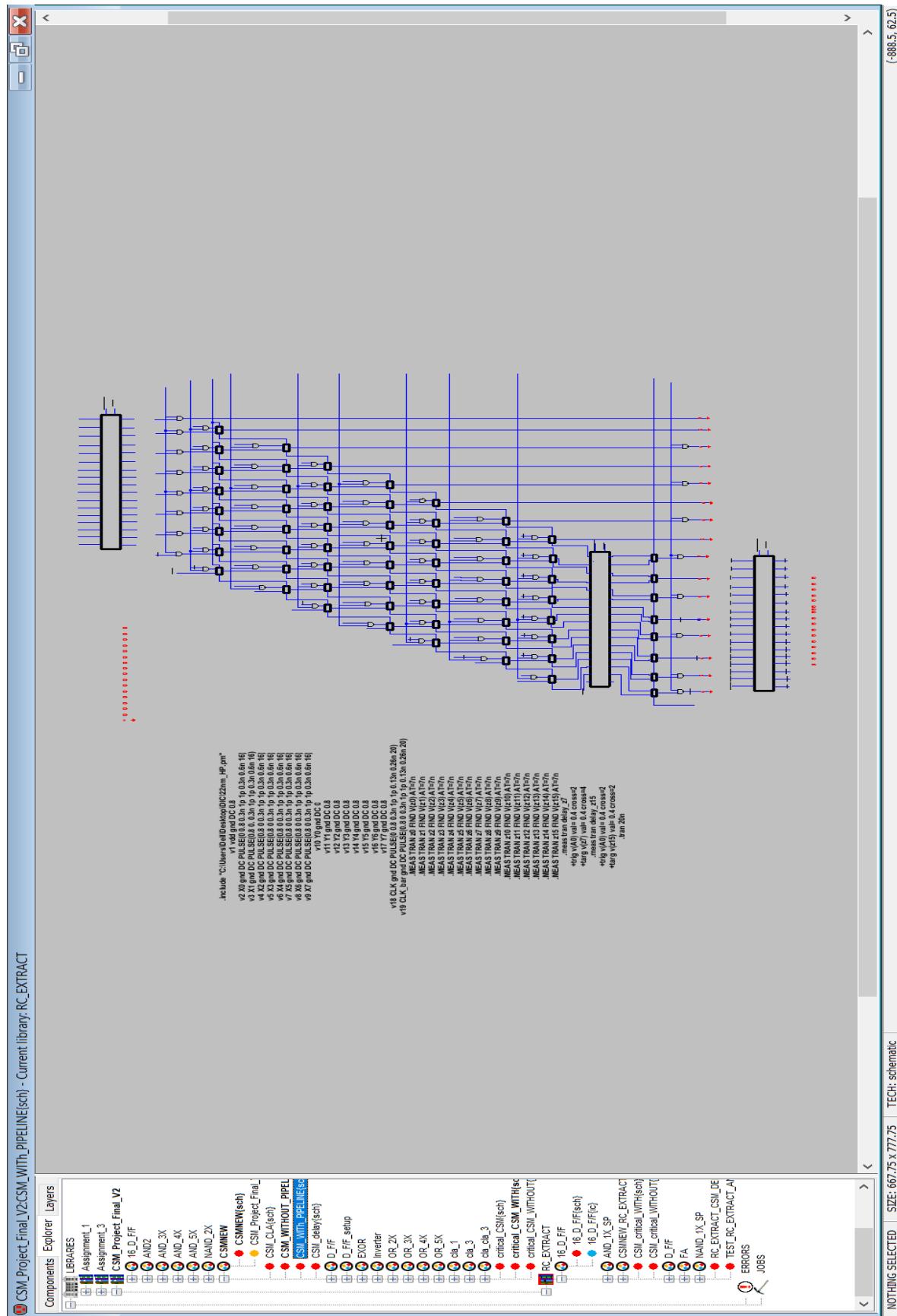
Date: Fri Dec 10 18:37:17 2021

Ready

➤ Schematic of 8-bit Unsigned CSM without pipeline –



➤ Schematic of 8-bit Unsigned CSM with pipeline –



❖ **Without RC Extract-**

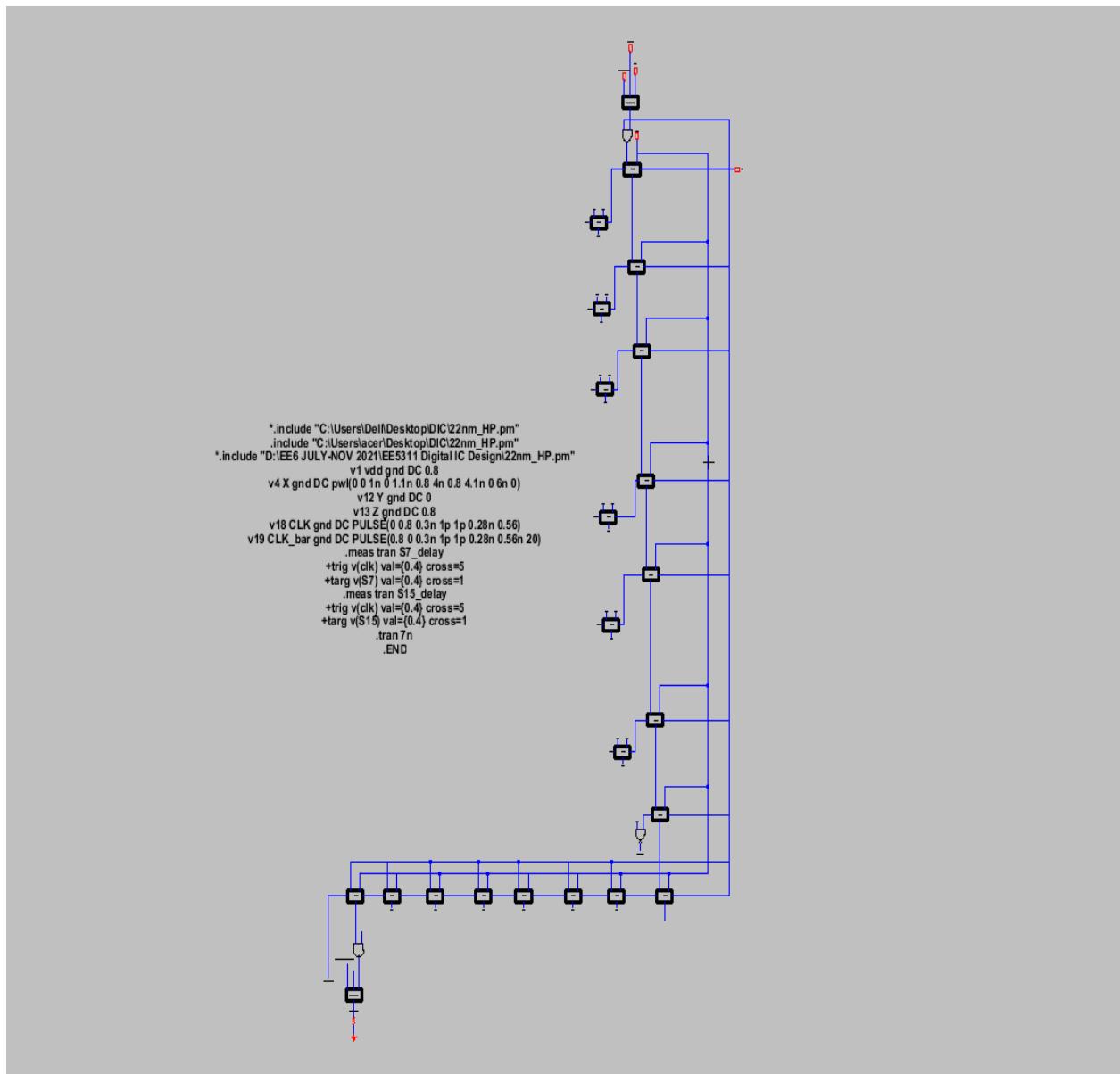
➤ **Maximum operating frequency of the CSM (without Pipeline)-**

To ensure CSM work satisfactorily clock frequency of D-Flop should be such that it should not contaminate CSM operation by feeding in new data while preceding data is being processed.

So, while determining maximum clock frequency of operation we should consider CSM for maximum delay i.e., critical path delay.

Total time taken in CSM without pipeline to reflect input to output is =
CSM delay + Initial Flop delay(T-Q) + Last Flop delay(T-Q).

So first we should calculate Critical path delay without pipeline –

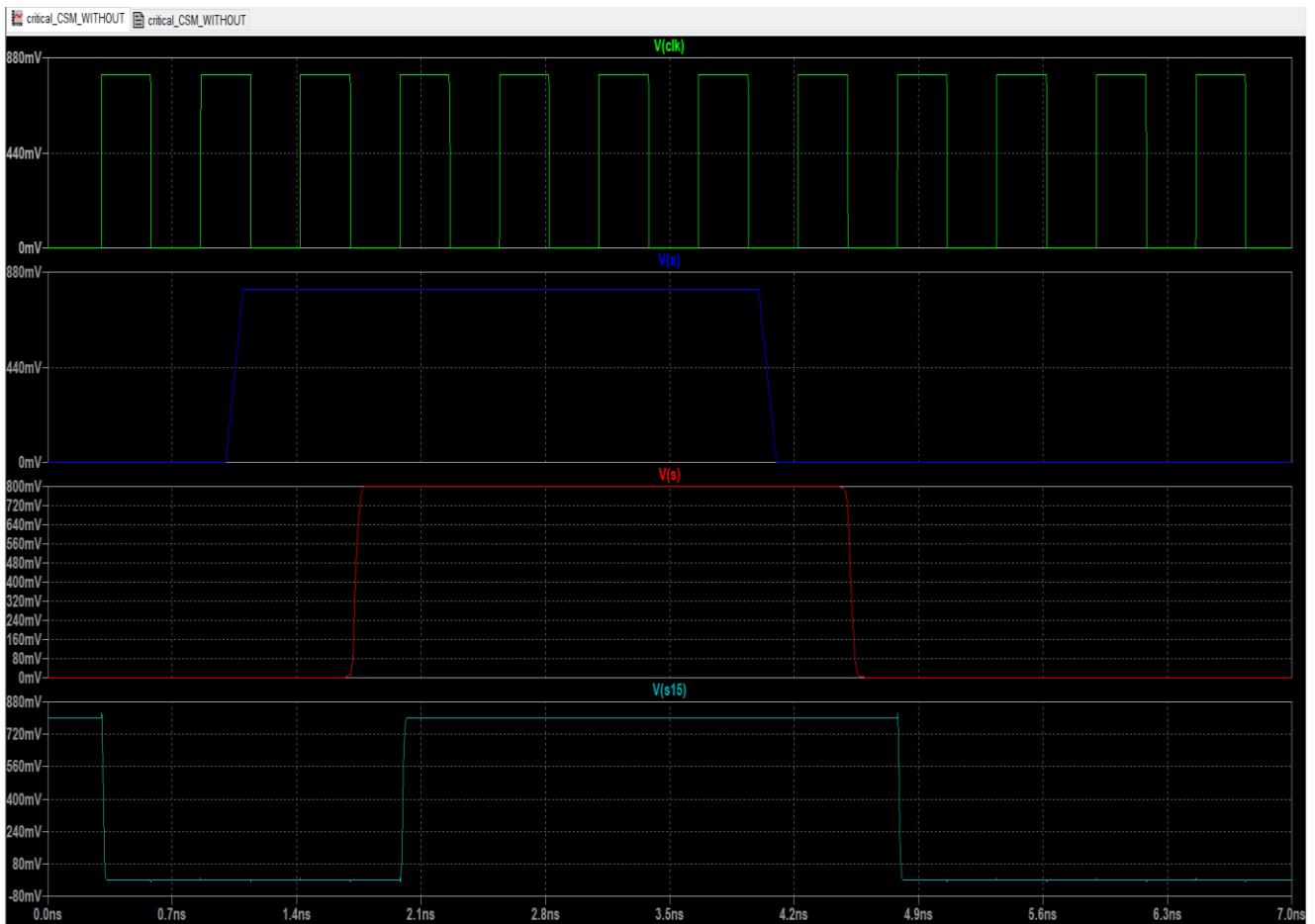


It is ensured that for change in X input will change all output bit to its complimentary value.

It is found that for CSM critical path **without Pipeline** is working satisfactorily for Clock Period = 0.56ns. (Frequency = 1.785 GHz)

MAXIMUM OUTPUT FREQUENCY WITHOUT PIPELINE (without RC) = 1.785 GHz

LTSPICE Result – Here S is input to vector merge block.



For above case S15 delay = Clock period + CLK-Q delay = 0.577ns

i.e., approx. CLK- Q delay = 11ps. We also verified this CLK-Q delay using D-FLOP test schematic.

From above it is clear that vector merge delay S15 Delay - S delay= 267ps.

So best place to place third flop is before vector merge.

S delay= 310ps, S15 delay = 267ps

CSM 1 delay = 310ps (S delay)

CSM 2 delay = 577—310 =267ps

Max (CSM1, CSM2) = 310ps

critical_CSM_WITHOUT critical_CSM_WITHOUT

```

XFA@92 Y Z net@1320 net@2017 gnd net@2014 vdd Assignment_3_FA
XFA@101 Y Z net@2014 net@1276 gnd net@714 vdd Assignment_3_FA
XFA@110 Y Z net@714 net@1261 gnd net@741 vdd Assignment_3_FA
XFA@119 Y Z net@741 net@1971 gnd S vdd Assignment_3_FA
XFA@120 Y Z S net@815 gnd net@2158 vdd Assignment_3_FA
XFA@121 Y net@776 Cout gnd net@1806 vdd Assignment_3_FA
XFA@122 Y net@837 Z net@776 gnd FA@122_S vdd Assignment_3_FA
XFA@123 Y net@1558 Z net@837 gnd FA@123_S vdd Assignment_3_FA
XFA@124 Y net@828 Z net@1558 gnd FA@124_S vdd Assignment_3_FA
XFA@125 Y net@1559 Z net@828 gnd FA@125_S vdd Assignment_3_FA
XFA@126 Y net@1557 Z net@1559 gnd FA@126_S vdd Assignment_3_FA
XFA@127 Y net@815 Z net@1557 gnd FA@127_S vdd Assignment_3_FA
XFA@128 FA@128 A net@1261 FA@128 Ci FA@128_Co gnd FA@128_S vdd Assignment_3_FA
XFA@129 FA@129_A net@1276 FA@129_Ci FA@129_Co gnd FA@129_S vdd Assignment_3_FA
XFA@130 FA@130_A net@2017 FA@130_Ci FA@130_Co gnd FA@130_S vdd Assignment_3_FA
XFA@131 FA@131_A net@2024 FA@131_Ci FA@131_Co gnd FA@131_S vdd Assignment_3_FA
XFA@132 FA@132_A net@2026 FA@132_Ci FA@132_Co gnd FA@132_S vdd Assignment_3_FA
XFA@133 FA@133_A net@2028 FA@133_Ci FA@133_Co gnd FA@133_S vdd Assignment_3_FA
XNAND_1X_061 vdd net@1806 gnd net@2155 vdd Assignment_1_NAND_1X_SP
XNAND_1X_062 net@1971 NAND_1X_062_B gnd NAND_1X_062_OUT vdd Assignment_1_NAND_1X_SP

* Spice Code nodes in cell 'CSM_Project_Final_V2:critical_CSM_WITHOUT(sch)'
*.include "C:\Users\Del\Desktop\DCIV22nm_HF.pm"
*.include "C:\Users\acer\Desktop\DCI\22nm_HP.pm"
*.include "D:\EE6 JULY-NOV 2021\EE5311 Digital IC Design\22nm_HP.pm"
v1 vdd gnd DC 0.8
v4 X gnd DC pw1(0 0n 0 1.n 0.8 4n 0.8 4.ln 0 6n 0)
v12 Y gnd DC 0
v13 Z gnd DC 0.8
v18 CLK gnd DC PULSE(0 0.8 0.3n 1p 1p 0.28n 0.56n 20)
v19 CLK_bar gnd DC PULSE(0.8 0 0.3n 1p 1p 0.28n 0.56n 20)
.meas tran S_delay
+trig v(clk) val={0.4} cross=5
+targ v(S) val={0.4} cross=1
.meas tran S15_delay
+trig v(clk) val={0.4} cross=5
+targ v(S15) val={0.4} cross=2
.tran 7n
.END
.EDN
```

SPICE Error Log: C:\Users\acer\Desktop\DCI\PROJECT\SAP\critical_CSM_WITHOUT.log

```

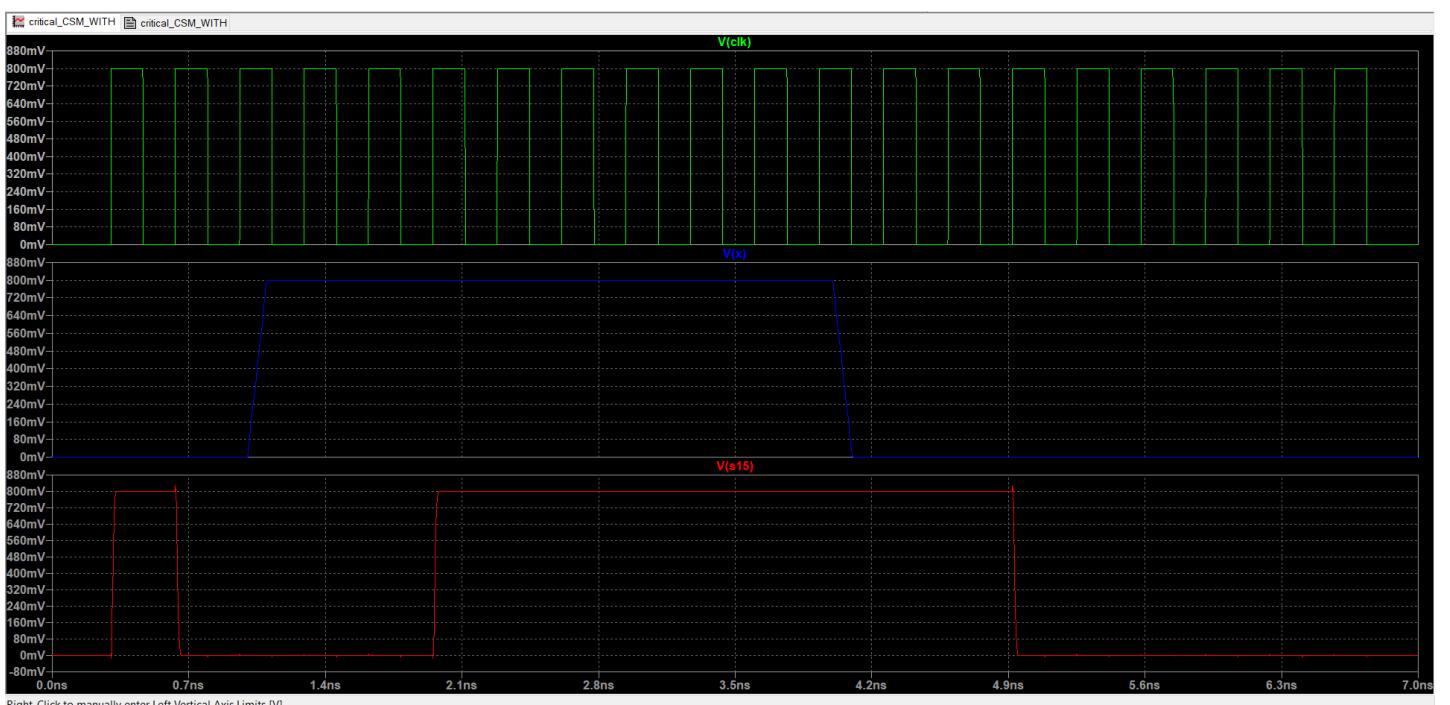
Starting source stepping with srcstepmethod=0
Source Step = 3.0303%
Source Step = 33.3333%
Source Step = 63.6364%
Source Step = 93.9394%
Source stepping succeeded in finding the operating point.

s1_delay=3.0995e-010 FROM 1.4205e-009 TO 1.73045e-009
s15_delay=5.77747e-010 FROM 1.4205e-009 TO 1.99825e-009

Date: Fri Dec 10 19:47:49 2021
Total elapsed time: 22.263 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 4885
traniter = 4196
trancopts = 1668
accept = 1535
rejected = 133
matrix size = 2532
fillins = 329
solver = Normal
Thread vector: 1122.0/589.6[8] 307.7/110.3[8] 207.3/136.3[8] 34.7/37.5[1] 2592/50
Matrix Compiler1: 424.21 KB object code size 516.1/199.1/[127.2]
```

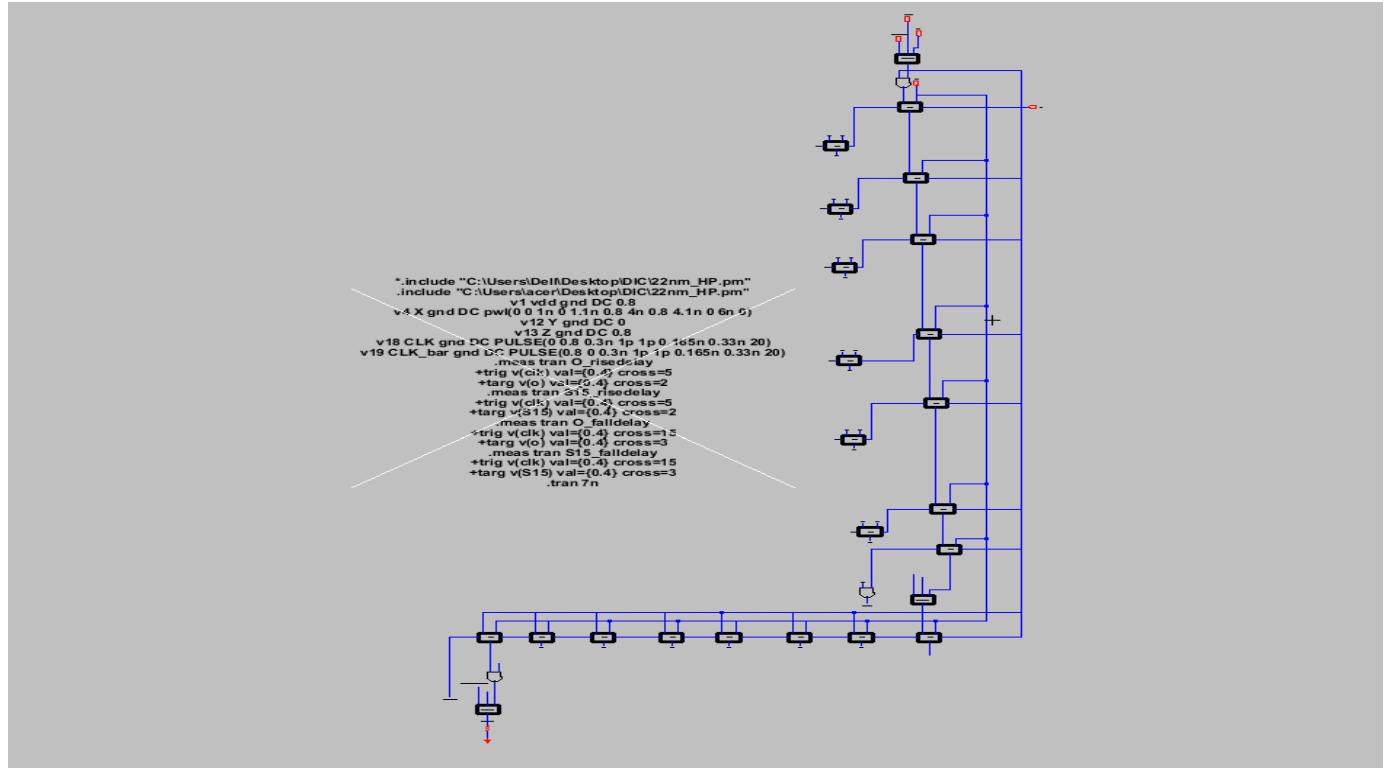
➤ Maximum operating frequency of the CSM (with Pipeline)-



Right-Click to manually enter Left Vertical Axis limits (V)

For above case S15 delay = 2*Clock period + CLK-Q delay = 0.669ns

It is observed that for T period of CLK = 0.33ns Critical CSM with pipeline working satisfactorily.



MAXIMUM CLOCK FREQUENCY WITH PIPELINE (without RC) = 3.03 GHz

```

critical_CSM_WITH critical_CSM_WITH
XFA@73 Y Z net@691 net@2026 gnd net@1090 vdd Assignment_3_FA
XFA@82 Y Z net@1090 net@2024 gnd net@1320 vdd Assignment_3_FA
XFA@92 Y Z net@1320 net@2017 gnd net@2014 vdd Assignment_3_FA
XFA@101 Y Z net@2014 net@1276 gnd net@714 vdd Assignment_3_FA
XFA@110 Y Z net@714 net@1261 gnd net@741 vdd Assignment_3_FA
XFA@119 Y Z net@741 net@1971 gnd net@2168 vdd Assignment_3_FA
XFA@120 Y Z net@2160 net@815 gnd vdd Assignment_3_FA
XFA@121 Y net@876 Z Cout gnd net@1806 vdd Assignment_3_FA
XFA@122 Y net@837 Z net@876 gnd FA@122_S vdd Assignment_3_FA
XFA@123 Y net@1558 Z net@837 gnd FA@123_S vdd Assignment_3_FA
XFA@124 Y net@828 Z net@1558 gnd FA@124_S vdd Assignment_3_FA
XFA@125 Y net@1559 Z net@828 gnd FA@125_S vdd Assignment_3_FA
XFA@126 Y net@1557 Z net@1559 gnd FA@126_S vdd Assignment_3_FA
XFA@127 Y net@815 Z net@1557 gnd FA@127_S vdd Assignment_3_FA
XFA@128 FA@128_A net@1261 FA@128_Ci FA@128_Co gnd FA@128_S vdd Assignment_3_FA
XFA@129 FA@129_A net@1276 FA@129_Ci FA@129_Co gnd FA@129_S vdd Assignment_3_FA
XFA@130 FA@130_A net@2017 FA@130_Ci FA@130_Co gnd FA@130_S vdd Assignment_3_FA
XFA@131 FA@131_A net@2024 FA@131_Ci FA@131_Co gnd FA@131_S vdd Assignment_3_FA
XFA@132 FA@132_A net@2026 FA@132_Ci FA@132_Co gnd FA@132_S vdd Assignment_3_FA
XFA@133 FA@133_A net@2028 FA@133_Ci FA@133_Co gnd FA@133_S vdd Assignment_3_FA
XNAND_1X_#61 vdd net@1806 gnd net@2155 vdd Assignment_1_NAND_1X_SP
XNAND_1X_#62 net@1971 NAND_1X_#62_B gnd NAND_1X_#62_OUT vdd Assignment_1_NAND_1X_SP

* Spice Code nodes in cell cell 'CSM_Project_Final_V2:critical_CSM_WITH(sch)'
*.include "C:\Users\acer\Desktop\DI\22nm_HP.pm"
.include "C:\Users\acer\Desktop\DI\22nm_HP.pm"
v1 vdd gnd DC 0.8
v4 X gnd DC pw1(0 0 1n 0 1n 0.8 4n 0.8 4.ln 0 6n 0)
v12 Y gnd DC 0
v13 gnd DC 0
v18 CLK gnd DC PULSE(0 0.8 0.3n 1p 0 165n 0.33n 20)
v19 CLK_bar gnd DC PULSE(0.8 0 0.3n 1p 1p 0 165n 0.33n 20)
.meas tran S15_risedelay
+trig v(clk) val=0.4 cross=7
+trig v(S15) val=0.4 cross=3
.meas tran S15_falldelay
+trig v(clk) val=0.4 cross=13
+trig v(S15) val=0.4 cross=4
+trig v(S15) val=0.4 cross=4
.tran 7n
.END

```

SPICE Error Log: C:\Users\acer\Desktop\DI\PROJECT\SAP\critical_CSM_WITH.log

```

Gmin = 0.000142725
Gmin = 1.5325e-005
vernier = 0.5
vernier = 0.25
Gmin = 0
Gmin stepping aborted per request.

Starting source stepping with srcstepmethod=0
Source Step = 3.03038
Source Step = 33.33338
vernier = 0.25
Source stepping aborted.
Starting source stepping with srcstepmethod=1
Source Step = 3.03038
Source Step = 33.33338
Source Step = 63.63648
Source Step = 93.93948
Source stepping succeeded in finding the operating point.

s15_risedelay=6.69676e-010 FROM 1.2905e-009 TO 1.96018e-009
s15_falldelay=2.65083e-009 FROM 2.2805e-009 TO 4.93133e-009

Date: Fri Dec 10 20:20:13 2021
Total elapsed time: 236.301 seconds.

tnom = 27
tmax = 27

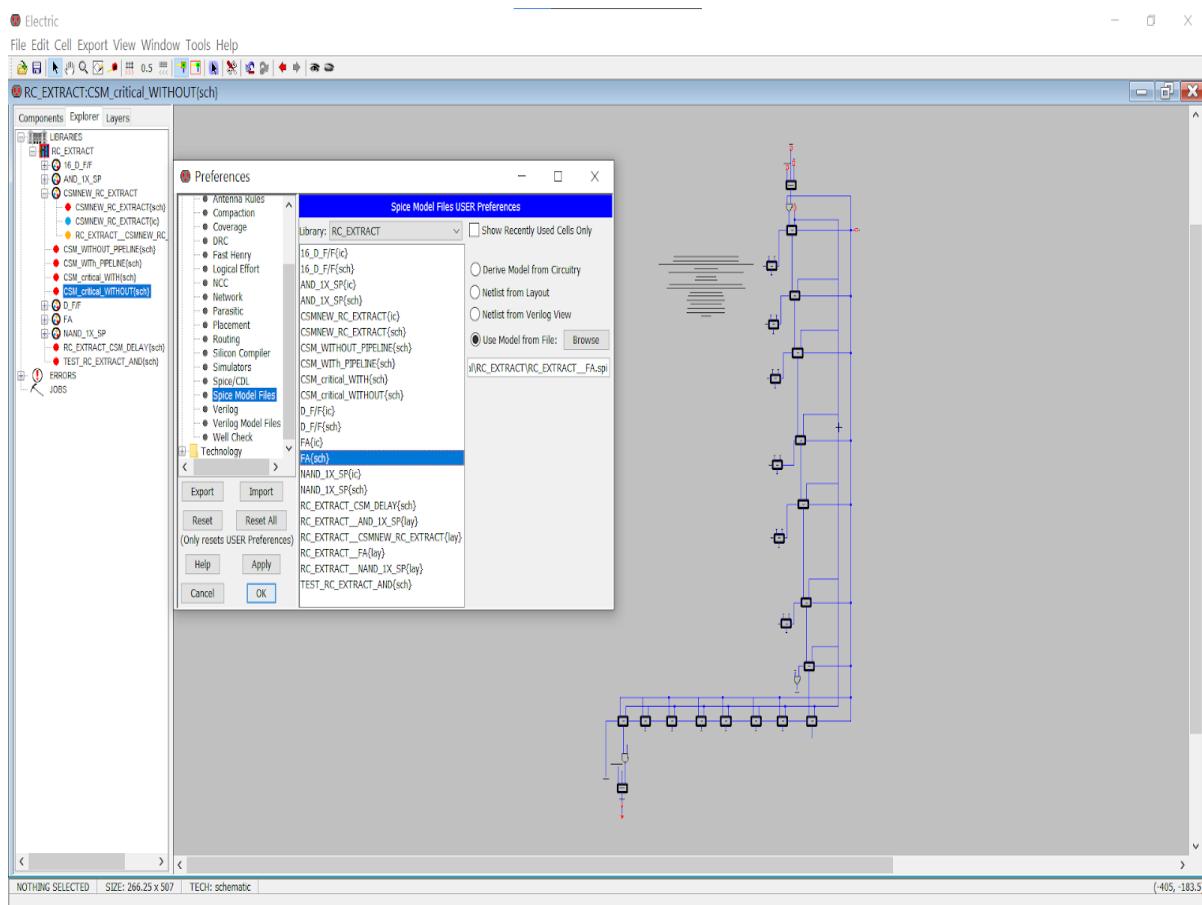
```

❖ With RC Extract-

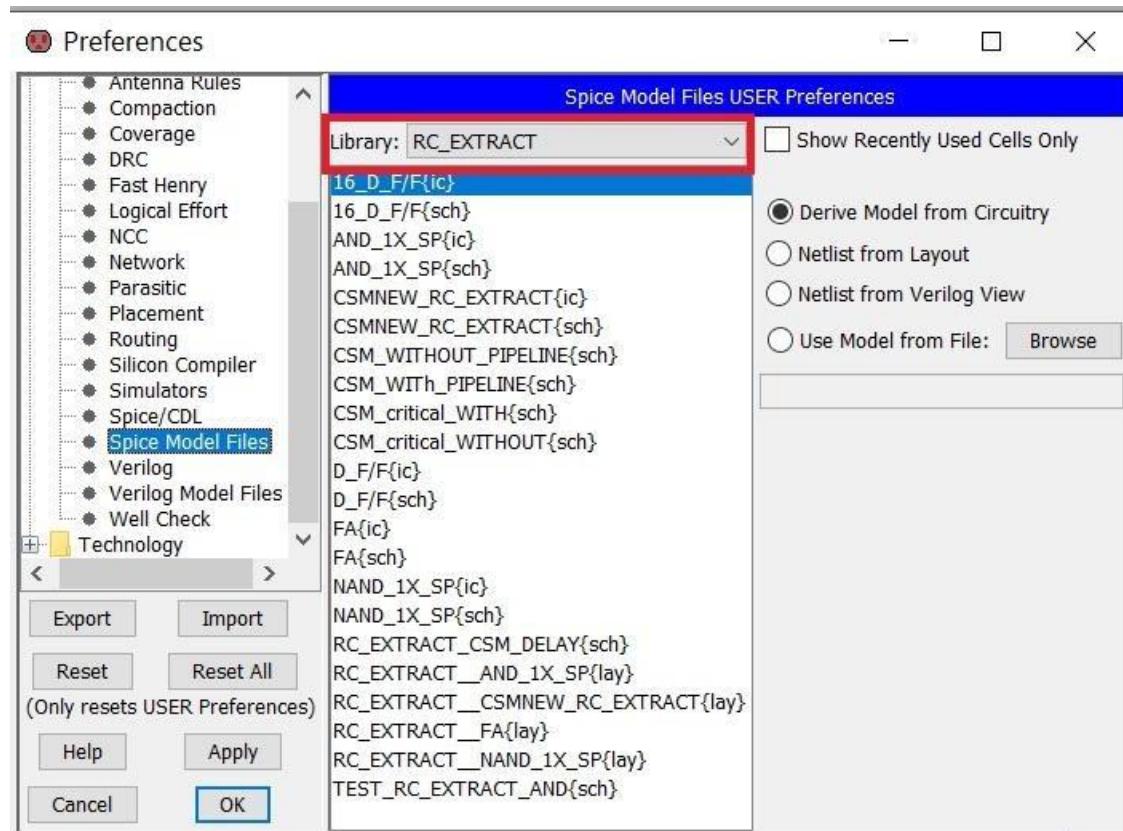
If we measure individual block delays and add them up to get the entire schematic delay, we cannot assure accurate values as loading effects of multiple Full Adders' inputs will not be considered. Instead, we can use individual block extracted RC netlist model files to measure delays in Spice simulation.

How did we calculate RC Extracted Netlist Delay in Electric using individual Blocks' (NAND, AND, Full Adder) RC extracted netlist .spi files?

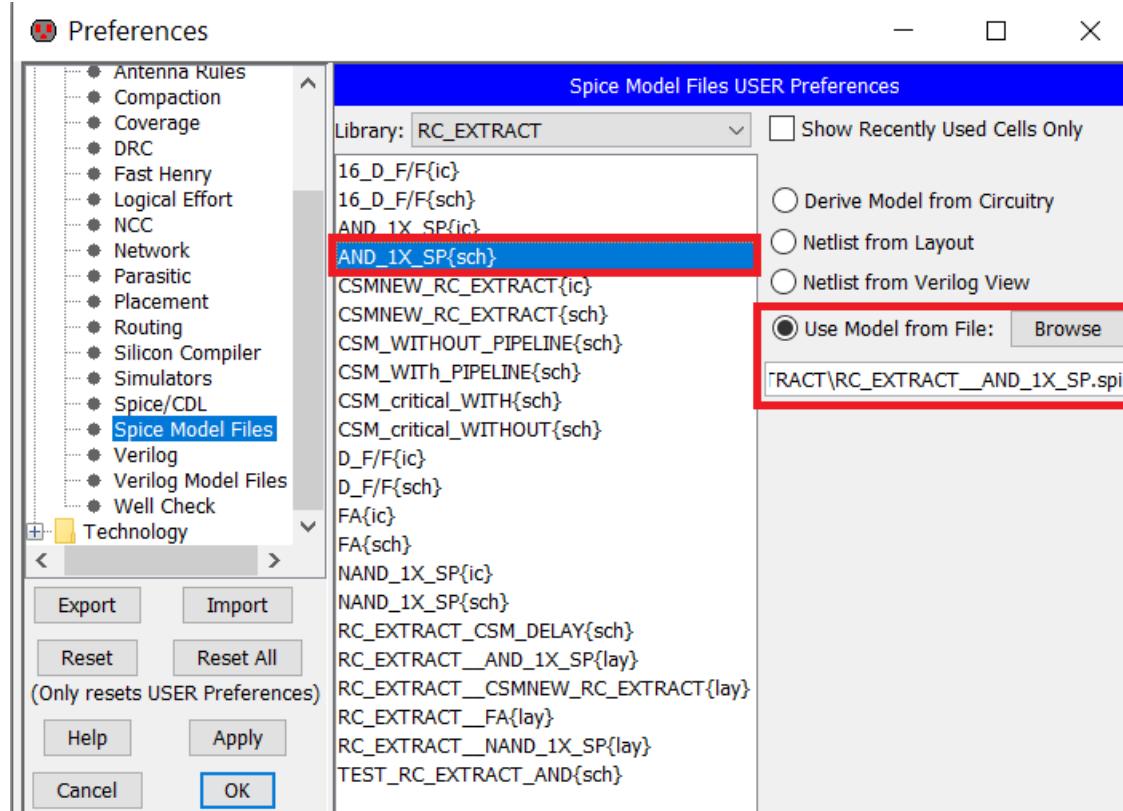
1. We copied all necessary groups which include schematic, layout and icon and extracted the RC Netlists for all individual blocks as per instructions given and instantiated desired icons in required schematic.

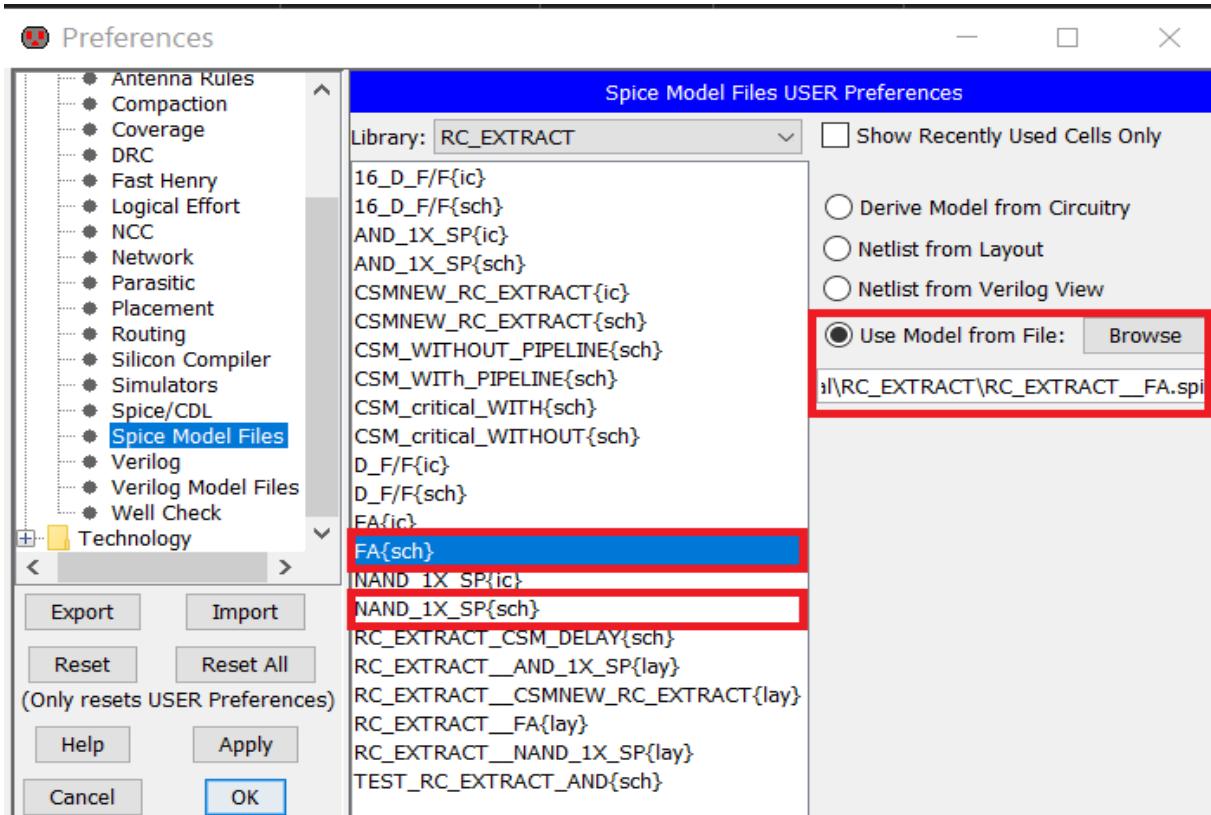


2. For using RC extracted netlist model files we headed to File-> Preferences-> Tools-> Spice Model Files as shown below. One can see all used schematics and icon views in the same library.



3. Then we selected respective extracted RC netlist files for schematics of NAND, AND and Full Adder as shown below.





4. We then ran the Spice simulation to calculate the rise and fall delays for Critical Path schematic with and without Pipelined schematics. One can ensure the model files used in simulation are Extracted RC Netlist of each individual blocks in the LTPICE console.

```

LTPICE XVII - (CSM_critical_WITHOUT)
File Edit View Simulate Tools Window Help
D:\EE6 JULY-NOV 2021\EE5311 Digital IC Design\Project Files\Final\Fully Final\RC_EXTRACT\RC_EXTRACT_FA.spi

*** SPICE deck for cell 'CSM_critical WITHOUT{sch}' from library 'RC_EXTRACT'
*** Created on Tue Nov 30, 2021 14:57:39
*** Last revised on Thu Dec 09, 2021 15:22:00
*** Written on Fri Dec 10, 2021 16:29:19 by Electric VLSI Design System, version 9.07
*** Layout tech: mocomos, foundry MOSIS
*** UC SPICE *** , MIN_RESIST 4.0, MIN_CAPAC 0.01FF

* cell 'AND_IX_SP{sch}' is described in this file:
.include D:\EE6 JULY-NOV 2021\EE5311 Digital IC Design\Project Files\Final\Fully Final\RC_EXTRACT\RC_EXTRACT_AND_IX_SP.spi

*** SUBCIRCUIT RC_EXTRACT_D_F/F FROM CELL D_F/F{sch}
.SUBCKT RC_EXTRACT_D_F/F CLK CLK_bar D gnd Q vdd
Mmos0 net@2 CLK net@5 gnd nmos L=0.022U W=0.044U
Mmos02 net@114 CLK_bar net@5 gnd nmos L=0.022U W=0.044U
Mmos03 net@226 CLK_bar net@22 gnd nmos L=0.022U W=0.044U
Mmos04 net@204 CLK net@22 gnd nmos L=0.022U W=0.044U
Mmos06 net@114 D gnd gnd nmos L=0.022U W=0.044U
Mmos09 net@154 net@5 gnd gnd nmos L=0.022U W=0.044U
Mmos0@10 net@2 net@154 gnd gnd nmos L=0.022U W=0.044U
Mmos0@11 net@226 Q gnd gnd nmos L=0.022U W=0.044U
Mmos0@12 net@204 net@154 gnd gnd nmos L=0.022U W=0.044U
Mmos0@13 Q net@22 gnd gnd nmos L=0.022U W=0.044U
Mpmos0 net@0 CLK_bar net@2 vdd pmos L=0.022U W=0.088U
Mpmos1 net@0 CLK net@114 vdd pmos L=0.022U W=0.088U
Mpmos2 net@22 CLK net@26 vdd pmos L=0.022U W=0.088U
Mpmos3 net@22 CLK_bar net@204 vdd pmos L=0.022U W=0.088U
Mpmos4 vdd D net@114 vdd pmos L=0.022U W=0.088U
Mpmos7 vdd net@154 vdd pmos L=0.022U W=0.088U
Mpmos8 vdd net@154 net@2 vdd pmos L=0.022U W=0.088U
Mpmos9 vdd Q net@26 vdd pmos L=0.022U W=0.088U
Mpmos@10 vdd net@154 net@204 vdd pmos L=0.022U W=0.088U
Mpmos@11 vdd net@22 Q vdd pmos L=0.022U W=0.088U
.ENDS RC_EXTRACT_D_F/F

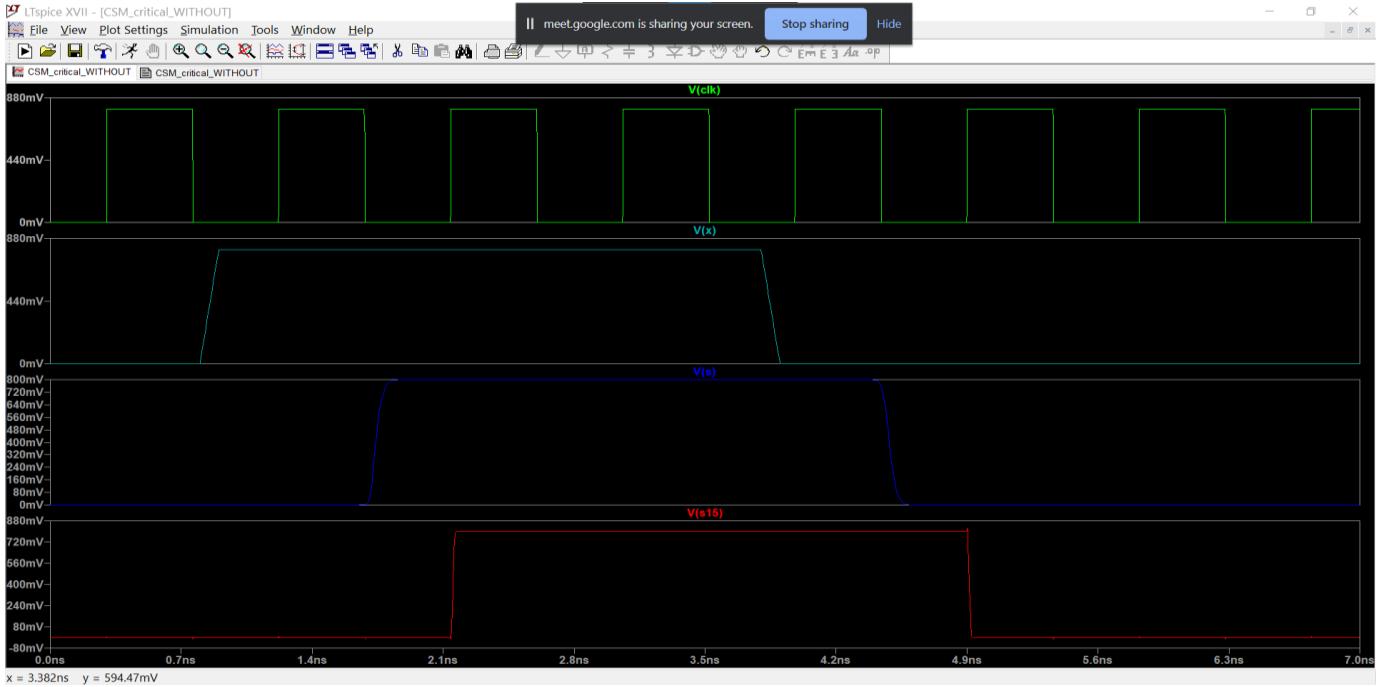
* cell 'FA{sch}' is described in this file:
.include D:\EE6 JULY-NOV 2021\EE5311 Digital IC Design\Project Files\Final\Fully Final\RC_EXTRACT\RC_EXTRACT_FA.spi

* cell 'NAND_IX_SP{sch}' is described in this file:
.include D:\EE6 JULY-NOV 2021\EE5311 Digital IC Design\Project Files\Final\Fully Final\RC_EXTRACT\RC_EXTRACT_NAND_IX_SP.spi

*** TOP LEVEL CELL: CSM_critical WITHOUT{sch}
Ries@0 315 qnd 100MEG

```

➤ Maximum operating frequency of the CSM (without Pipeline)-



It is found that for CSM critical path **without Pipeline** is working satisfactorily for Clock Period = 0.92ns. (Frequency = 1.0869 GHz)

MAXIMUM OUTPUT FREQUENCY WITHOUT PIPELINE (with RC) = 1.0869 GHz

```

LTspice XVII - [CSM_critical_WITHOUT]
File Edit View Simulate Tools Window Help
File Edit View Simulate Tools Window Help
CSM_critical_WITHOUT CSM_critical_WITHOUT
XFA@121 net@776 Z Cout gnd net@1806 vdd RC EXTRACT_FA
XFA@122 Y net@937 Z net@776 gnd FA@122_S vdd RC EXTRACT_FA
XFA@123 Y net@1558 Z net@8837 gnd FA@123_S vdd RC EXTRACT_FA
XFA@124 Y net@828 Z net@1558 gnd FA@124_S vdd RC_EXTRACT_FA
XFA@125 Y net@1559 Z net@8828 gnd FA@125_S vdd RC_EXTRACT_FA
XFA@126 Y net@1557 Z net@81559 gnd FA@126_S vdd RC_EXTRACT_FA
XFA@127 Y net@815 Z net@1557 gnd FA@127_S vdd RC_EXTRACT_FA
XFA@128 FA@128_A net@1261 FA@128_C1 FA@128_Co gnd FA@128_S vdd RC_EXTRACT_FA
XFA@129 FA@129_A net@1276 FA@129_C1 FA@129_Co gnd FA@129_S vdd RC_EXTRACT_FA
XFA@130 FA@130_A net@2017 FA@130_C1 FA@130_Co gnd FA@130_S vdd RC_EXTRACT_FA
XFA@131 FA@131_A net@2024 FA@131_C1 FA@131_Co gnd FA@131_S vdd RC_EXTRACT_FA
XFA@132 FA@132_A net@2026 FA@132_C1 FA@132_Co gnd FA@132_S vdd RC_EXTRACT_FA
XFA@133 FA@133_A net@2028 FA@133_C1 FA@133_Co gnd FA@133_S vdd RC_EXTRACT_FA
XNAND_1X_@61 vdd net@1806 gnd net@2155 vdd RC_EXTRACT_NAND_1X_SP
XNAND_1X_@62 net@1971 NAND_1X_@62_B gnd NAND_1X_@62_OUT vdd RC_EXTRACT_NAND_1X_SP
* Spice Code nodes in cell cell 'CSM_critical_WITHOUT{sch}'
*.include "C:\Users\DELL\Desktop\DIGIC\22nm_HP.pm"
*.include "C:\Users\acer\Desktop\DIGIC\22nm_HP.pm"
*.include "D:\EE6 JULY-NOV 2021\EE5311 Digital IC Design\22nm_HP.pm"
v1 vdd gnd DC 0.8
v4 X gnd DC PWL(0 0 0.8n 0 0.9n 0.8 3.8n 0.8 3.9n 0 5.8n 0)
v12 Y gnd DC 0
v13 Z gnd DC 0.8
v18 CLK gnd DC PULSE(0 0.8 0.3n 1p 1p 0.46n 0.92n 20)
v19 CLK_bar gnd DC PULSE(0.8 0 0.3n 1p 1p 0.46n 0.92n 20)
.meas tran S15_risedelay
+trig v(clk) val=(0.4) cross=3
+targ v(S15) val=(0.4) cross=1
.meas tran S15_falldelay
+trig v(clk) val=(0.4) cross=9
+targ v(S15) val=(0.4) cross=2
.meas tran S_risedelay
+trig v(clk) val=(0.4) cross=3
+targ v(S) val=(0.4) cross=1
.meas tran S_falldelay
+trig v(clk) val=(0.4) cross=9
+targ v(S) val=(0.4) cross=2
.tran 7n
.END

Ready

```

SPICE Error Log: D:\EE6 JULY-NOV 2021\EE5311 Digital IC Design\22nm_HP.pm

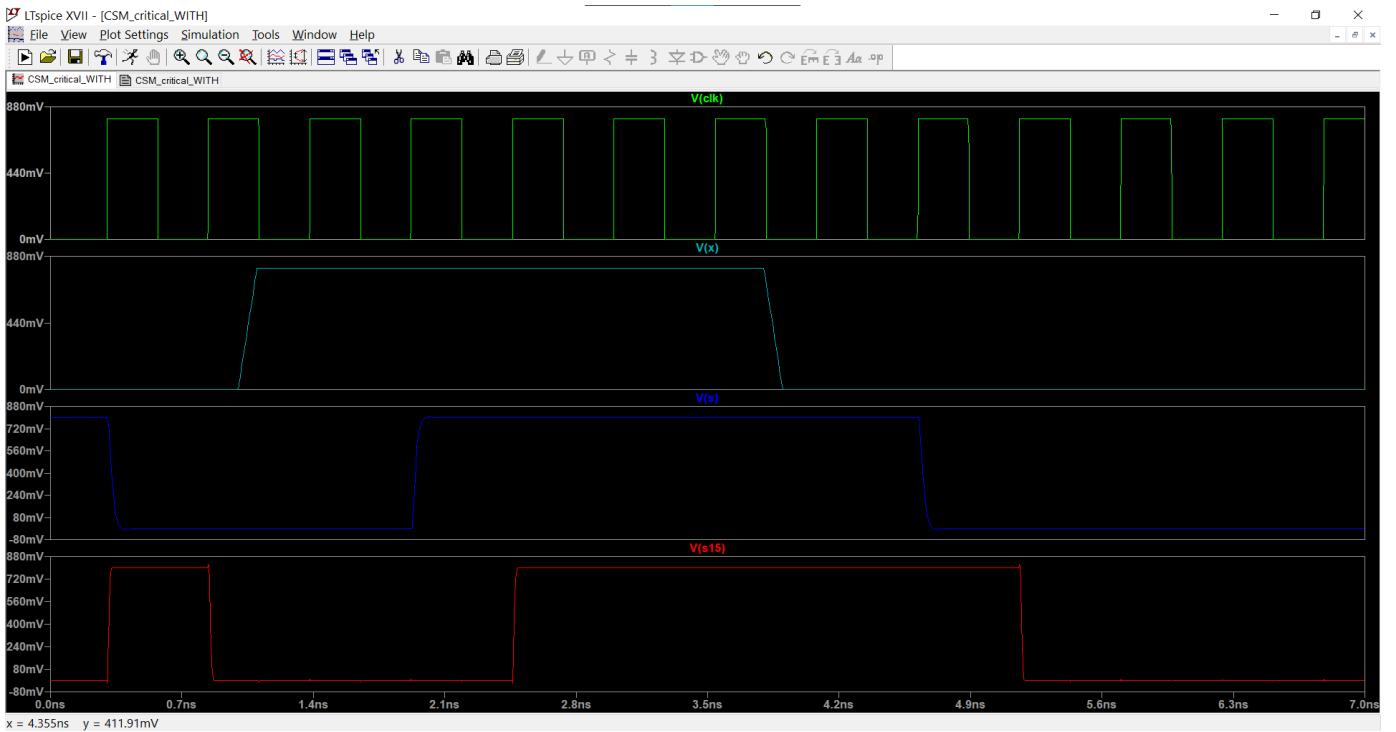
Source stepping succeeded in finding the operating point.

s15_risedelay=9.31847e-010 FROM 1.2205e-009 TO 2.15235e-009
s15_falldelay=9.30873e-010 FROM 3.9805e-009 TO 4.91137e-009
s_risedelay=5.19187e-010 FROM 1.2205e-009 TO 1.73969e-009
s_falldelay=5.04242e-010 FROM 3.9805e-009 TO 4.48474e-009

Date: Fri Dec 10 20:30:04 2021
Total elapsed time: 586.328 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 4742
traniter = 3500
tranpoints = 1395
accept = 1306
rejected = 89
matrix size = 5942
fillins = 15821
solver = Normal
Thread vector: 2991.9/1191.7[8] 234.5/99.5[8] 158.9/88.8[8] 229.2/97.0[8] 2592/50
Matrix Compiler1: 2.35 MB object code size 1075.5/669.2/[632.8]
Matrix Compiler2: 927.52 KB object code size 682.5/512.0/[288.6]

➤ Maximum operating frequency of the CSM (with Pipeline)-



It is found that for CSM critical path **with Pipeline** is working satisfactorily for
Clock Period = 0.54ns. (Frequency = 1.8518 GHz)

MAXIMUM OUTPUT FREQUENCY WITH PIPELINE (with RC) = 1.8518 GHz

```

LTspice XVII - [CSM_critical_WITH]
File Edit View Plot Settings Simulation Tools Window Help
CSM_critical_WITH CSM_critical_WITH
V(clk)
V(x)
V(s)
V(s15)
0.0ns 0.7ns 1.4ns 2.1ns 2.8ns 3.5ns 4.2ns 4.9ns 5.6ns 6.3ns 7.0ns
x = 4.355ns y = 411.91mV

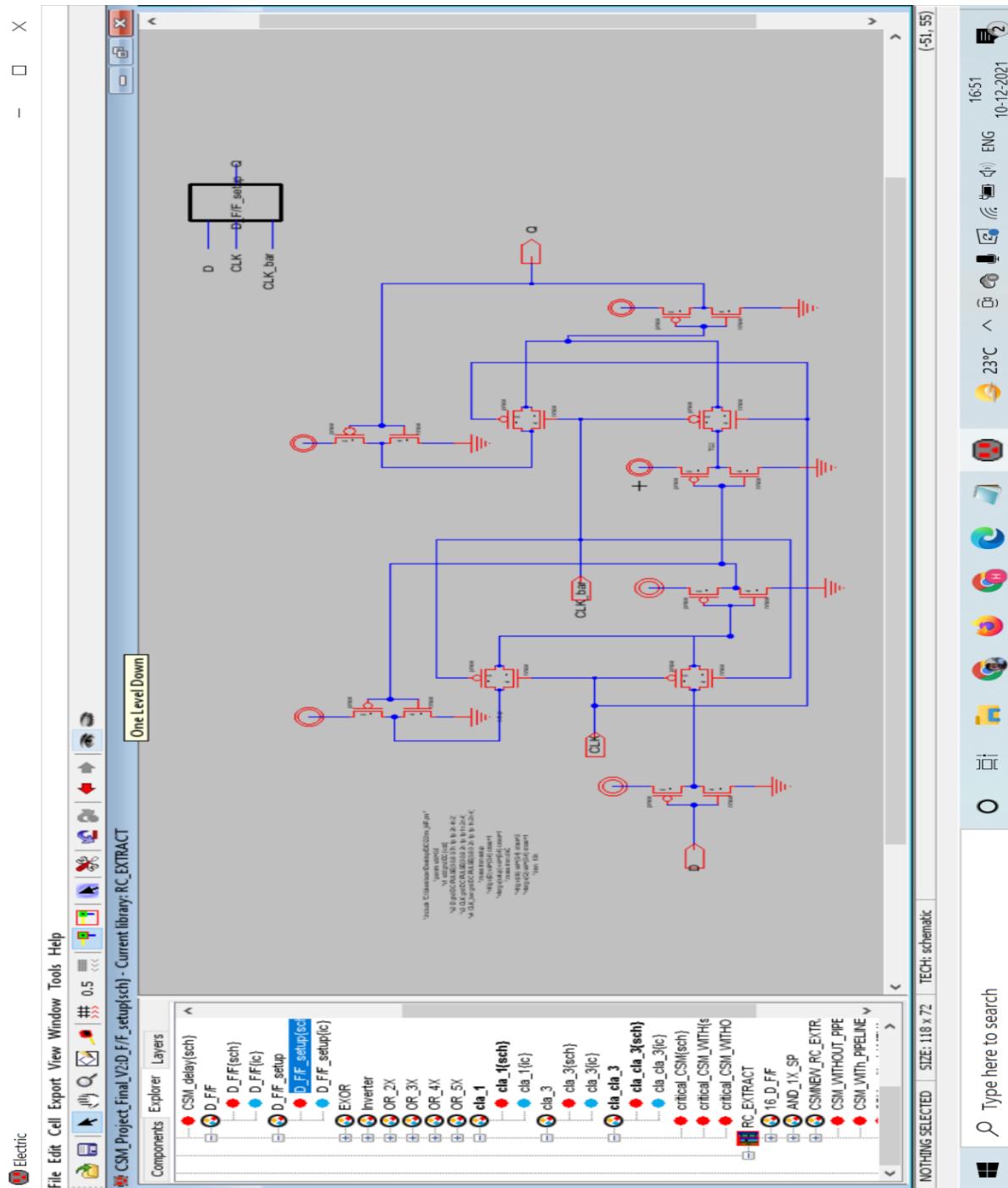
XFA@121 Y net@8776 Z Cout gnd net@1806 vdd RC_EXTRACT_FA
XFA@122 Y net@8837 Z net@776 gnd FA@122_S vdd RC_EXTRACT_FA
XFA@123 Y net@1558 Z net@837 gnd FA@123_S vdd RC_EXTRACT_FA
XFA@124 Y net@828 Z net@1558 gnd FA@124_S vdd RC_EXTRACT_FA
XFA@125 Y net@1559 Z net@828 gnd FA@125_S vdd RC_EXTRACT_FA
XFA@126 Y net@1557 Z net@1557 gnd FA@126_S vdd RC_EXTRACT_FA
XFA@127 Y net@815 Z net@1555 gnd FA@127_S vdd RC_EXTRACT_FA
XFA@128 FA@128_A net@1261 FA@128_Ci FA@128_Co gnd FA@128_S vdd RC_EXTRACT_FA
XFA@129 FA@129_A net@1276 FA@129_Ci FA@129_Co gnd FA@129_S vdd RC_EXTRACT_FA
XFA@130 FA@130_A net@2017 FA@130_Ci FA@130_Co gnd FA@130_S vdd RC_EXTRACT_FA
XFA@131 FA@131_A net@2024 FA@131_Ci FA@131_Co gnd FA@131_S vdd RC_EXTRACT_FA
XFA@132 FA@132_A net@2026 FA@132_Ci FA@132_Co gnd FA@132_S vdd RC_EXTRACT_FA
XFA@133 FA@133_A net@2028 FA@133_Ci FA@133_Co gnd FA@133_S vdd RC_EXTRACT_FA
XNAND_IX_@61 Vdd net@1806 gnd net@2140 vdd RC_EXTRACT_NAND_IX_SP
XNAND_IX_@62 net@1971 NAND_IX_@62_B gnd NAND_IX_@62_OUT vdd RC_EXTRACT_NAND_IX_SP

* Spice Code nodes in cell 'CSM_critical WITH(sch)'
*.include "D:\EE6 JULY-NOV 2021\EE5311_Digital IC Design\22nm_HP.pmc"
*.include "C:/Users/Dell/Desktop/DIC/22nm_HP.pmc"
*.include "C:/Users/acer/Desktop/DIC/22nm_HP.pmc"
v1 vdd gnd DC 0.8
v4 X gnd DC pw1(0 0n 0 1.1n 0.8 3.8n 0.8 3.9n 0 6n 0)
v12 Y gnd DC 0
v13 Z gnd DC 0.8
v18 CLK gnd DC PULSE(0 0.8 0.3n 1p 1p 0.27n 0.540n 20)
v19 CLK_bar gnd DC PULSE(0.8 0 0.3n 1p 1p 0.27n 0.540n 20)
.meas tran S15_risedelay
+trig v(clk) val={0.4} cross=5
+targ v(S15) val={0.4} cross=3
.meas tran S15_falldelay
+trig v(clk) val={0.4} cross=15
+targ v(S15) val={0.4} cross=4
.meas tran S_risedelay
+trig v(clk) val={0.4} cross=5
+targ v(S) val={0.4} cross=2
.meas tran S_falldelay
+trig v(clk) val={0.4} cross=15
+targ v(S) val={0.4} cross=3
.tran 7n
.END

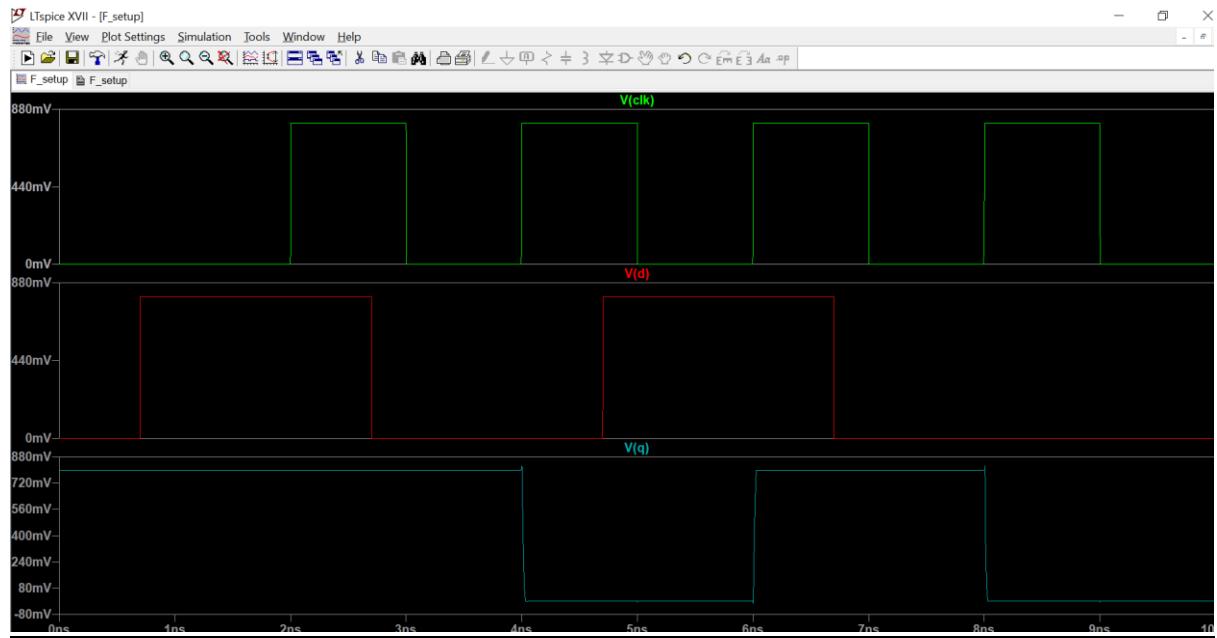
Ready
```

➤ D-Flip SETUP time and CLK-Q time calculation-

❖ Schematic-



LTSPICE Simulation showing functionality of D-FLOP-



SET-UP TIME= 21.64ps, CLK-Q TIME = 11.58ps

17 input D-Flop IC is generated for ease of use in CSM circuit.

```

X SPICE Error Log: C:\Users\Del\Downloads\F_setup.log
Circuit: *** SPICE deck for cell D_F/F_setup{sch} from library CSM_Project_Fi
Direct Newton iteration for .op point succeeded.

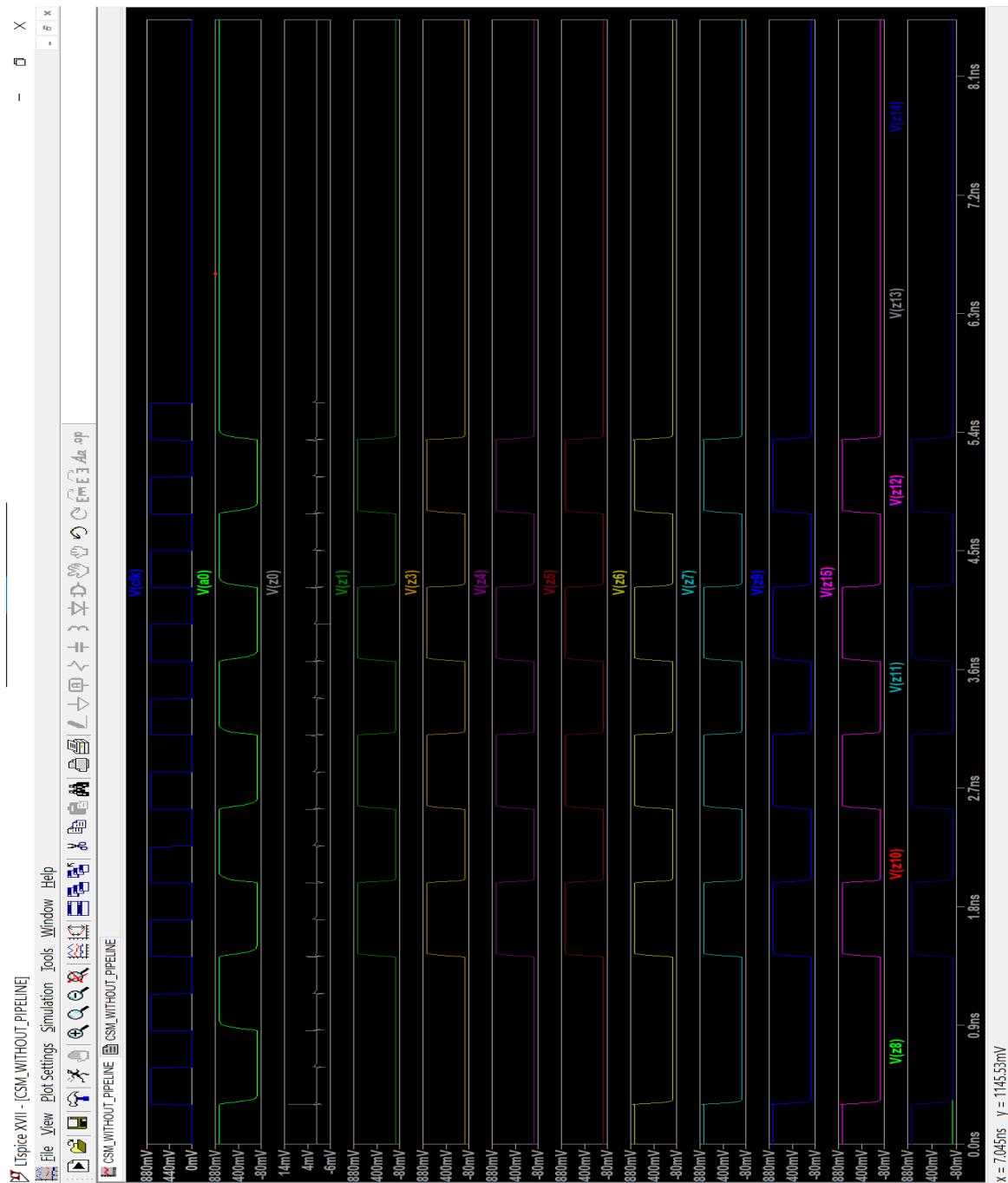
setup_delay=2.1643e-011 FROM 7.005e-010 TO 7.22143e-010
clk_q_delay=1.15877e-011 FROM 4.0005e-009 TO 4.01209e-009

Date: Fri Dec 10 16:56:16 2021
Total elapsed time: 0.416 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 3138
traniter = 3108
tranpoints = 1370
accept = 1282
rejected = 88
matrix size = 96
fillins = 2
solver = Normal
Thread vector: 83.2/28.4[2] 15.4/11.9[2] 2.1/6.9[1] 0.6/40.0[1] 2592/500
Matrix Compiler1: 13.25 KB object code size 26.2/6.3/[1.7]
Matrix Compiler2: 12.10 KB object code size 4.2/15.2/[0.7]
```

We have verified the functionality of CSM (with RC netlist and schematic) for above frequencies for with and without pipeline.

Given below the CSM schematic (without RC) without pipeline functioning correctly for Clock Frequency = 1.785GHz i.e., T period of clock = 0.56ns in LTSPICE-



Given below the CSM schematic (without RC) with pipeline functioning correctly for Clock Frequency = 3.03GHz i.e., T period of clock = 0.33ns in LTSPICE

A screenshot of a Windows desktop environment. In the center, there is a window titled 'PSpice XVII - [CSM_WITH_PIPELINE]' displaying a Spice simulation log. The log shows the following content:

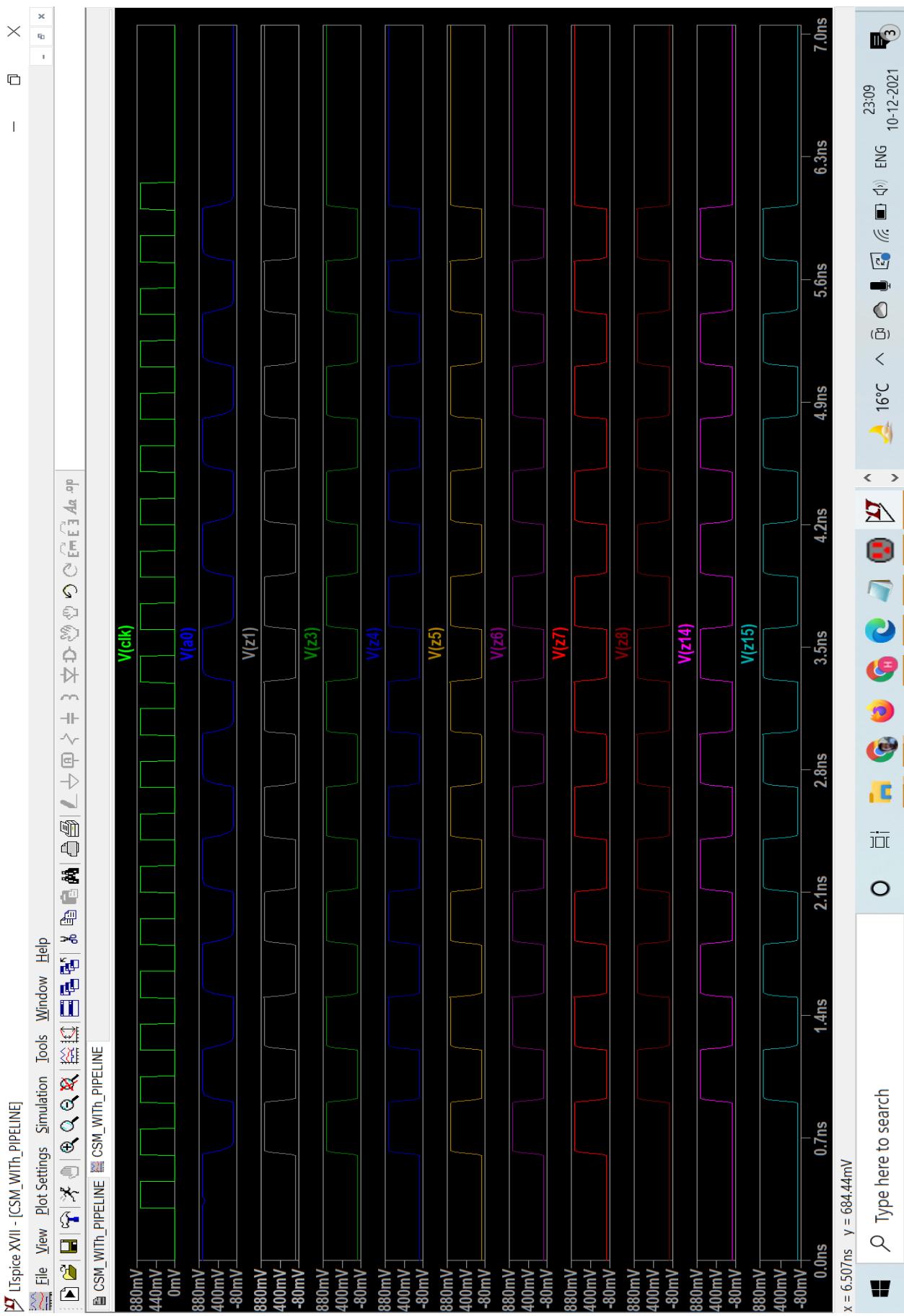
```
* Spice Code nodes in cell cell 'CSM WITH PIPELINE{sch}'
#include "C:\Users\DELL\Desktop\DC\22nm_HP.pmc

V1 V1 vdd gnd DC 0 8
V2 X0 gnd DC PULSE(0 0.8 0.2n 1p 0.3n 0.6n 16)
V3 X1 gnd DC PULSE(0 0.8 0.2n 1p 0.3n 0.6n 16)
V4 X2 gnd DC PULSE(0 0.8 0.2n 1p 0.3n 0.6n 16)
V5 X3 gnd DC PULSE(0 0.8 0.2n 1p 0.3n 0.6n 16)
V6 X4 gnd DC PULSE(0 0.8 0.2n 1p 0.3n 0.6n 16)
V7 X5 gnd DC PULSE(0 0.8 0.2n 1p 0.3n 0.6n 16)
V8 X6 gnd DC PULSE(0 0.8 0.2n 1p 0.3n 0.6n 16)
V9 X7 gnd DC PULSE(0 0.8 0.2n 1p 0.3n 0.6n 16)

V10 Y0 gnd DC 0
V11 Y1 gnd DC 0.8
V12 Y2 gnd DC 0.8
V13 Y3 gnd DC 0.8
V14 Y4 gnd DC 0.8
V15 Y5 gnd DC 0.8
V16 Y6 gnd DC 0.8
V17 Y7 gnd DC 0.8
V18 CLK gnd DC PULSE(0 0.8 0.3n 1p 1p 0.15n 0.3n 20)
V19 CLK_bar gnd DC PULSE(0 0.8 0.3n 1p 1p 0.15n 0.3n 20)

.meas tran delay Z7
+trig v(clk) val= 0.4 CROSS=6
+trig v(z7) val= 0.4 CROSS=4
.meas tran delay Z15
+trig v(clk) val= 0.4 CROSS=6
+trig v(z15) val= 0.4 CROSS=4
.tran 10n
.END
```

The right side of the screen shows the Windows taskbar with various pinned icons and the system tray at the bottom.



➤ **SPICE simulation showing comparison between ripple carry adder VS Carry look ahead adder for vector merge block in 8-bit signed CSM**

- Theory behind CARRY LOOK AHEAD ADDER-

We define two variables as ‘carry generate’ “ G_i ” and ‘carry propagate’ “ P_i ” then

$$P_i = A_i \oplus B_i$$

$$G_i = A_i \cdot B_i$$

The sum output and carry output can be expressed in terms of carry generate “ G_i ” and carry propagate “ P_i ” as

$$\begin{aligned} S_i &= P_i \oplus C_i \\ C_{i+1} &= G_i + P_i \cdot C_i \end{aligned}$$

$$C_1 = G_0 + P_0 \cdot C_0$$

$$C_2 = G_2 + P_2 \cdot C_2$$

$$C_3 = G_3 + P_3 \cdot C_3$$

$$C_4 = G_4 + P_4 \cdot C_4$$

$$C_5 = G_5 + P_5 \cdot C_5$$

$$C_6 = G_6 + P_6 \cdot C_6$$

$$C_7 = G_7 + P_7 \cdot C_7$$

Substituting C_1 into C_2 , then C_2 into C_3 , and so on yields the following expanded equations:

$$C_1 = (C_0 \cdot P_0 + G_0)$$

$$C_2 = (C_0 \cdot P_0 \cdot P_1 + P_1 \cdot G_0 + G_1)$$

$$C_3 = (C_0 \cdot P_0 \cdot P_1 \cdot P_2 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot G_1 + G_2)$$

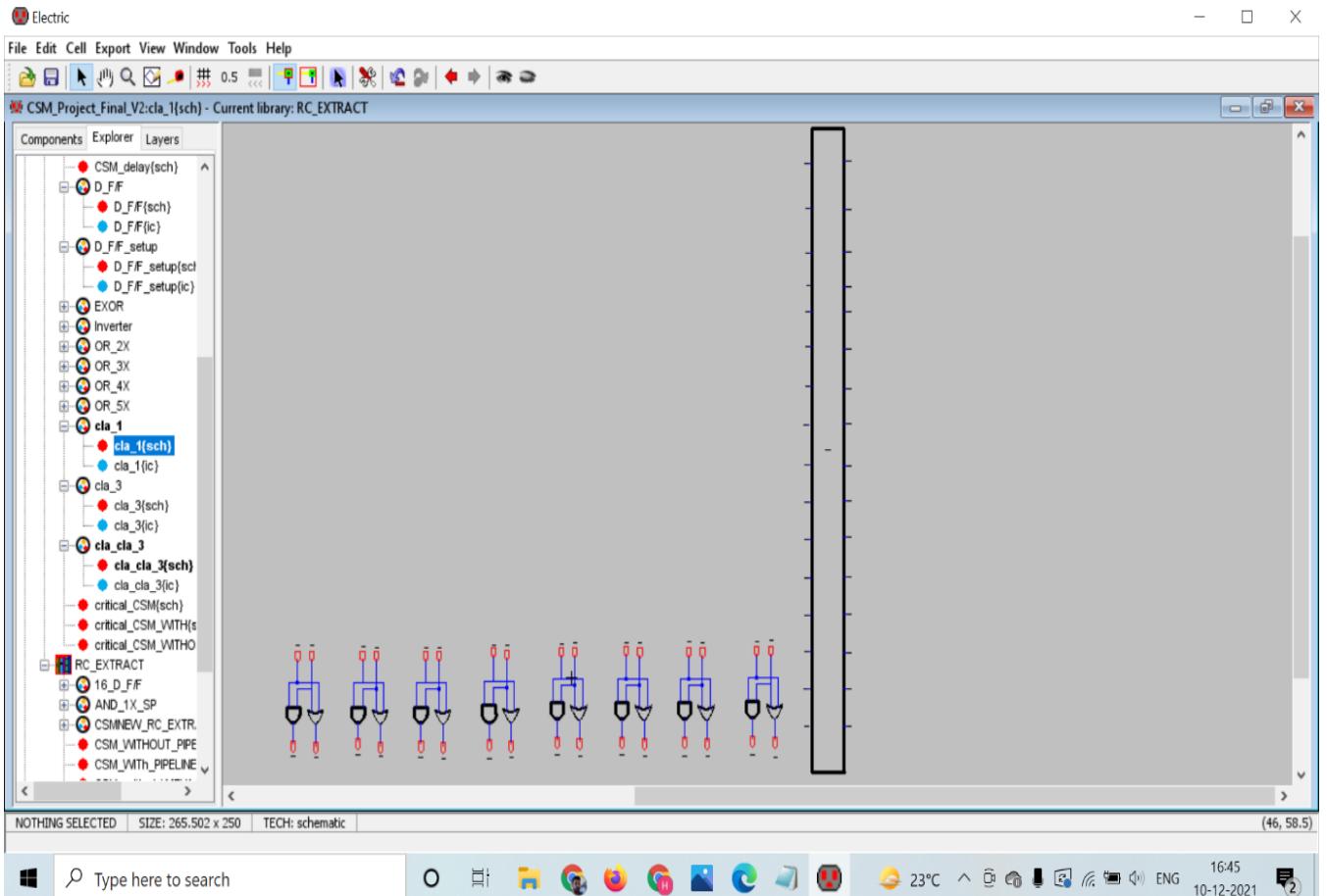
$$C_4 = (C_0 \cdot P_0 \cdot P_1 \cdot P_2 \cdot P_3 + P_3 \cdot P_2 \cdot P_1 \cdot G_0 + P_3 \cdot P_2 \cdot G_1 + G_2 \cdot P_3 + G_3)$$

$$C_5 = (C_0 \cdot P_0 \cdot P_1 \cdot P_2 \cdot P_3 + P_3 \cdot P_2 \cdot P_1 \cdot G_0 + P_3 \cdot P_2 \cdot G_1 + G_2 \cdot P_3 + G_3)P_4 + G_4$$

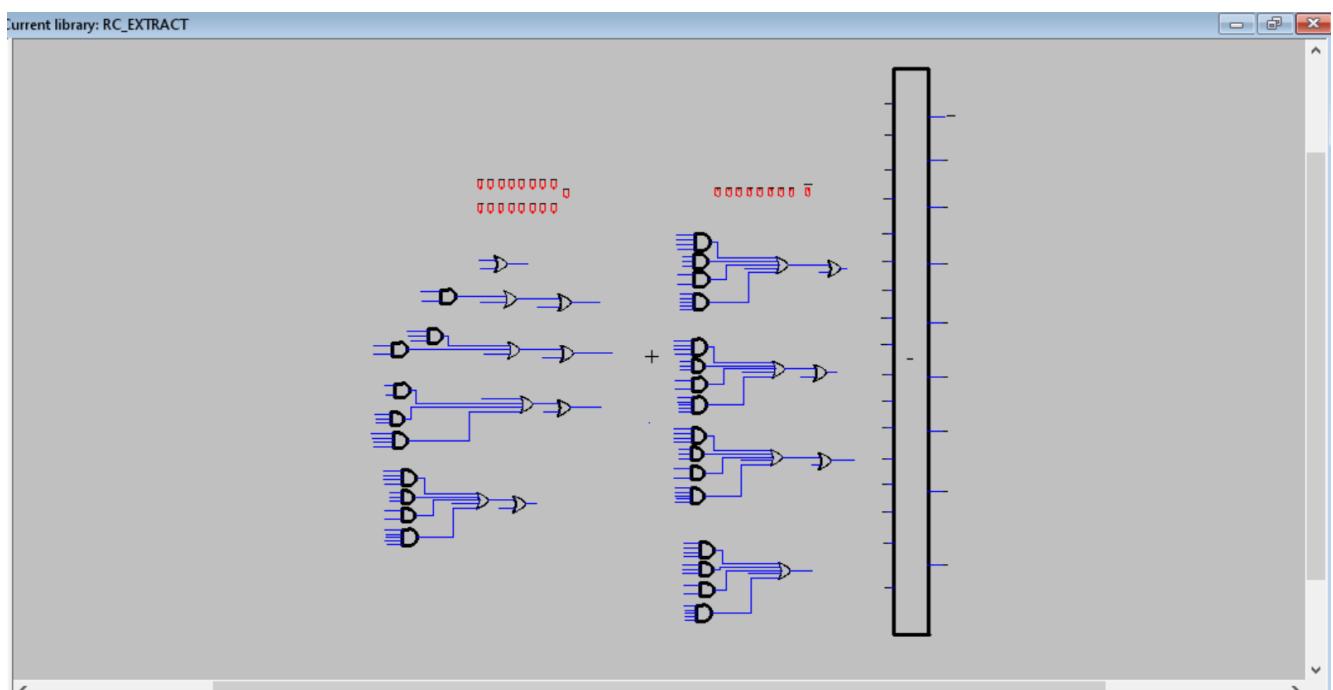
$$C_6 = ((C_0 \cdot P_0 \cdot P_1 \cdot P_2 \cdot P_3 + P_3 \cdot P_2 \cdot P_1 \cdot G_0 + P_3 \cdot P_2 \cdot G_1 + G_2 \cdot P_3 + G_3)P_4 + G_4)P_5 + G_5$$

$$C_7 = ((C_0 \cdot P_0 \cdot P_1 \cdot P_2 \cdot P_3 + P_3 \cdot P_2 \cdot P_1 \cdot G_0 + P_3 \cdot P_2 \cdot G_1 + G_2 \cdot P_3 + G_3)P_4 + G_4)P_5 + G_5).P_6 + G_6$$

Propagation and generation bits (Gi & Pi) generation



Sum and Carry generation using Gi & Pi-



❖ LTSPICE Simulation-

CSM WITH RIPPLE CARRY ADDER-

Z15 Delay = 406ps, Z7 Delay = 232.82ps,
Ripple carry adder delay as a vector merge = 173.18ps

A screenshot of a Spice simulation interface, likely HSPICE or a similar tool. The main window shows a terminal-like interface with the following content:

```
Uspice XVII - [CSMNEW]
File Edit View Simulate Tools Window Help
[Icons] CSMNEW

* Spice Code nodes in cell cell 'CSMNEW[sch]'
*.include "C:\Users\DeLL\Desktop\Dic\22nm_HP.pm"
*.include "C:\Users\acer\Desktop\Dic\22nm_HP.pm"

V1 vdd gnd DC 0.8
V2 A0 gnd DC PULSE(0 0.8 2n 1p 4n 8n 2)
V3 A1 gnd DC PULSE(0 -0.8 0 2n 1p 4n 8n 2)
V4 A2 gnd DC PULSE(0 -0.8 0 2n 1p 4n 8n 2)
V5 A3 gnd DC PULSE(0 -0.8 0 2n 1p 4n 8n 2)
V6 A4 gnd DC PULSE(0 -0.8 0 2n 1p 4n 8n 2)
V7 A5 gnd DC PULSE(0 -0.8 0 2n 1p 4n 8n 2)
V8 A6 gnd DC PULSE(0 -0.8 0 2n 1p 4n 8n 2)
V9 A7 gnd DC PULSE(0 -0.8 0 2n 1p 4n 8n 2)
V10 B0 gnd DC 0
V11 B1 gnd DC 0.8
V12 B2 gnd DC 0.8
V13 B3 gnd DC 0.8
V14 B4 gnd DC 0.8
V15 B5 gnd DC 0.8
V16 B6 gnd DC 0.8
V17 B7 gnd DC 0.8
.VTRAN delay_z7 WITHOUT CLA
+trig v(A0) val=0.4 cross=2
+trig v(z7) val=0.4 cross=4
.meas tran delay_z15 WITHOUT CLA
+trig v(A0) val=0.4 cross=2
+trig v(z15) val=0.4 cross=2
.tran 10n
.END

Circuit: *** SPICE deck for cell CSMNEW[sch] from library CSM_Project_Final_V^
Starting Gmin stepping
Gmin = 1.07374
Gmin = 0.115292
Gmin = 0.0123794
Gmin = 0.00132923
Gmin = 0.00142725
Gmin = 1.5325e-005
Gmin = 1.6455e-006
Gmin = 1.76685e-007
Gmin = 1.89714e-008
Gmin = 2.03704e-009
Gmin = 2.18725e-010
Gmin = 2.34854e-011
Gmin = 2.52173e-012
Gmin = 2.70769e-013
Gmin = 0
Gmin stepping succeeded in finding the operating point.

delay_z7 without clia=2.32816e-010 FROM 6.0015e-009 TO 6.23432e-009
delay z15 without clia=4.05599e-010 FROM 6.0015e-009 TO 6.4071e-009

Date: Fri Dec 10 20:11:37 2021
Total elapsed time: 66.889 seconds.
```

The interface includes a toolbar with various icons for file operations, simulation, and analysis. The status bar at the bottom right shows the date and time as 10-12-2021 20:11, along with system status icons like battery level, signal strength, and temperature (18°C).

CSM WITH CARRY LOOK AHEAD ADDER-

Z15 Delay = 389.25ps, Z7 Delay = 226.03ps,

CARRY LOOK AHEAD ADDER delay as a vector merge = 163.22ps

CLA DELAY = 163.22ps is less than RIPPLE CARRY ADDER DELAY = 173.18ps

```

[X:\spiceXVII - [CSM_CLA]] File Edit View Simulate Tools Window Help
[X:\spiceXVII - [CSM_CLA]] CSM_CLA CSM_CLA

XNAND 1X @61 net@2214 vdd gnd Z15 vdd Assignment 1 NAND 1X SP
Xcla_1@0 net@2178 net@2181 net@2185 net@2188 net@2191 net@2194 net@2195 net@2196 gnd net@2198 net@2200 net@2202 net@2204 net@2206 net@2208 net@2230 net@2178 net@2181 net@2185 net@2188 net@2191 net@2194 net@2195 net@2196 and net@2198 net@2200 net@2202 net@2204 net@2208
[X:\spiceXVII - [CSM_CLA]] CSM_Error.log C:\Users\DeLL\Downloads\CSM_CLA\log
[X:\spiceXVII - [CSM_CLA]] CSM_Error.log C:\Users\DeLL\Downloads\CSM_CLA\log

Circuit: *** SPICE deck for cell CSM_CLA{sch} from library CSM_Project_Final_
Direct Newton iteration failed to find .op point. (Use ".option noopter" to
Starting Gmin stepping
Gmin = 10
Gmin = 1.07374
Gmin = 0.115292
Gmin = 0.0123794
Gmin = 0.00132923
Gmin = 0.00142725
Gmin = 1.5325e-005
Gmin = 1.6455e-006
Gmin = 1.76685e-007
Gmin = 1.89714e-008
Gmin = 2.03704e-009
Gmin = 2.18725e-010
Gmin = 2.34854e-011
Gmin = 2.52173e-012
Gmin = 2.70769e-013
Gmin = 0
Gmin stepping succeeded in finding the operating point.

.tnom = 27
Date: Fri Dec 10 20:13:01 2021
Total elapsed time: 50.195 seconds.

.meas tran delay_z7 WITH CLA
+trig v(A0) val= 0.4 cross=2
+trig v(z7) val= 0.4 cross=4
.meas tran delay_z15 WITH CLA
+trig v(A0) val= 0.4 cross=2
+trig v(z15) val= 0.4 cross=2
.tran 10n
.END

```

➤ Tables-

- **Maximum Clock Frequency for which CSM will work satisfactorily for all possible input combinations is given below.**

Schematic	Frequency (GHz)	
	Without Extracted RC Netlist	With Extracted RC Netlist
Critical (WITH)	3.0303	1.8518
Critical(W/O)	1.785	1.0869

- **Rubric for Project Evaluation-**

Metric				
is to verify F(A=-2,B= 1), -(A=-5,B= 5)				
DRC and LVS	-	-	Pass	✓
CSM LVS	-	-	Pass	✓
CSM DRC	-	-	Pass	✓
Inverting A	-	-	Used	✓
Settling time vs SS (W/O RC) 5 pS (RC Ex)	1.9885	1.9885	1X-2X	
Pipelining		Used Correct		✓
ency with a GHz (W/O GHz (With I	1.6969	1.6969	1.5X-2X	
Area	92.5 λ x 851	96157.5 λ^2		