EE6320: RF Integrated Circuit Design
Project: VCO

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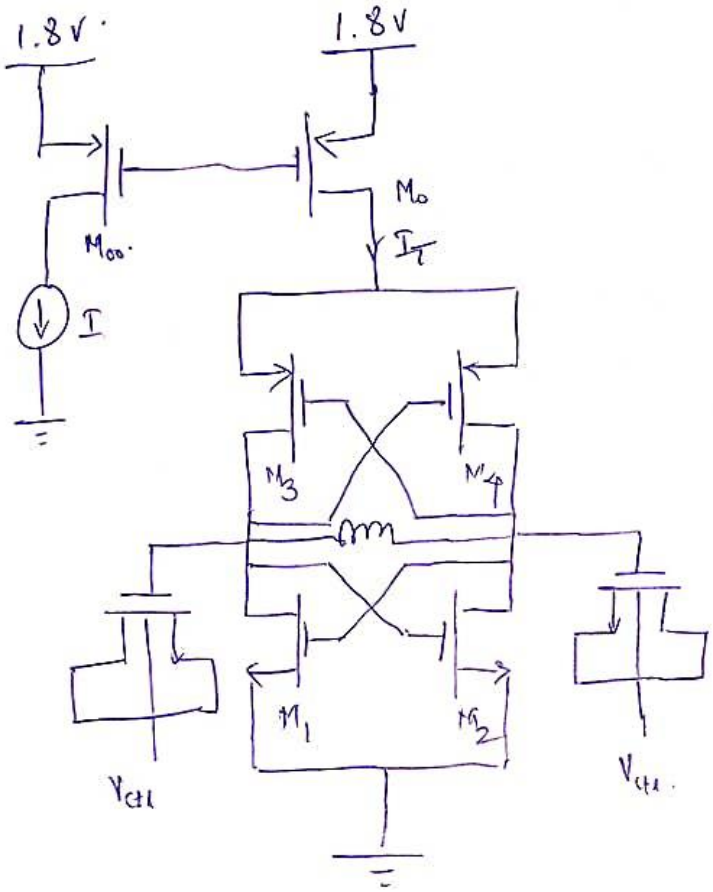


$$V_{oswing} = \frac{2}{\pi} I_T R$$

let, $I = 5mA$

$$\boxed{R = 314.16\ \Omega}$$

$$Q = \frac{R}{L\omega}$$

$$\boxed{L = 1.754\ nH}$$

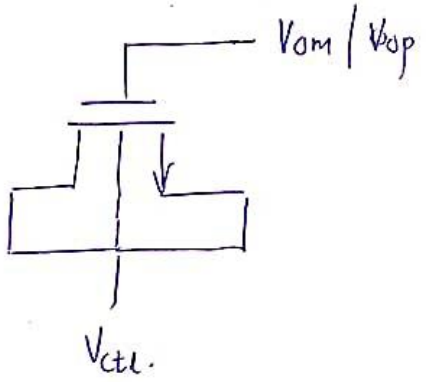
$$\omega_0 = \frac{1}{\sqrt{LC}}$$

$f_0 = 1.8\,GHz \sim 2.0\,GHz$.

realized using MOScap

$C = 4.0\,pF$ $\quad = C = C' + C_{dd} \Rightarrow C' = 3.7\,pF$

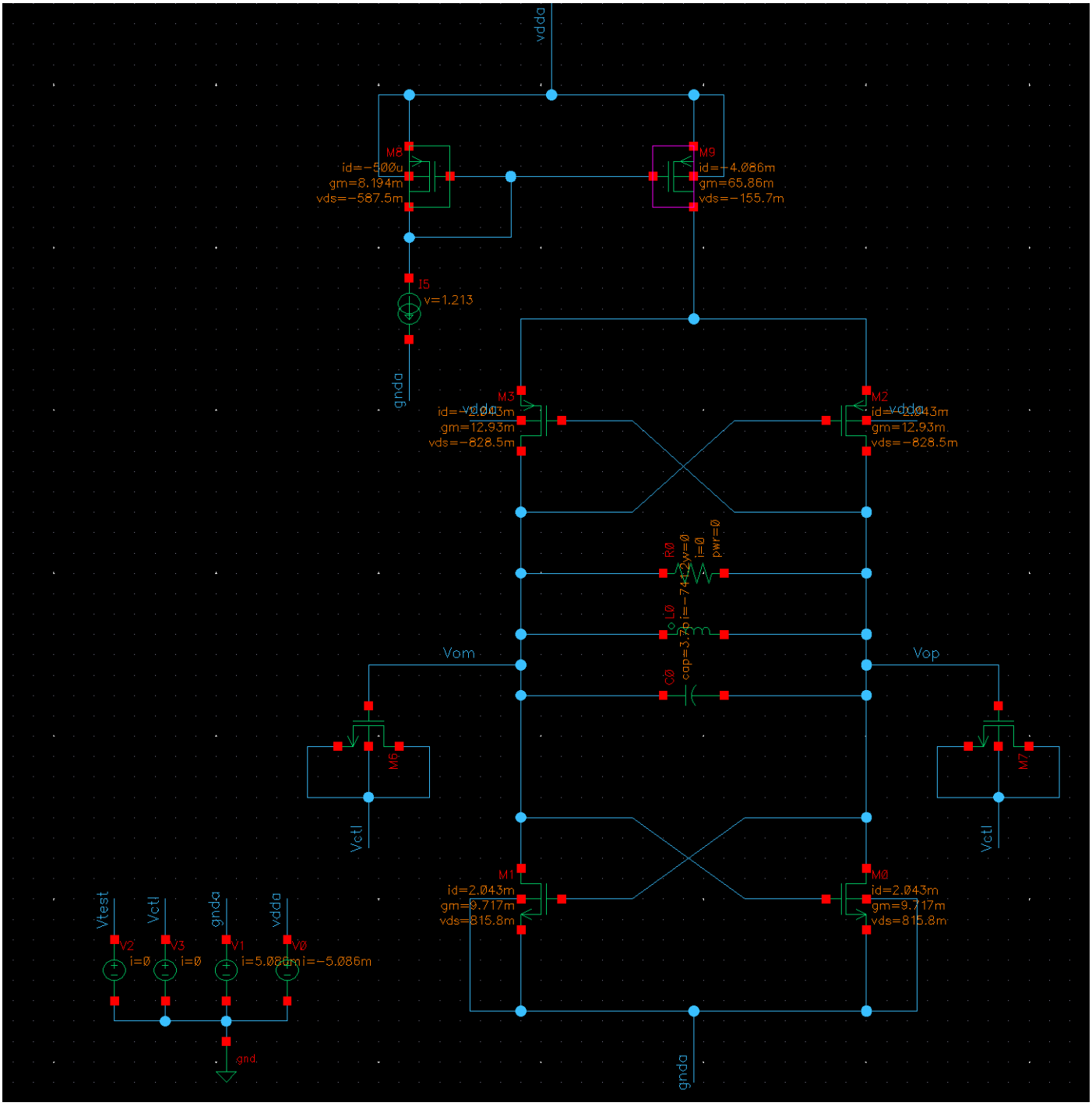
Sizes of M_{on} & M_{op} are chosen such that, M_3, M_4 are in saturation & g_{mn}, g_{mp} are such that, & $g_{mp} + g_{mn} > \frac{2}{R}$.



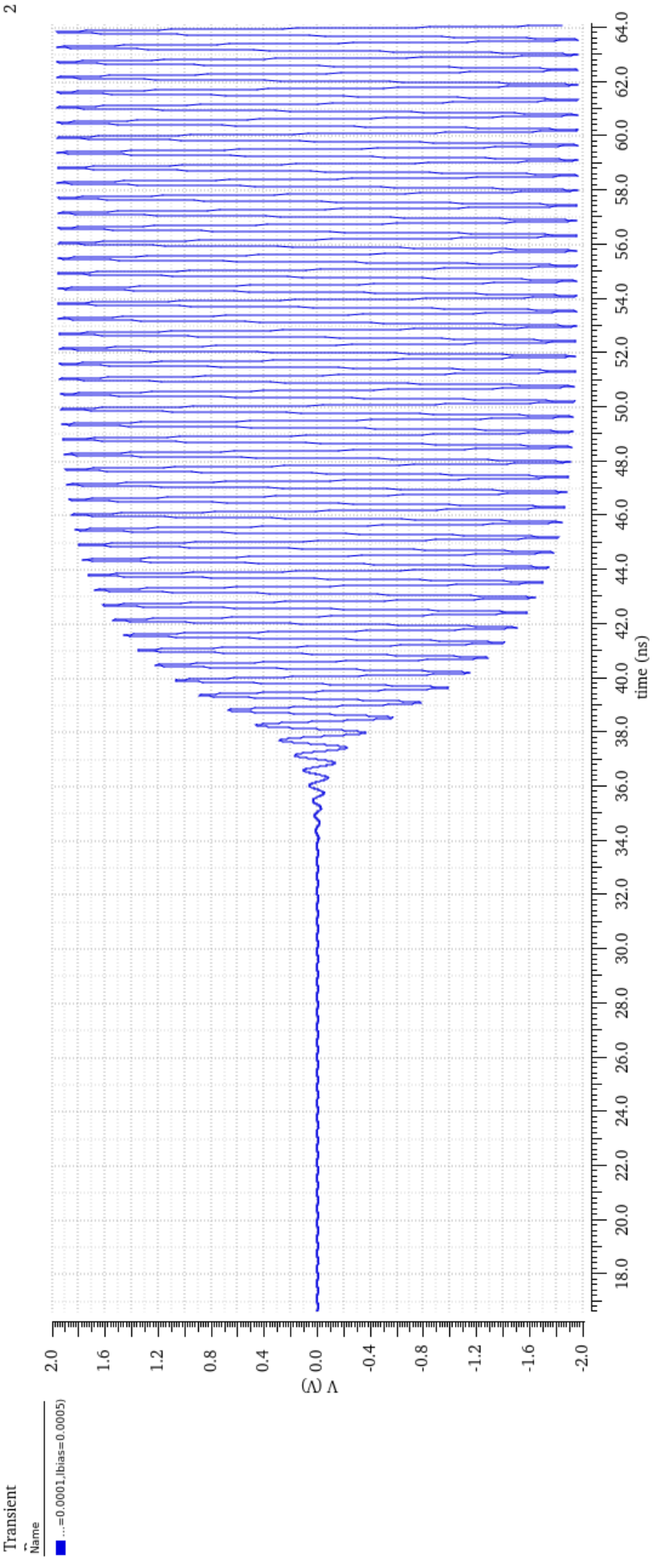
I varied V_{ctl} to get the freq vs V_{ctl} plot with which the width of MOS char is fixed by trial & error method.

With the desired width, I got freq. Vs V_{ctl} plot, then got the range of V_{ctl} for freq. variation from 1.8 GHz to 2 GHz.

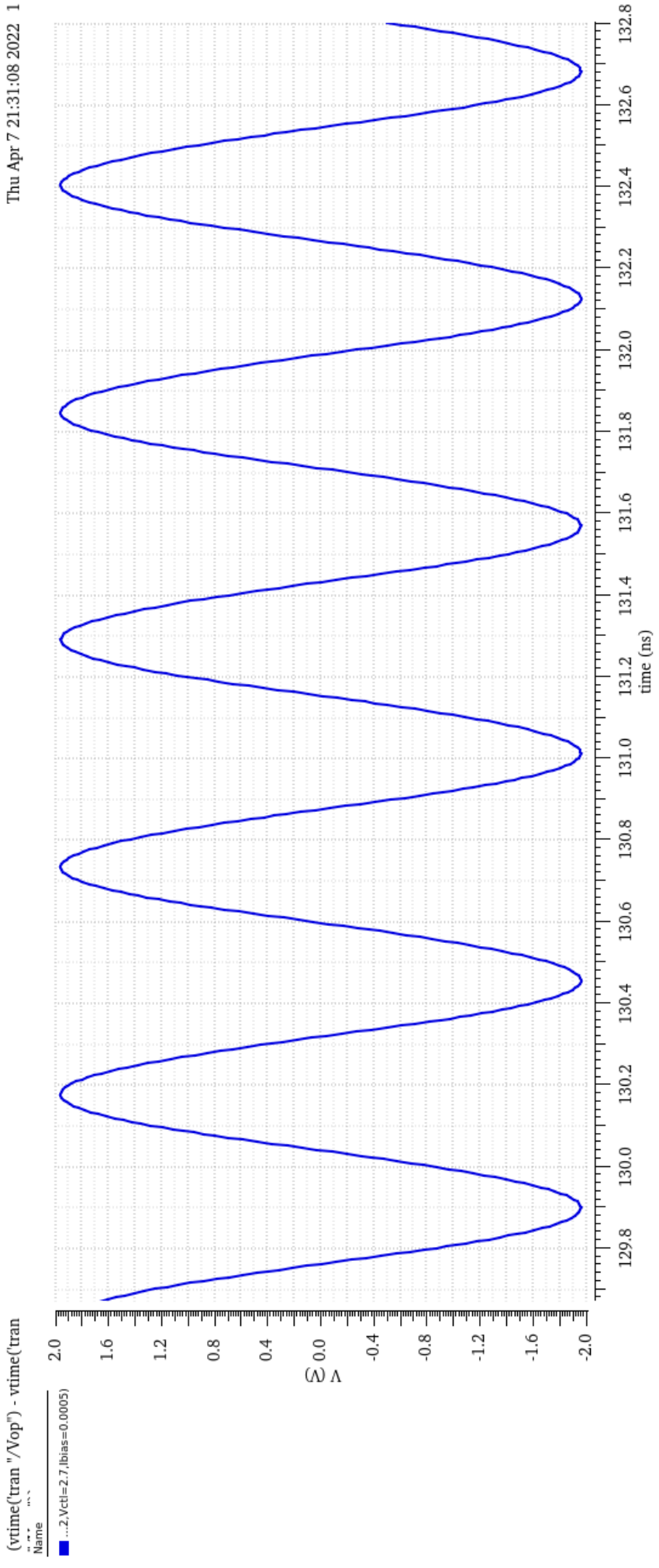
Schematic:


vdda
M8
id=-500u
gm=8.194m
vds=-587.5m
M9
id=-4.086m
gm=65.86m
vds=-155.7m
I5
v=1.213
gnda
M3
id=-2.043m
gm=12.93m
vds=-828.5m
M2
id=-2.043m
gm=12.93m
vds=-828.5m
R0
w=0
i=0
pwr=0
L0
cap=3.7p
C0
Vom
Vop
M6
M7
Vctl
Vctl
M1
id=2.043m
gm=9.717m
vds=815.8m
M0
id=2.043m
gm=9.717m
vds=815.8m
Vtest
Vctl
gnda
vdda
V2
i=0
V3
i=0
V1
i=5.086m
V0
i=-5.086m
gnd
gnda

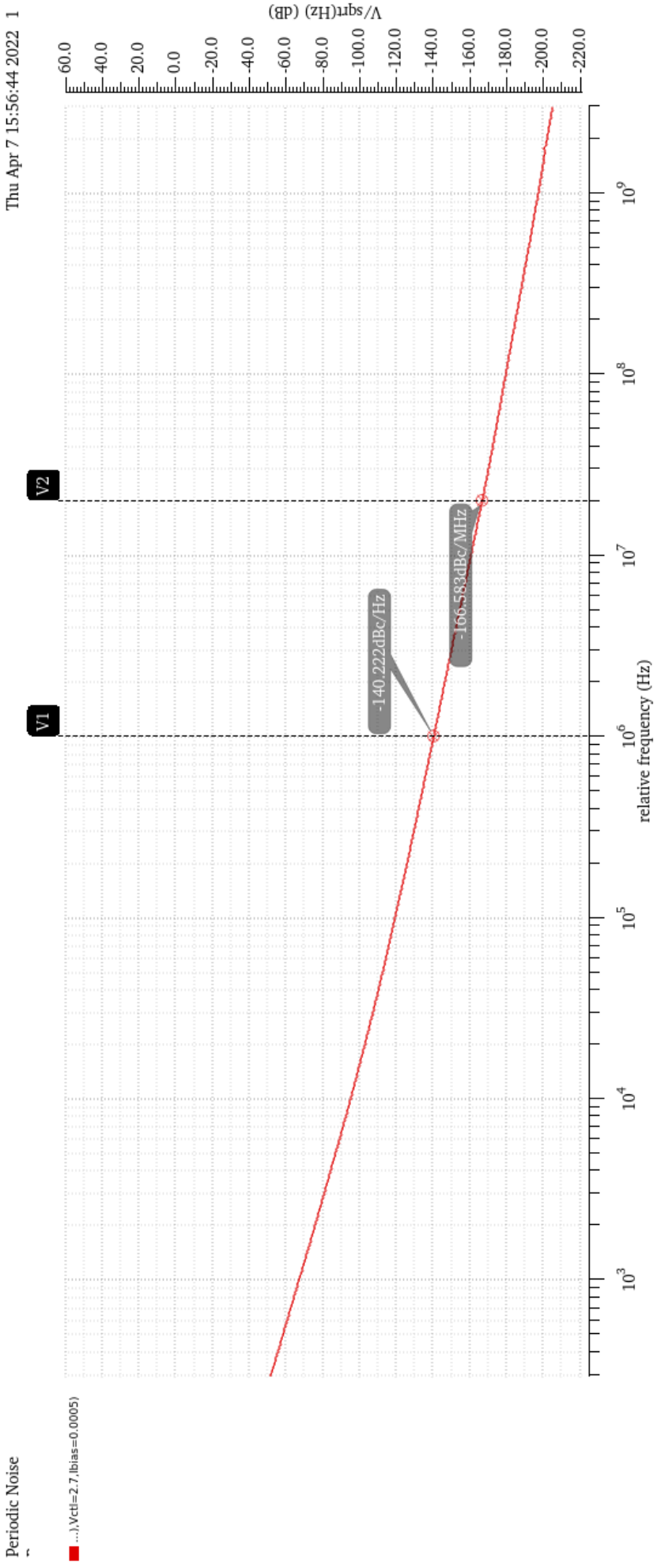
Plots:
$F = 1.8\,GHz$:
Transient:



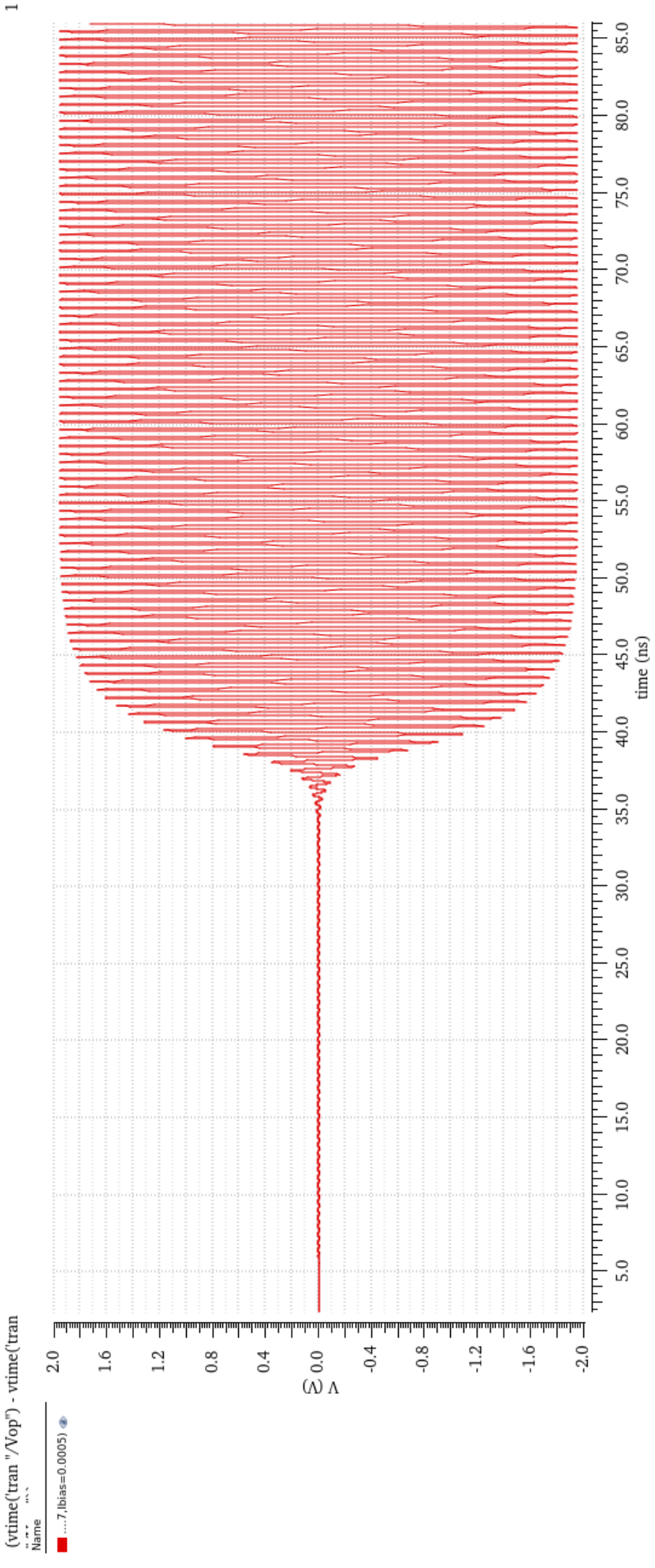
Steady State:



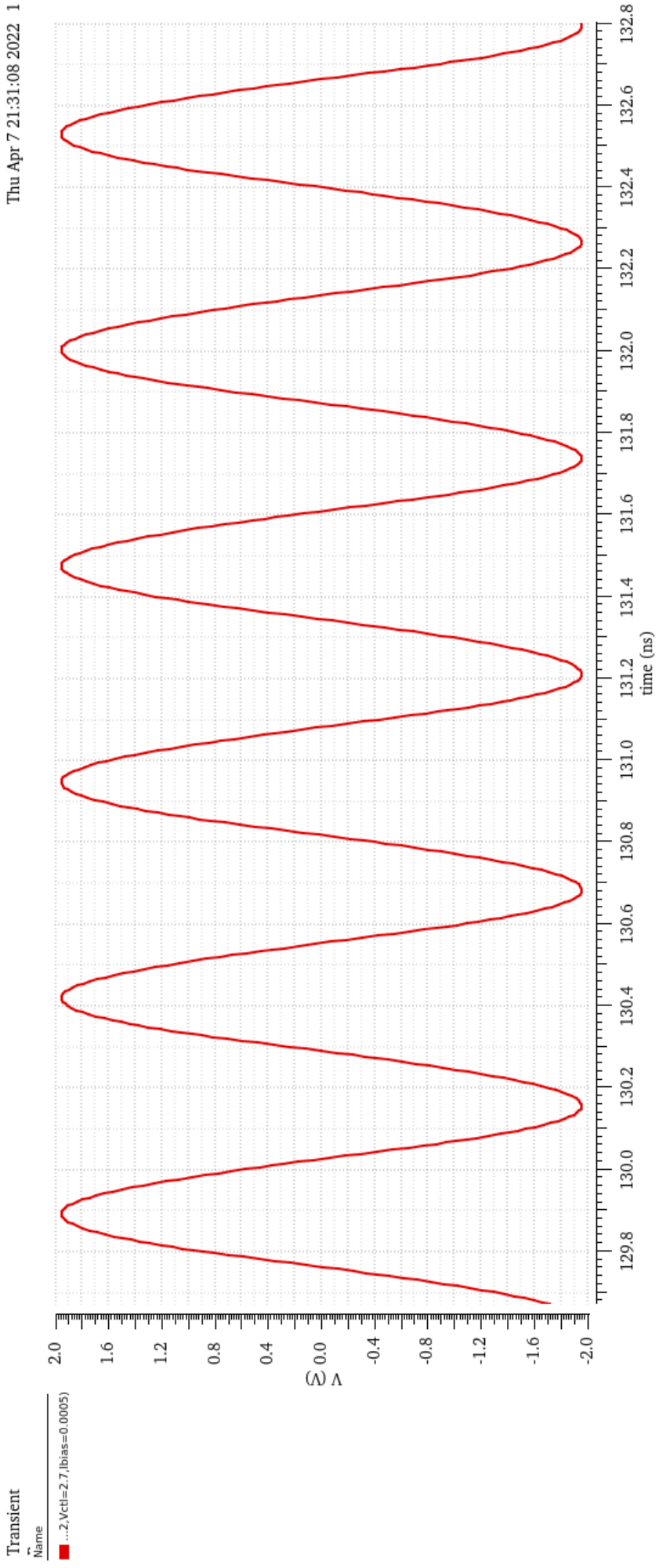
Phase Noise:


Thu Apr 7 15:56:44 2022 1
V/sqrt(Hz) (dB)
60.0
40.0
20.0
0.0
-20.0
-40.0
-60.0
-80.0
-100.0
-120.0
-140.0
-160.0
-180.0
-200.0
-220.0
V2
V1
-140.222dBc/Hz
-166.583dBc/MHz
10^3
10^4
10^5
10^6
10^7
10^8
10^9
relative frequency (Hz)
Periodic Noise
...),Vctl=2.7,Ibias=0.0005)

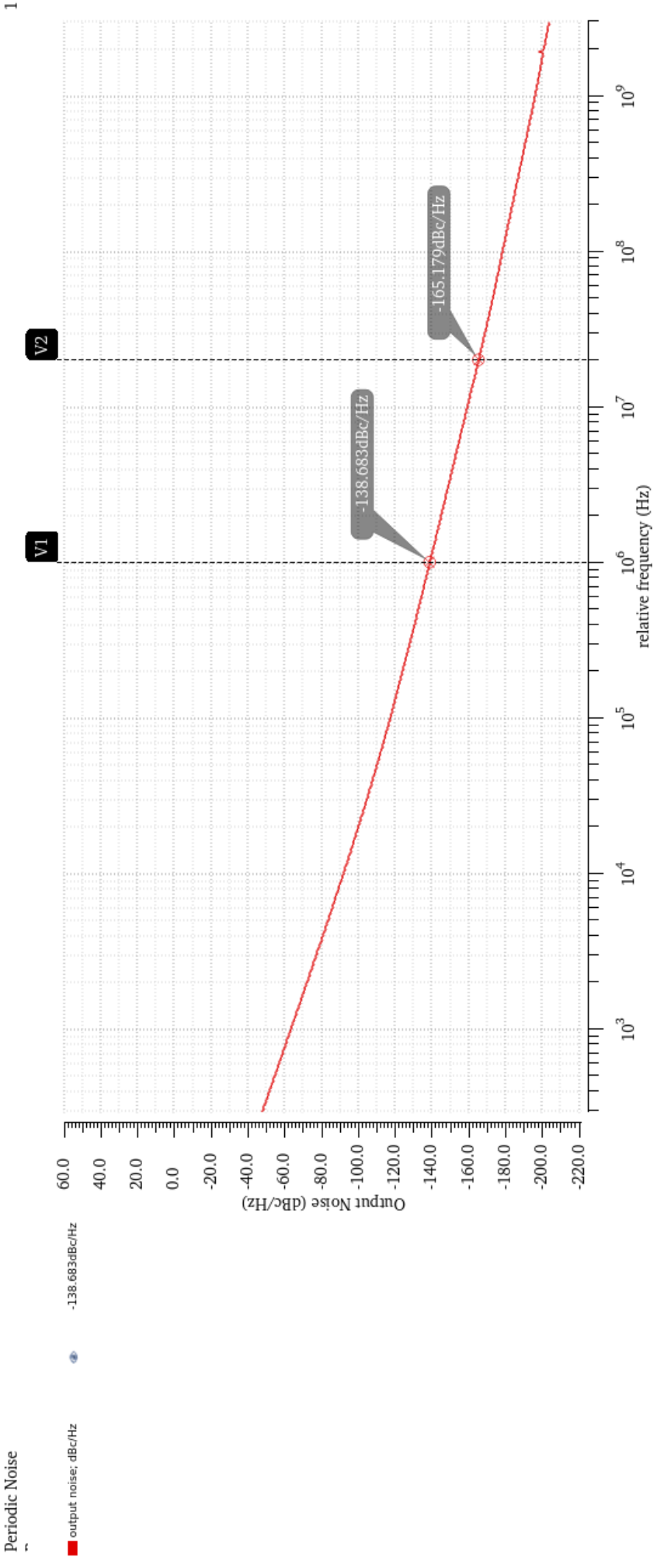
$F = 1.9GHz$:
Transient:



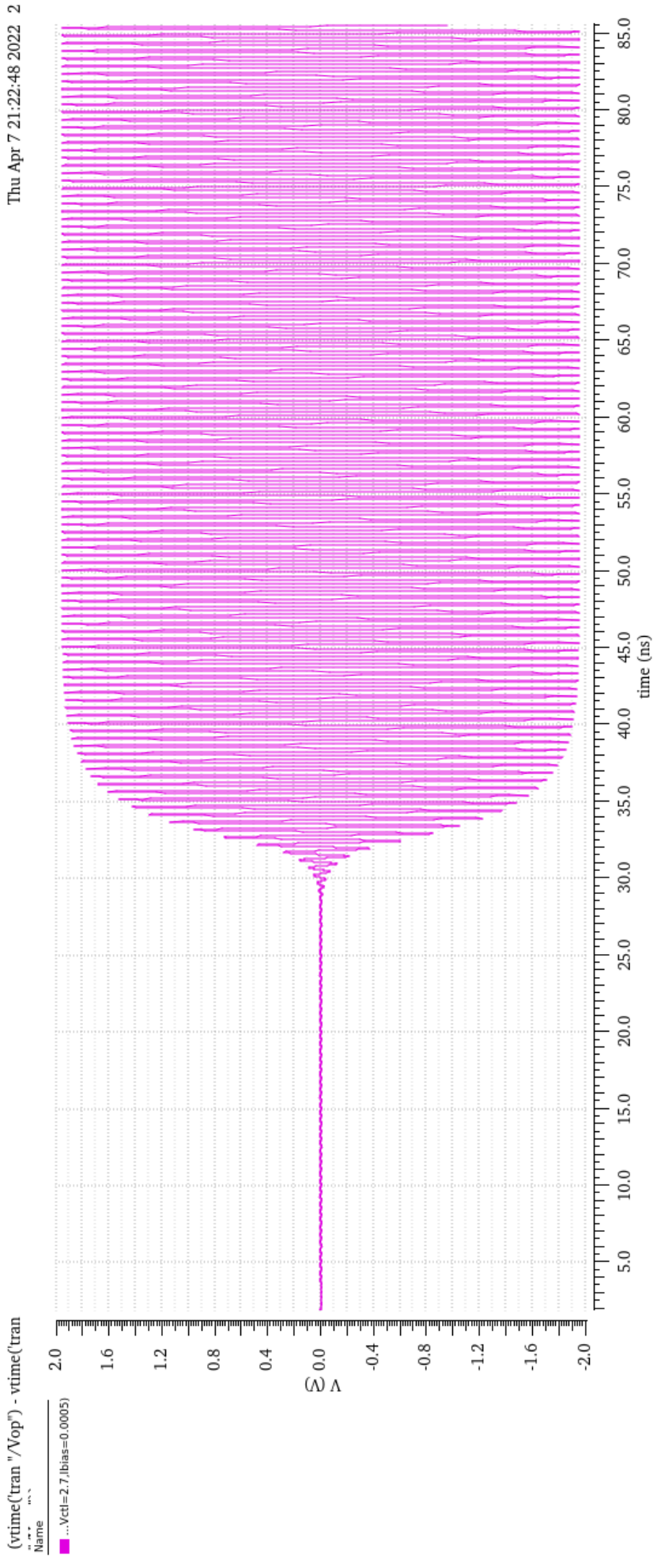
Steady State:



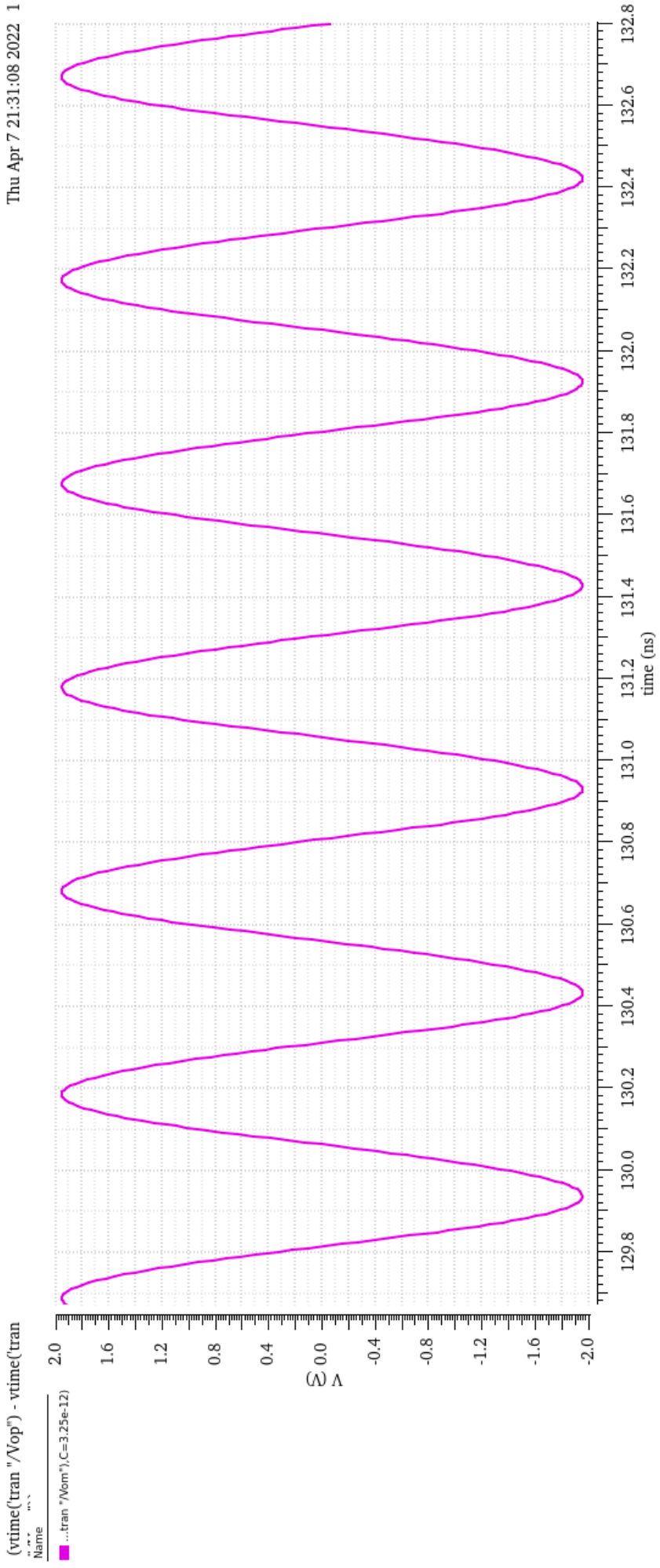
Phase Noise:


Periodic Noise
output noise: dBc/Hz
-138.683dBc/Hz
Output Noise (dBc/Hz)
60.0
40.0
20.0
0.0
-20.0
-40.0
-60.0
-80.0
-100.0
-120.0
-140.0
-160.0
-180.0
-200.0
-220.0
V1
V2
-138.683dBc/Hz
-165.179dBc/Hz
10^3
10^4
10^5
10^6
10^7
10^8
10^9
relative frequency (Hz)

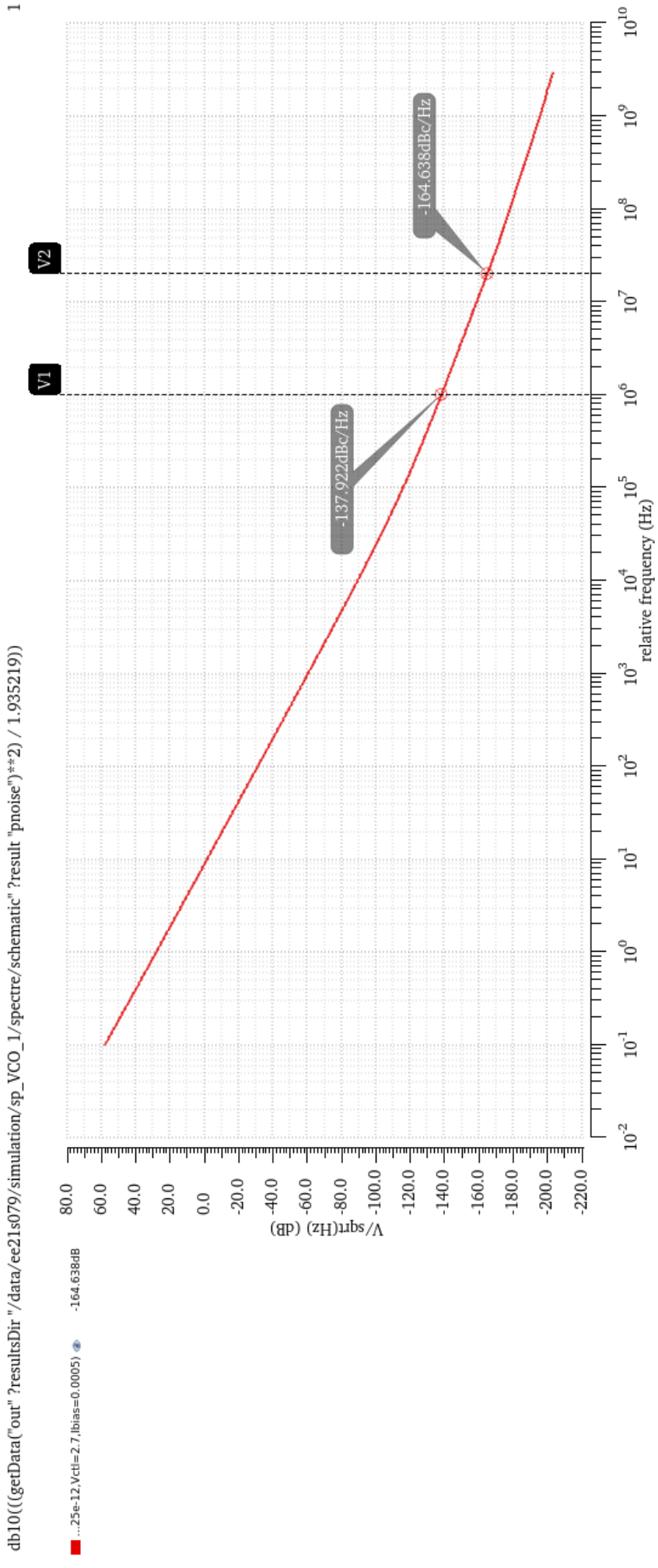
$F = 2GHz$:
Transient:



Steady State:



Phase Noise:


db10(((getData("our" ?resultsDir "/data/ee21s079/simulation/sp_VCO_1/spectre/schematic" ?result "pnoise")**2) / 1.935219))
1
...25e-12,Vctl=2.7,Ibias=0.0005)
-164.638dB
V/sqrt(Hz) (dB)
relative frequency (Hz)
V1
V2
-137.922dBc/Hz
-164.638dBc/Hz

	Design Metric	Performance	Specification
Output Amplitude	f_o = 1.8GHz	1.961V	≥1V
	f_o = 1.9GHz	1.959 V	≥1V
	f_o = 2.0GHz	1.956 V	≥1V
Phase Noise [1MHz offset]	f_o = 1.8GHz	-140.22 dBc/Hz	≤−117dBc/Hz
	f_o = 1.9GHz	-138.63 dBc/Hz	≤−117dBc/Hz
	f_o = 2.0GHz	-137.92 dBc/Hz	≤−117dBc/Hz
Phase Noise [20MHz offset]	f_o = 1.8GHz	-166.58 dBc/Hz	≤−140dBc/Hz
	f_o = 1.9GHz	-165.17 dBc/Hz	≤−140dBc/Hz
	f_o = 2.0GHz	-164.638 dBc/Hz	≤−140dBc/Hz
Tuning Range	Total Tuning Range [Specify Range]	215 MHz	≥200MHz
	Number of bits in coarse-tuning	-	
	Voltage range in fine-tuning	1.55 V	
	Average K_{VCO}	108.70 MHz/V	≈ 150MHz/V
	% Variation in K_{VCO}		Minimal
Power [1.8GHz]	VCO average power consumption [Excluding Bias]	8.524 mW	
	Bias circuit power consumption	0.929 mW	
Other	Sum of all capacitances [in capacitor bank]	3.25 pF	
	Inductance used	1.754 nH	
	Simulator Used	Virtuoso	

Table 1: VCO Performance Summary Table