EE6326 ICDT

Project: LDO

Sarvjit Ajit Patil

EE21S079

Path to Design:

OpAmp: */home/ee21s079/cadence/ee6326/sp_ee6326/SP_EE6326/sp_OpAmp_LDO_3*

Testbench: */home/ee21s079/cadence/ee6326/sp_ee6326/SP_EE6326/sp_OpAmp_Test*

LDO: */home/ee21s079/cadence/ee6326/sp_ee6326/SP_EE6326/sp_LDO_3*

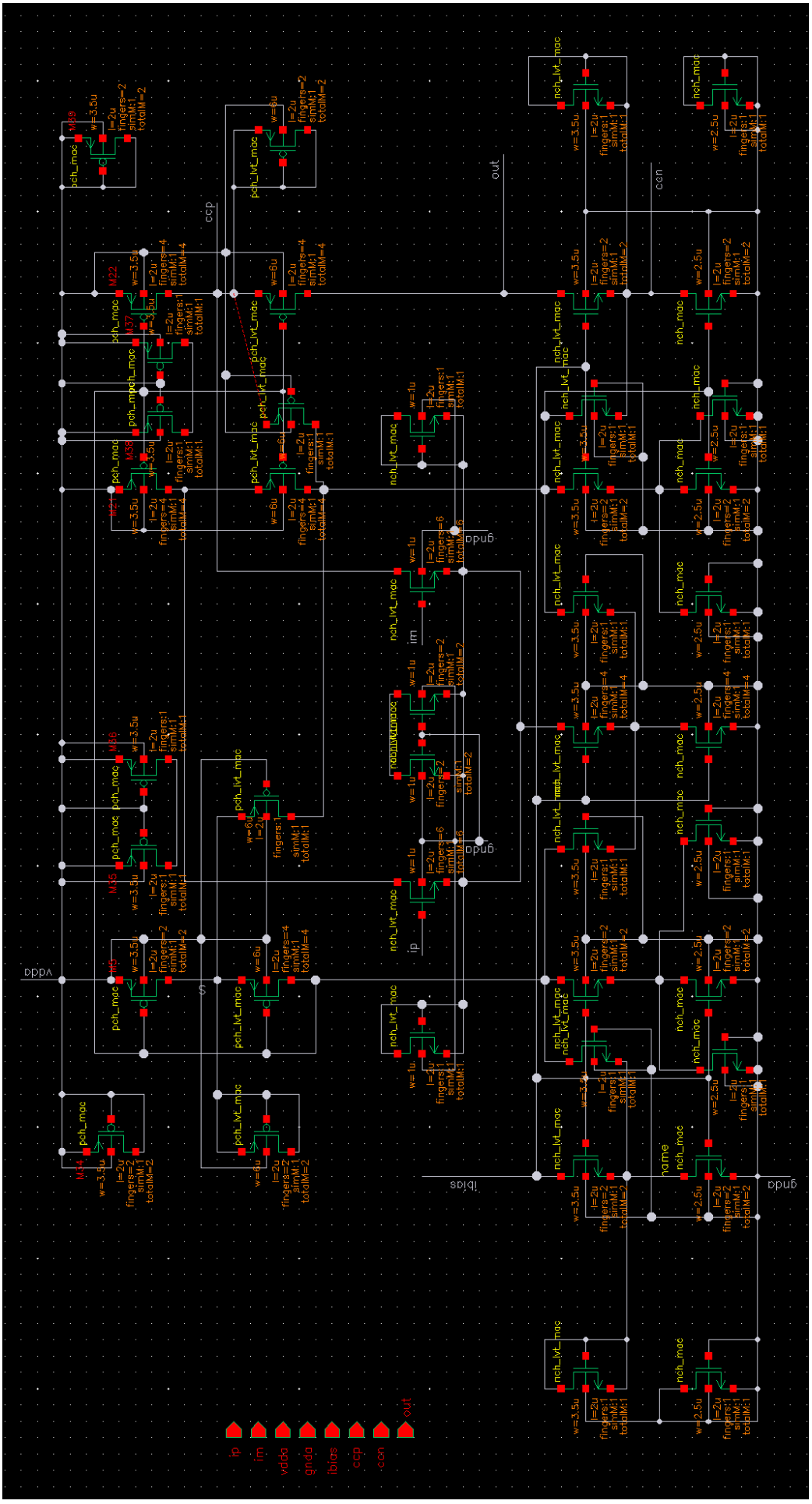
Testbench: */home/ee21s079/cadence/ee6326/sp_ee6326/SP_EE6326/sp_LDO_3_TEST*

Plots and Schematic Snapshots: */home/ee21s079/cadence/ee6326/sp_ee6326/SP_EE6326/sp_LDO_3/Plots*

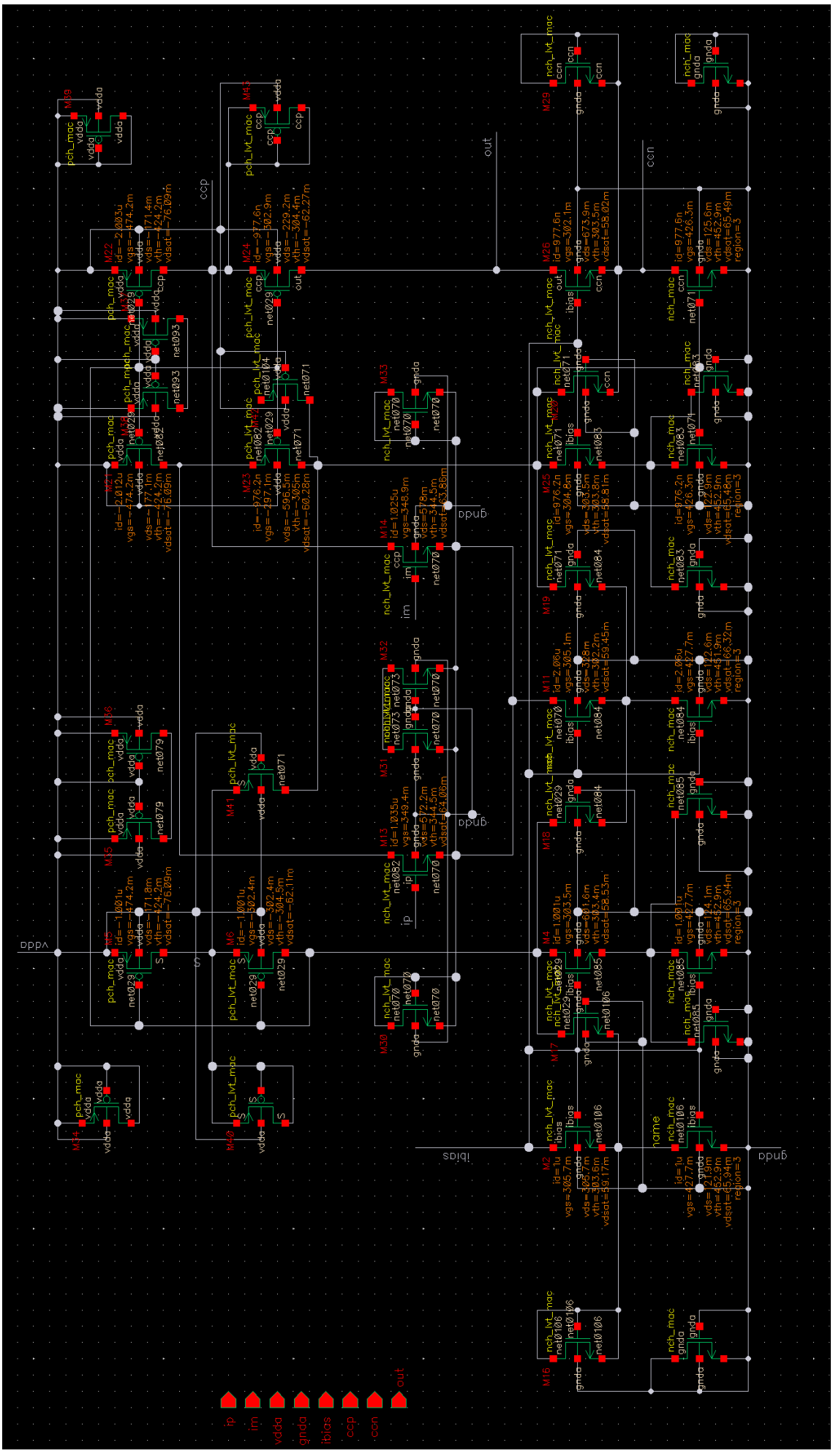
Devices used*: nch_mac, nch_lvt_mac, pch_mac, pch_lvt_mac, crtmom*

OpAmp (stb analysis):

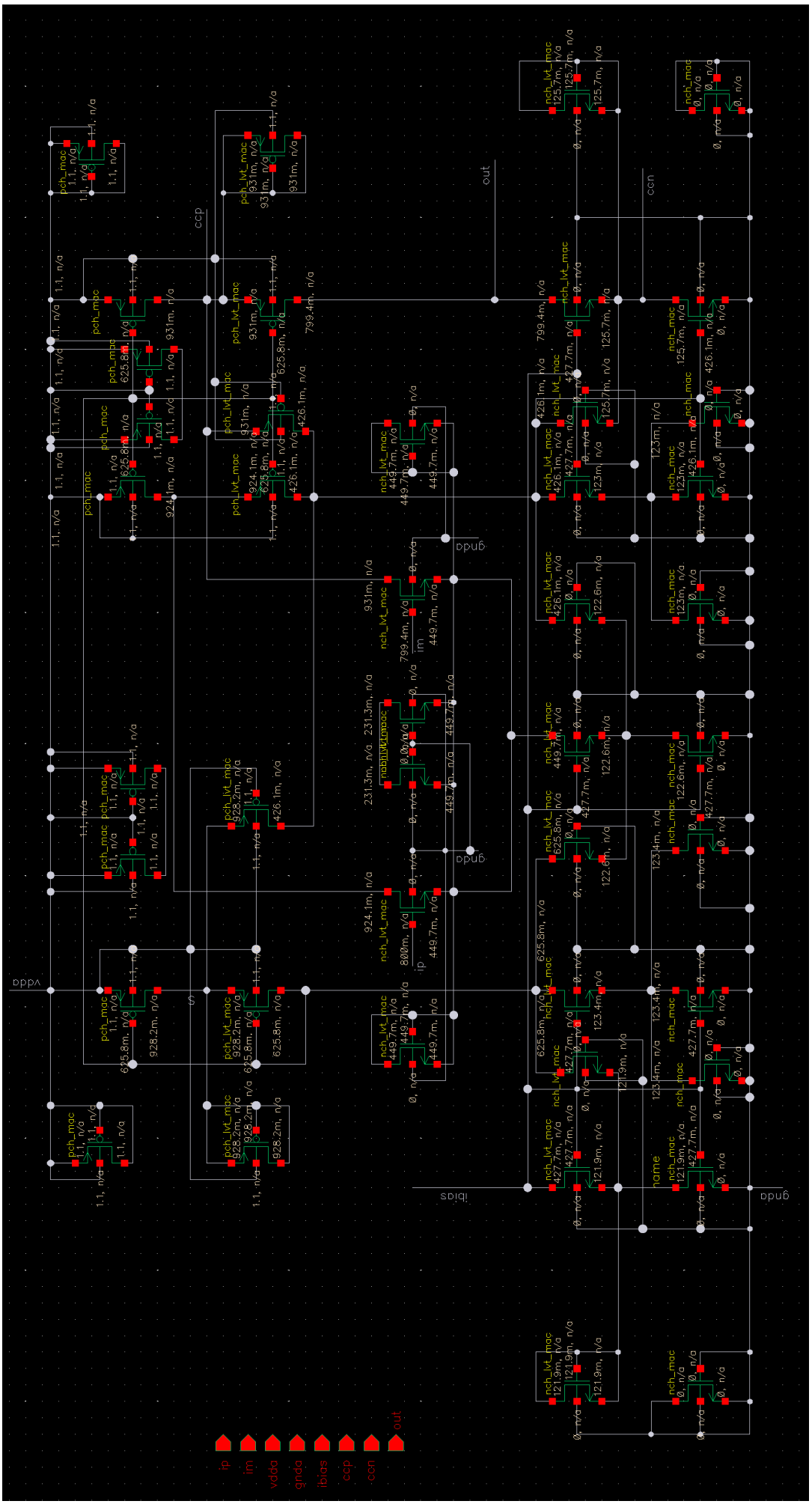
Transistor sizes:



Annotated DC Operating Points $(1.1v, tt, 50°C)$**:**



Annotated Node Voltages and Currents $(1.1v, tt, 50°C)$**:**

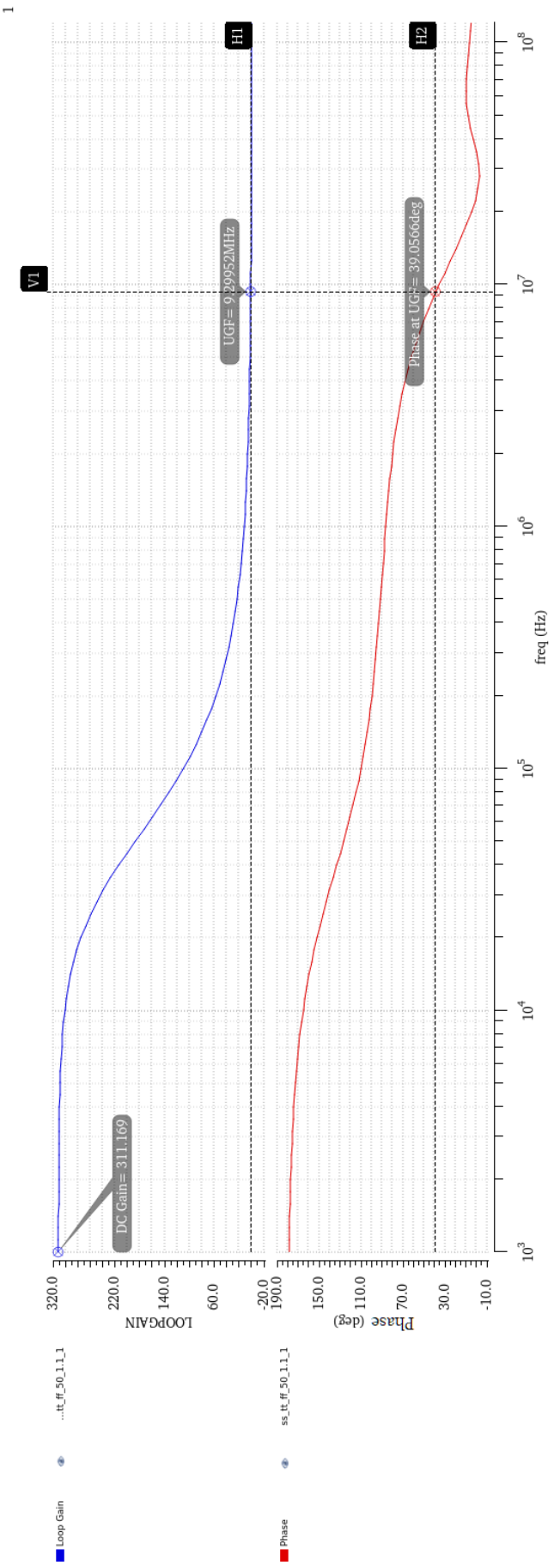


Plots:

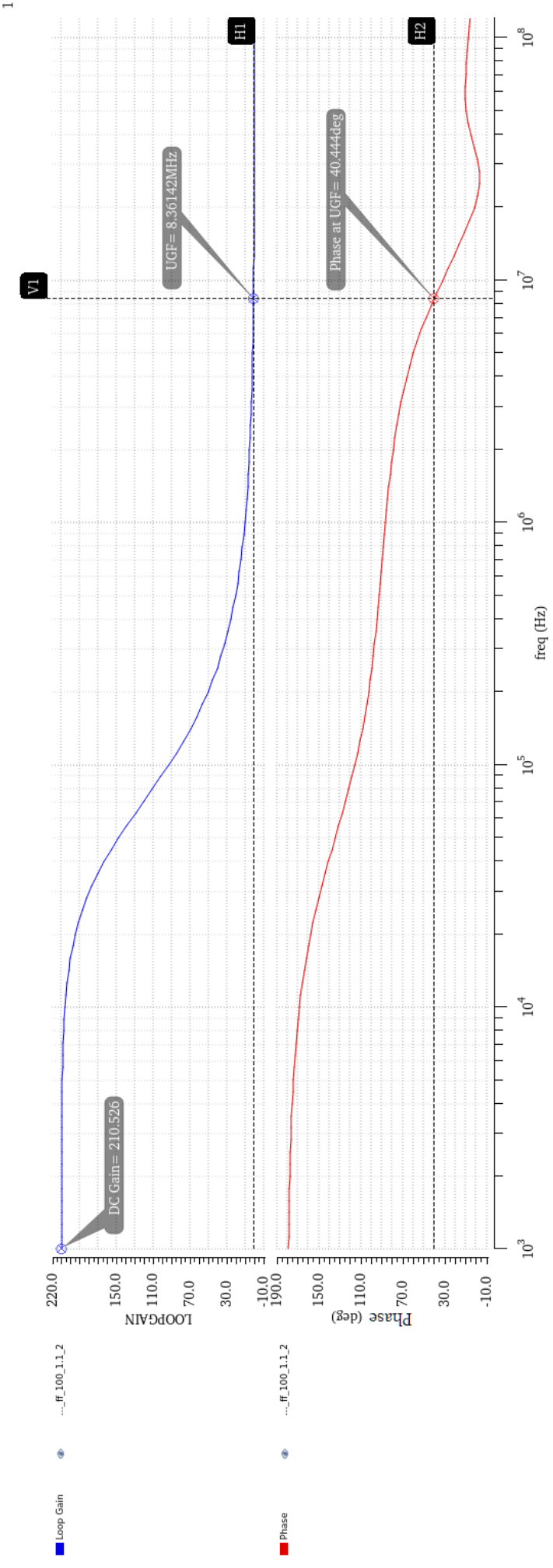
Magnitude, Phase Plot:

Schematic (W/O RC Extraction):

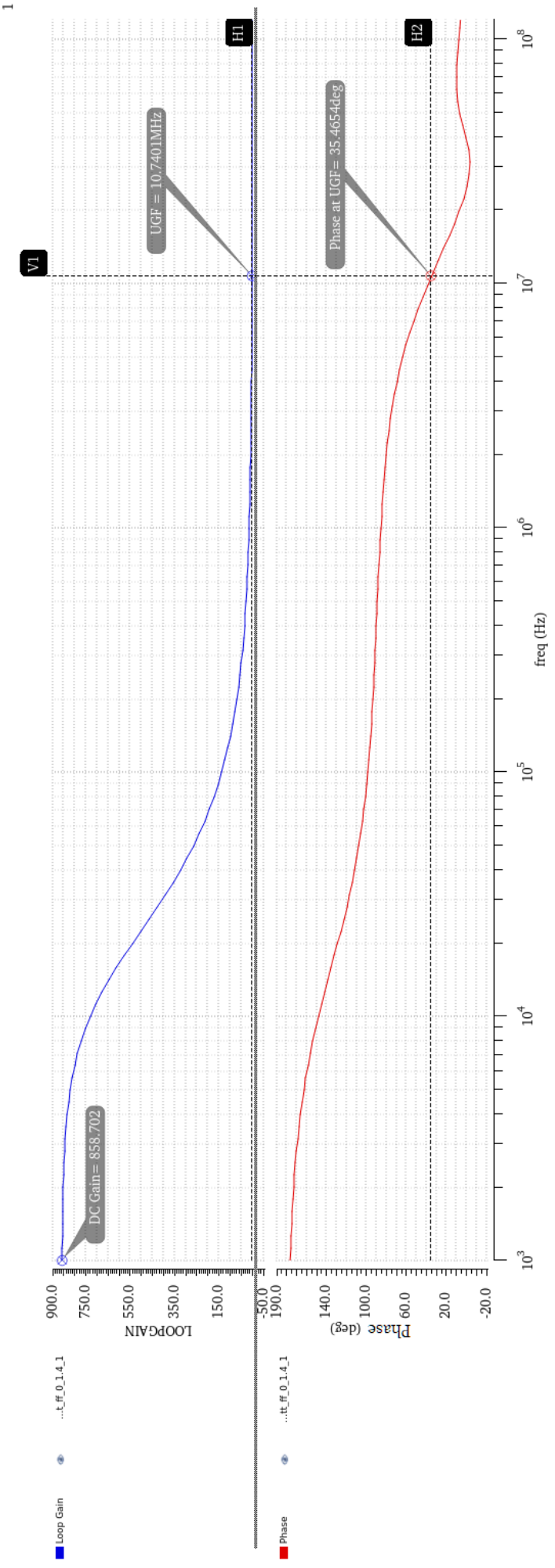
1. $\{1.1V, tt, 50℃\}$:



2. Minimum DC Gain $\{V_{dd}, ff, 0℃\}$:

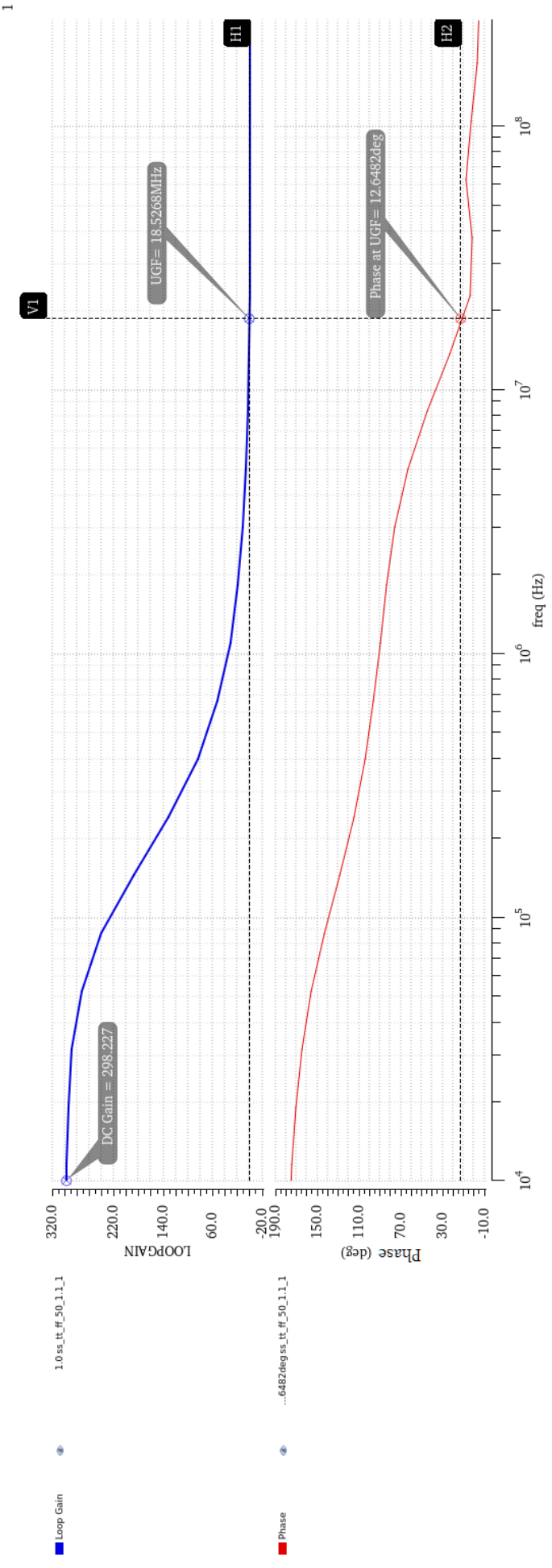


3. Maximum DC Gain $\{1.4V, tt, 0℃\}$:

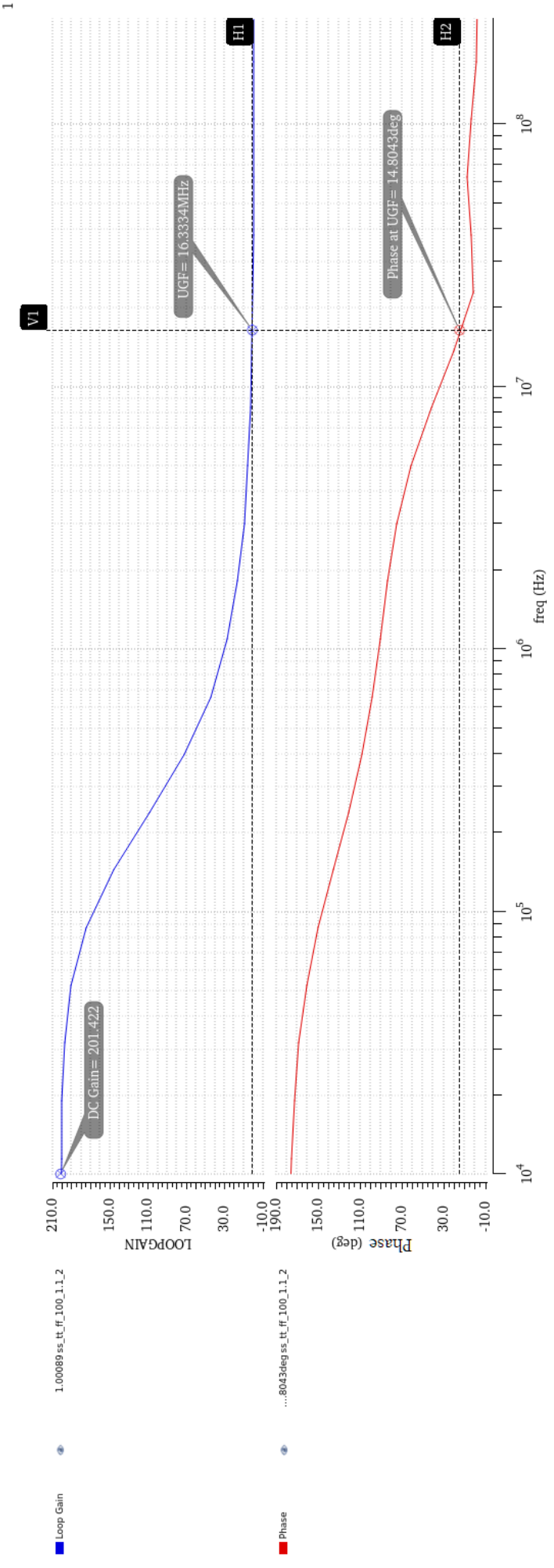


RC Extracted Schematic:

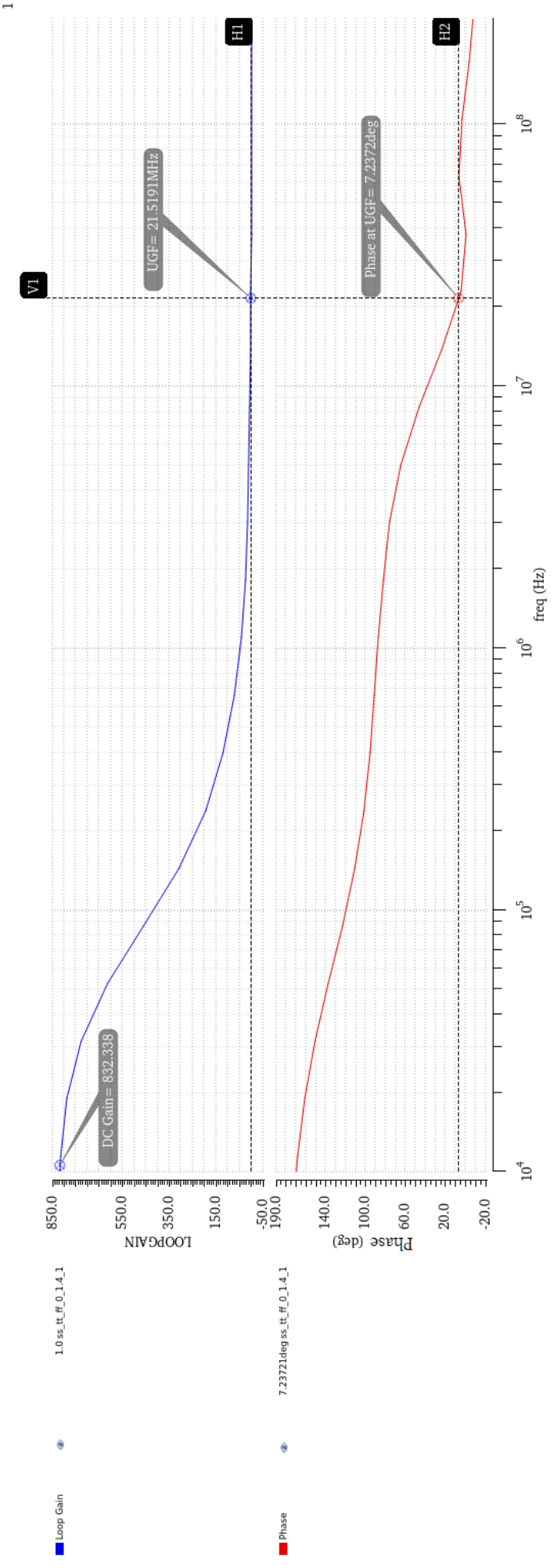
1. $\{1.1V, tt, 50℃\}$:



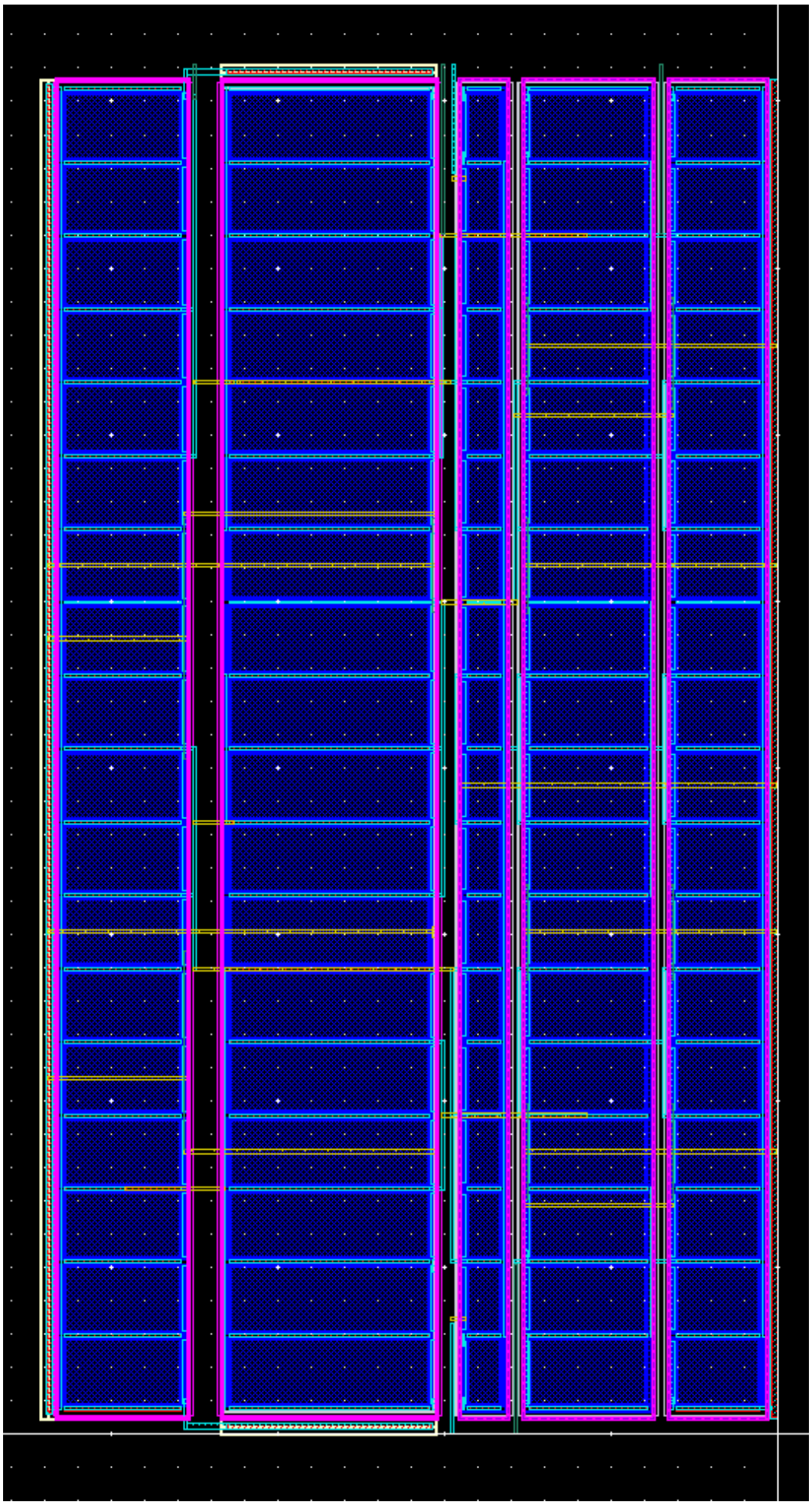
2. Minimum DC Gain $\{V_{dd}, ff, 0℃\}$:



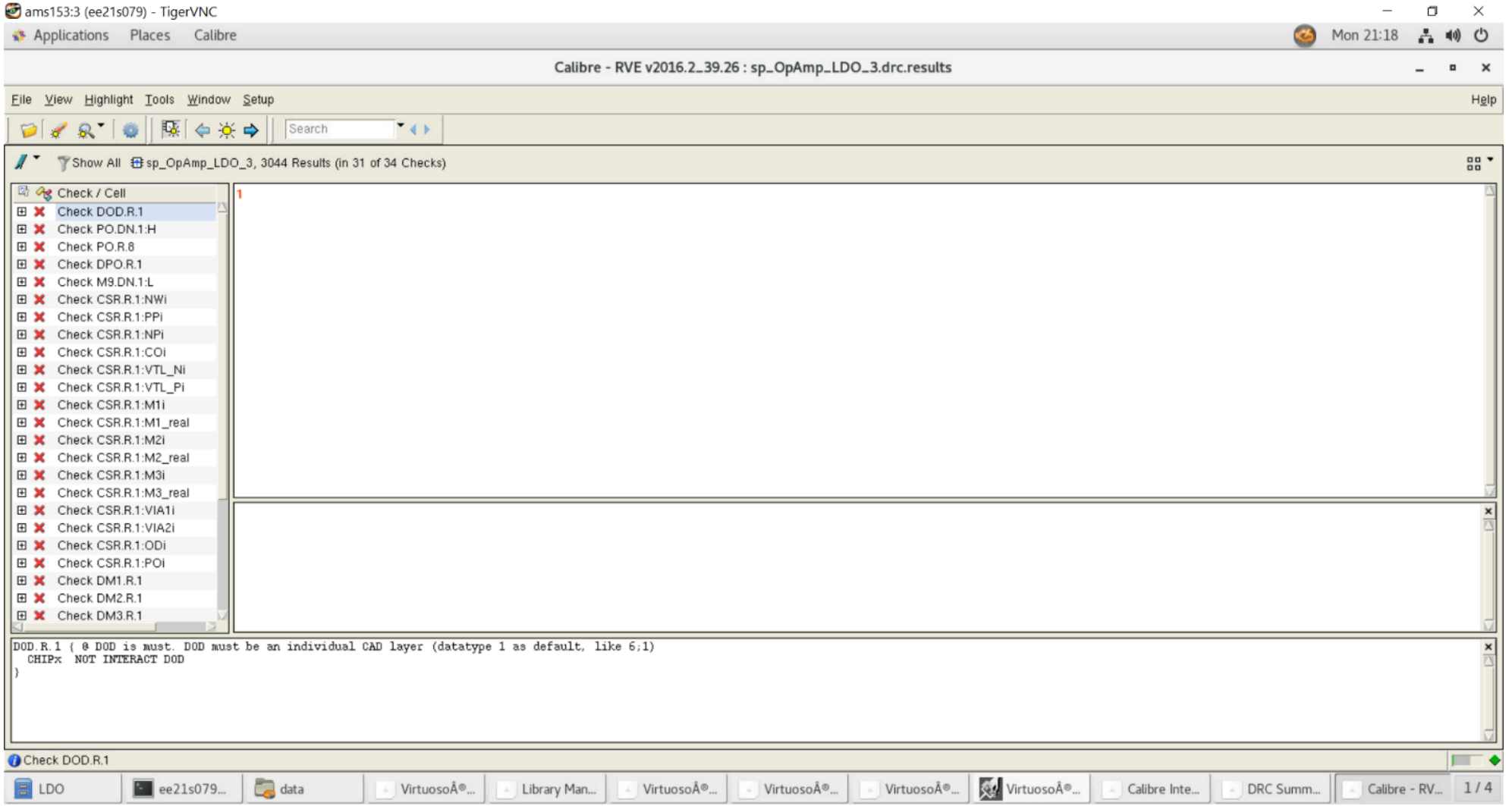
3. Maximum DC Gain $\{1.4V, tt, 0℃\}$:



Layout of OpAmp:



DRC :


ams153:3 (ee21s079) - TigerVNC
Applications
Places
Calibre
Mon 21:18
Calibre - RVE v2016.2_39.26 : sp_OpAmp_LDO_3.drc.results
File
View
Highlight
Tools
Window
Setup
Help
Search
Show All
sp_OpAmp_LDO_3, 3044 Results (in 31 of 34 Checks)
Check / Cell
Check DOD.R.1
Check PO.DN.1:H
Check PO.R.8
Check DPO.R.1
Check M9.DN.1:L
Check CSR.R.1:NWi
Check CSR.R.1:PPi
Check CSR.R.1:NPi
Check CSR.R.1:COi
Check CSR.R.1:VTL_Ni
Check CSR.R.1:VTL_Pi
Check CSR.R.1:M1i
Check CSR.R.1:M1_real
Check CSR.R.1:M2i
Check CSR.R.1:M2_real
Check CSR.R.1:M3i
Check CSR.R.1:M3_real
Check CSR.R.1:VIA1i
Check CSR.R.1:VIA2i
Check CSR.R.1:ODi
Check CSR.R.1:POi
Check DM1.R.1
Check DM2.R.1
Check DM3.R.1
1
DOD.R.1 { @ DOD is must. DOD must be an individual CAD layer (datatype 1 as default, like 6;1)
CHIPx NOT INTERACT DOD
}
Check DOD.R.1
LDO
ee21s079...
data
VirtuosoÂ®...
Library Man...
Calibre Inte...
DRC Summ...
Calibre - RV...
1 / 4

LVS:

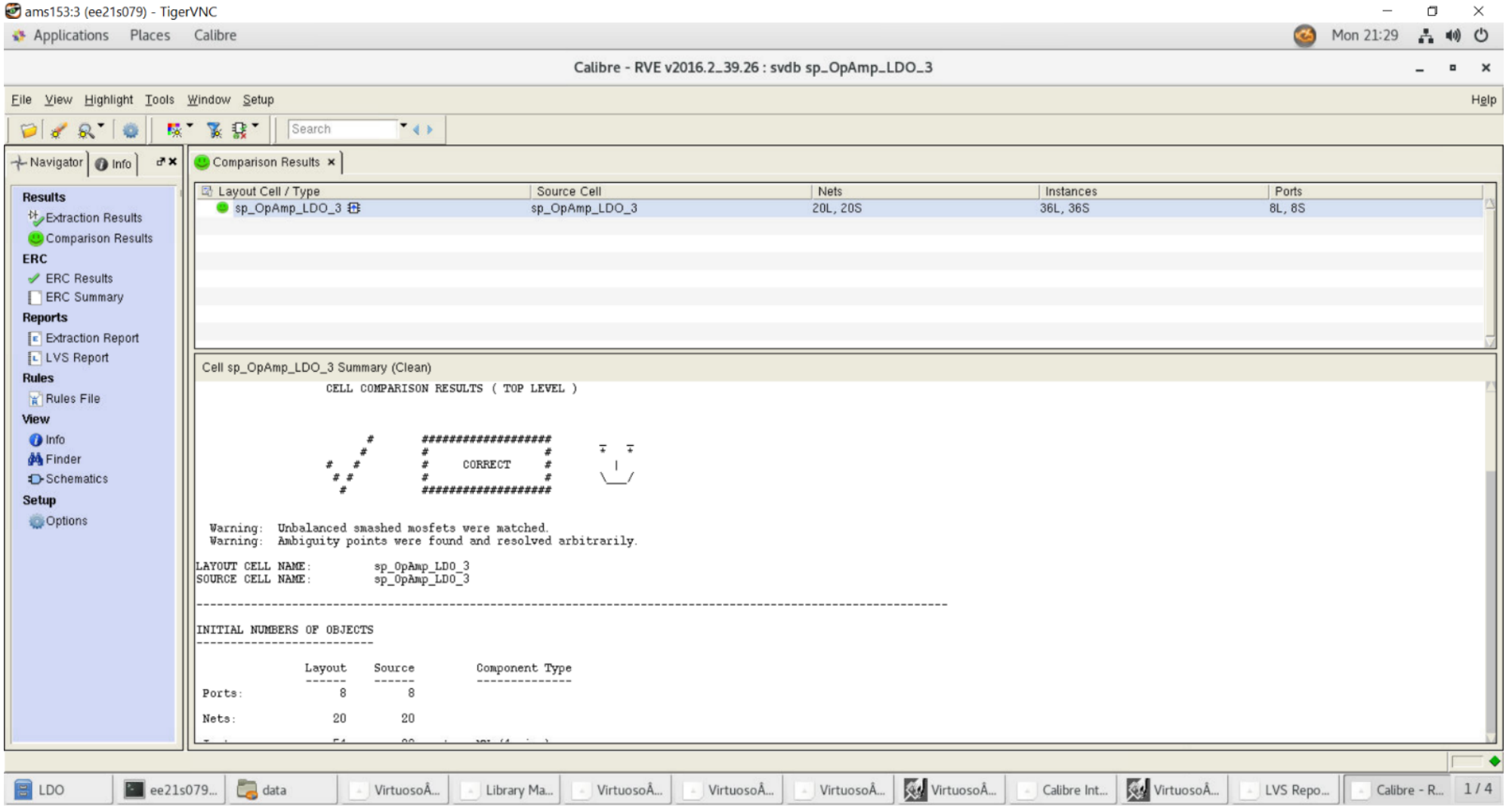

ams153:3 (ee21s079) - TigerVNC
Applications Places Calibre
Mon 21:29
Calibre - RVE v2016.2_39.26 : svdb sp_OpAmp_LDO_3
File View Highlight Tools Window Setup
Help
Search
Navigator
Info
Comparison Results
Results
Extraction Results
Comparison Results
ERC
ERC Results
ERC Summary
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Layout Cell / Type
Source Cell
Nets
Instances
Ports
sp_OpAmp_LDO_3
sp_OpAmp_LDO_3
20L, 20S
36L, 36S
8L, 8S
Cell sp_OpAmp_LDO_3 Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
Warning: Unbalanced smashed mosfets were matched.
Warning: Ambiguity points were found and resolved arbitrarily.
LAYOUT CELL NAME: sp_OpAmp_LDO_3
SOURCE CELL NAME: sp_OpAmp_LDO_3
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 8 8
Nets: 20 20
LDO
ee21s079...
data
VirtuosoÂ...
Library Ma...
Calibre Int...
LVS Repo...
Calibre - R...
1 / 4

Table:

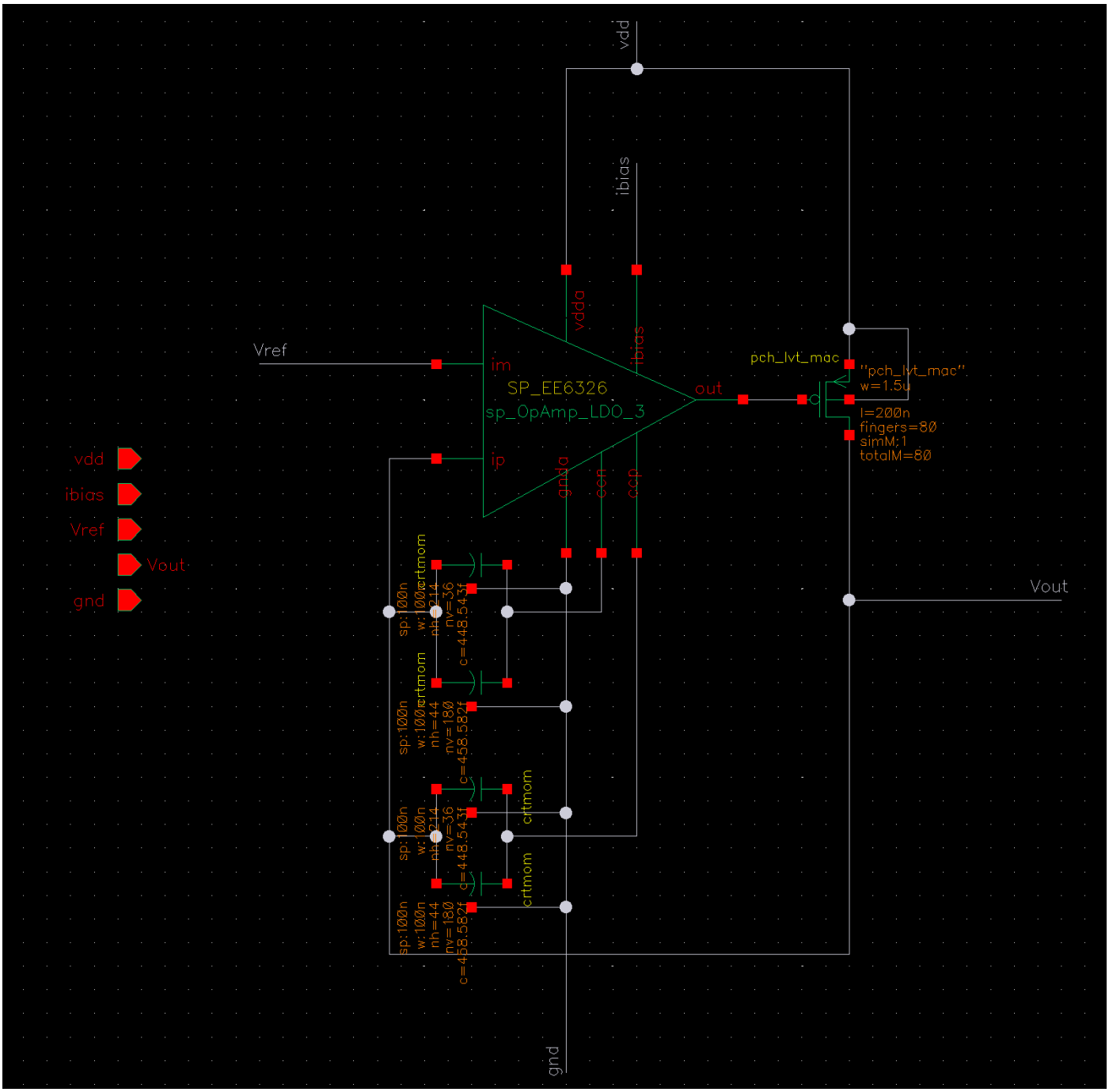
	Schematic				*RC Extracted Netlist*		
Corners	***Gain***	***UGF***	***Current Consumption***		***Gain***	***UGF***	***Current Consumption***
		(MHz)	*(uA)*			*(MHz)*	*(uA)*
{Vdd= 1.1v, ss, 0}	421.062	10.2359	6.003905		404.23	20.1685	6.057323
{Vdd= 1.1v, ss, 50}	309.618	9.25302	6.007798		296.408	18.5369	6.056954
{Vdd= 1.1v, ss, 100}	217.373	8.3642	6.013464		207.561	16.5742	6.058839
{Vdd= 1.1v, tt, 0}	422.702	10.2784	6.006993		405.849	20.1358	6.060721
{Vdd= 1.1v, tt, 50}	311.169	9.29952	6.011381		298.227	18.5268	6.060808
{Vdd= 1.1v, tt, 100}	218.323	8.41179	6.018777		208.531	16.5954	6.064449
{Vdd= 1.1v, ff, 0}	402.942	10.2255	6.010361		387.296	19.952	6.064093
{Vdd= 1.1v, ff, 50}	298.177	9.24594	6.015829		285.918	18.3059	6.065199
{Vdd= 1.1v, ff, 100}	210.526	8.36142	6.027017		201.422	16.3334	6.072716
{Vdd= 1.4v, ss, 0}	858.192	10.7048	6.021942		832.062	21.5706	6.075491
{Vdd= 1.4v, ss, 50}	740.216	9.74086	6.02708		718.473	20.4076	6.076319
{Vdd= 1.4v, ss, 100}	623.249	8.87629	6.034893		605.603	19.0836	6.08028
{Vdd= 1.4v, tt, 0}	858.702	10.7401	6.024769		832.338	21.5191	6.078651
{Vdd= 1.4v, tt, 50}	740.341	9.77778	6.030359		718.316	20.3639	6.079899
{Vdd= 1.4v, tt, 100}	621.663	8.91256	6.039888		603.769	19.0493	6.085626
{Vdd= 1.4v, ff, 0}	801.87	10.6856	6.028934		777.275	21.337	6.082857
{Vdd= 1.4v, ff, 50}	685.846	9.71837	6.035721		665.176	20.1431	6.085257
{Vdd= 1.4v, ff, 100}	569.36	8.85359	6.049276		552.59	18.789	6.095139

Gain	**MAX**	**MIN**
UGF	**MAX**	**MIN**
Current Consumption	**MAX**	**MIN**

LDO:

Schematic:

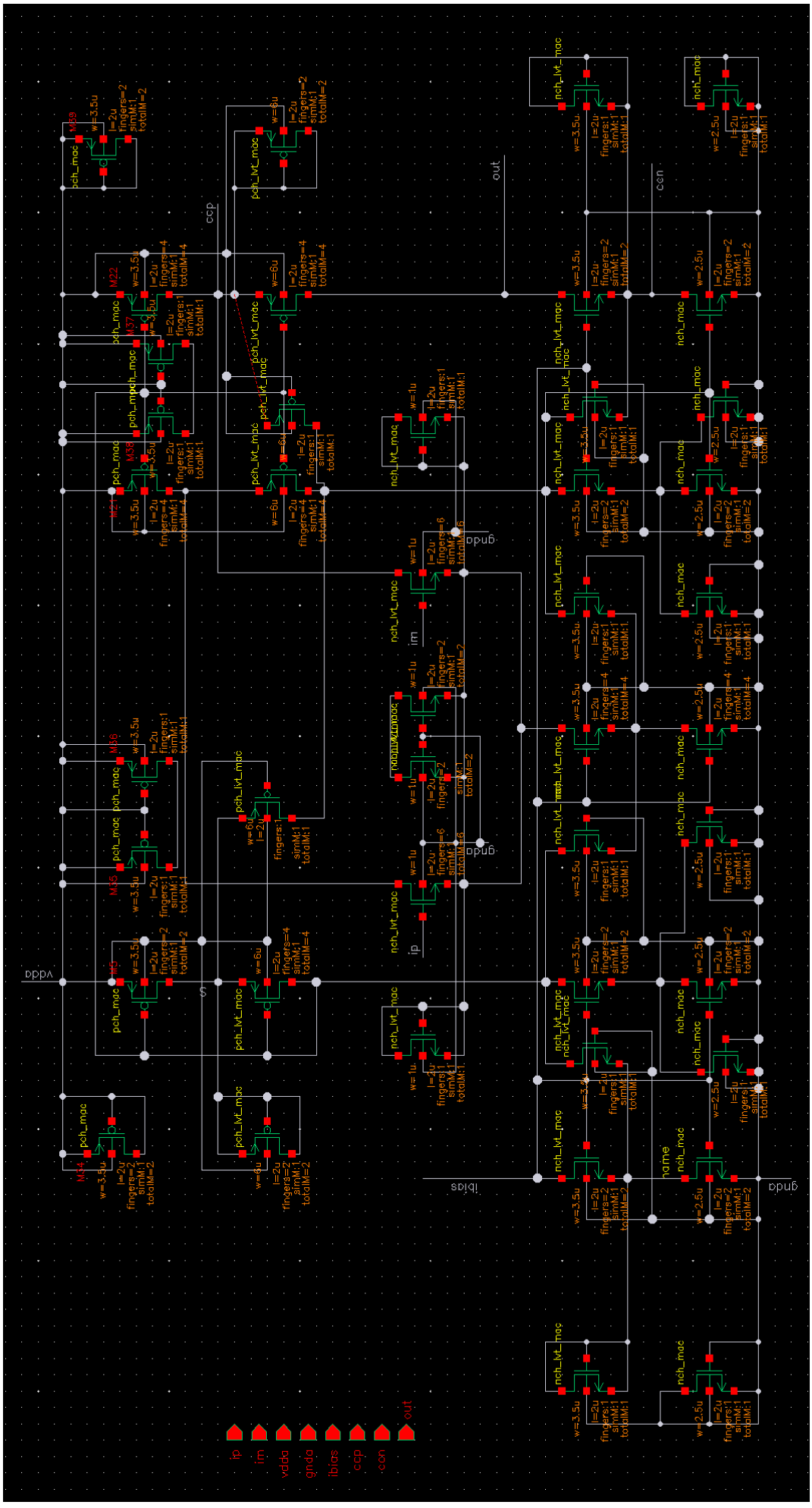
Transistor Sizes of LDO:



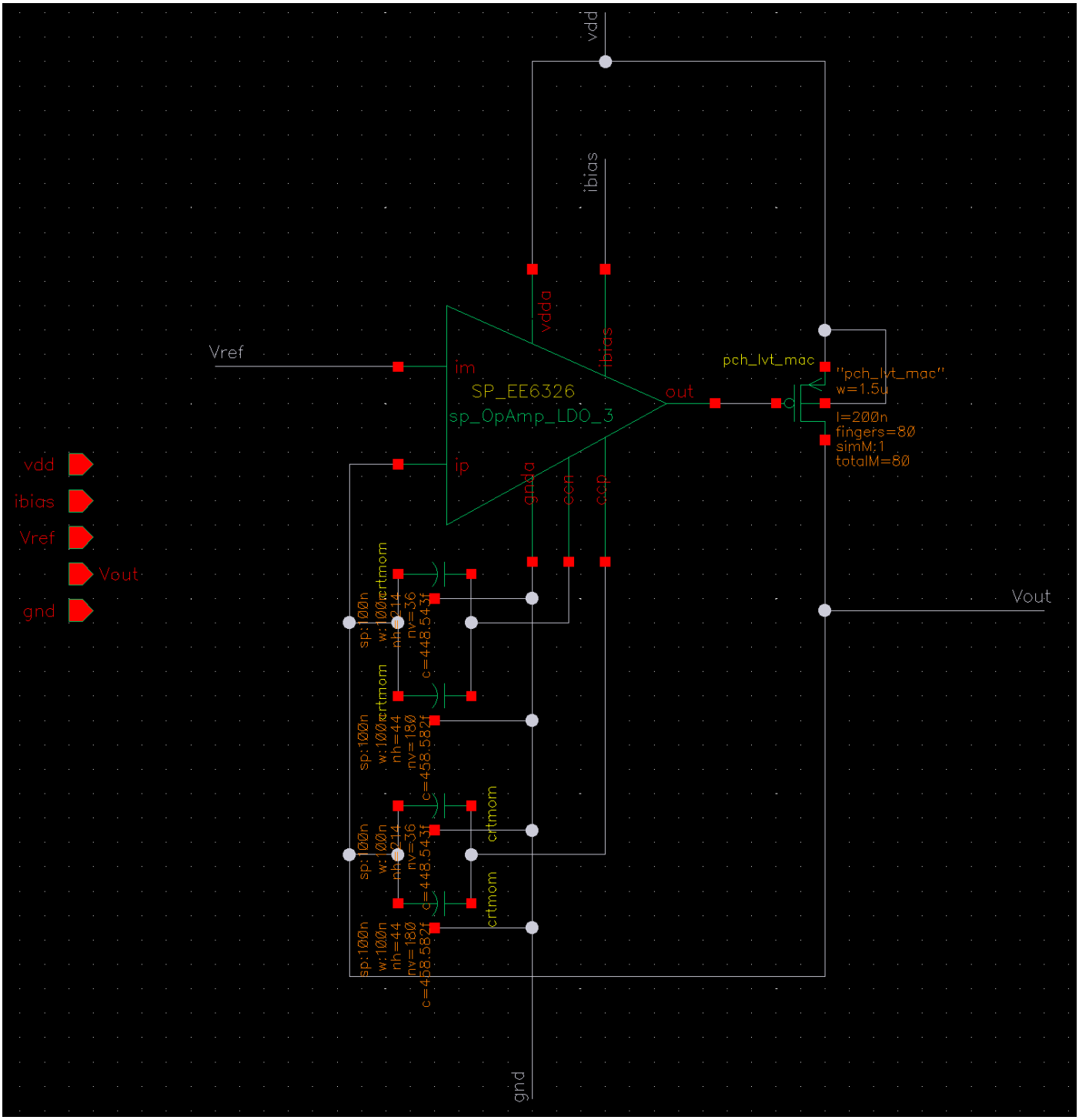
To reduce oscillations at output when load curent is changed abruptly, Compensation Capacitors (C_c) of values $\mathbf{907.125}\ \boldsymbol{fF}$ are used. These capacitors can be of higher values to have less oscillations (more stable response), which increases the layout area as capacitors take lots of space.

The capacitor is split into two parallel combination of capacitors with values $\mathbf{458.582}\ \boldsymbol{fF}$ and $\mathbf{448.543}\ \boldsymbol{fF}$ to make layout compact by maintaining the aspect ratio.

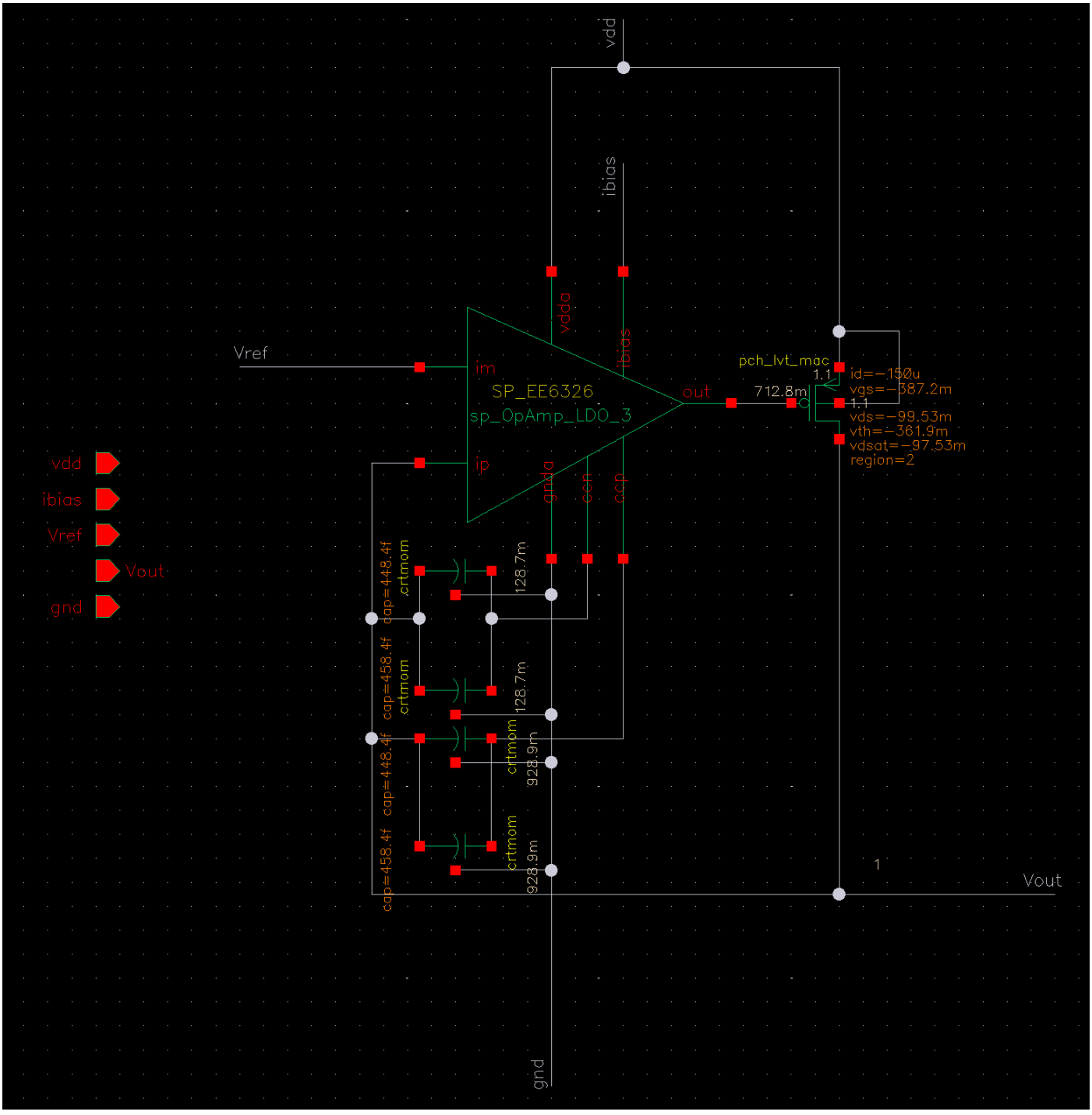
Transistor Sizes of OpAmp for LDO:



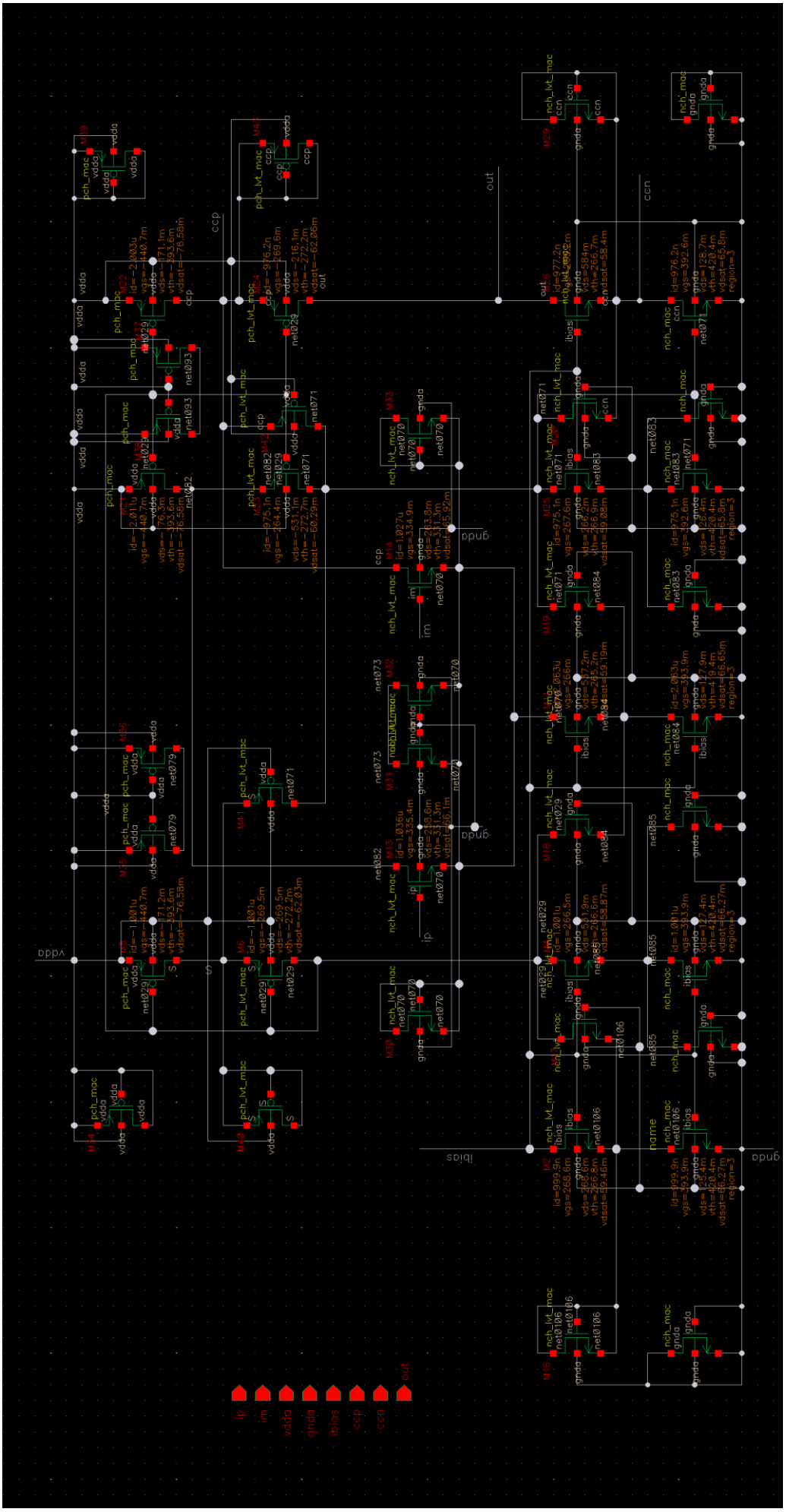
Transistor Size for LDO:



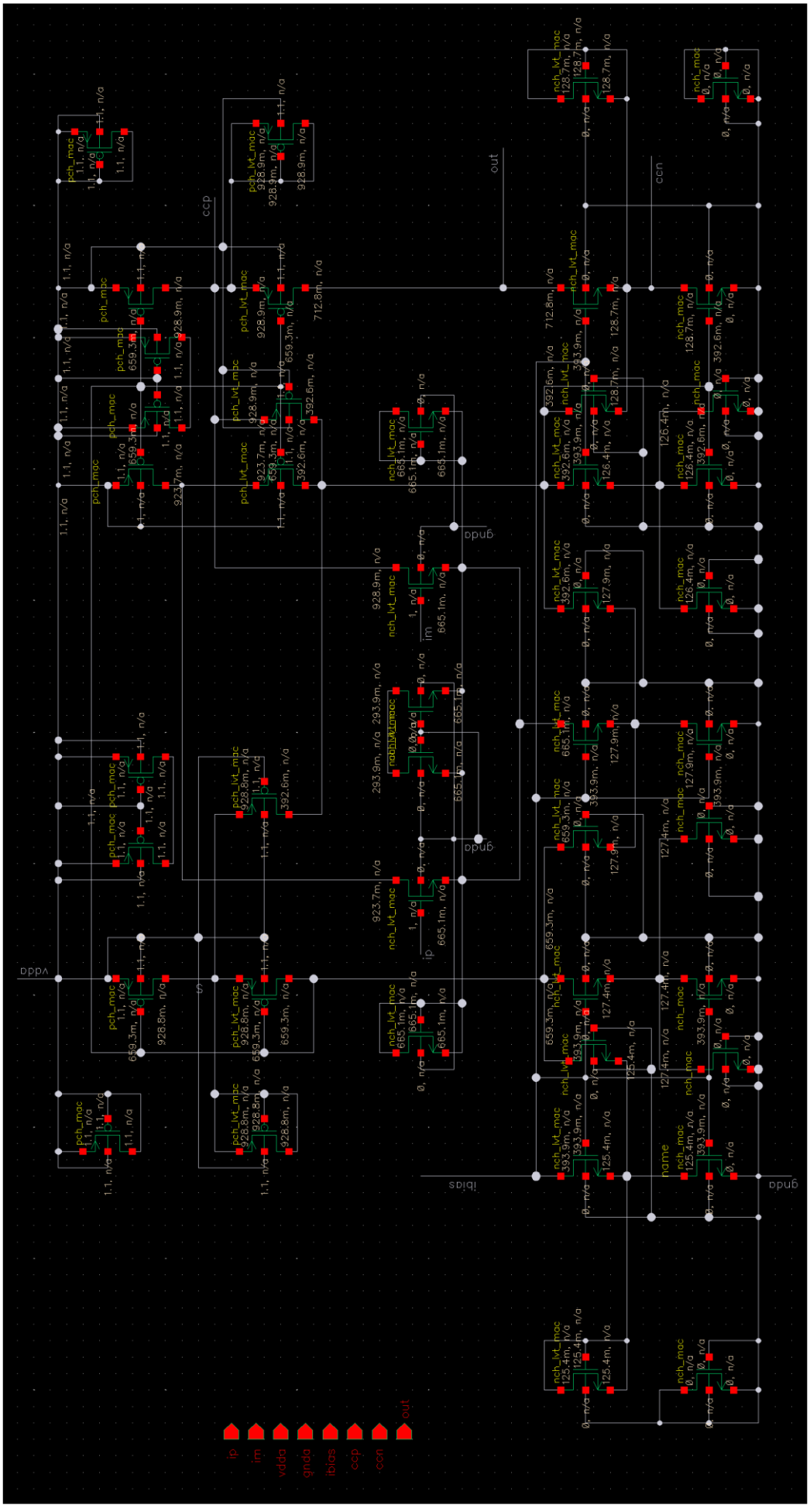
Annotated DC Operating Points LDO $(1.1v, tt, 50°C)$***:***



Annotated DC Operating Points of OpAmp for LDO $(1.1v, tt, 50°C)$***:***



Annotated DC Node Voltages and Current $(1.1v, tt, 50°C)$***:***

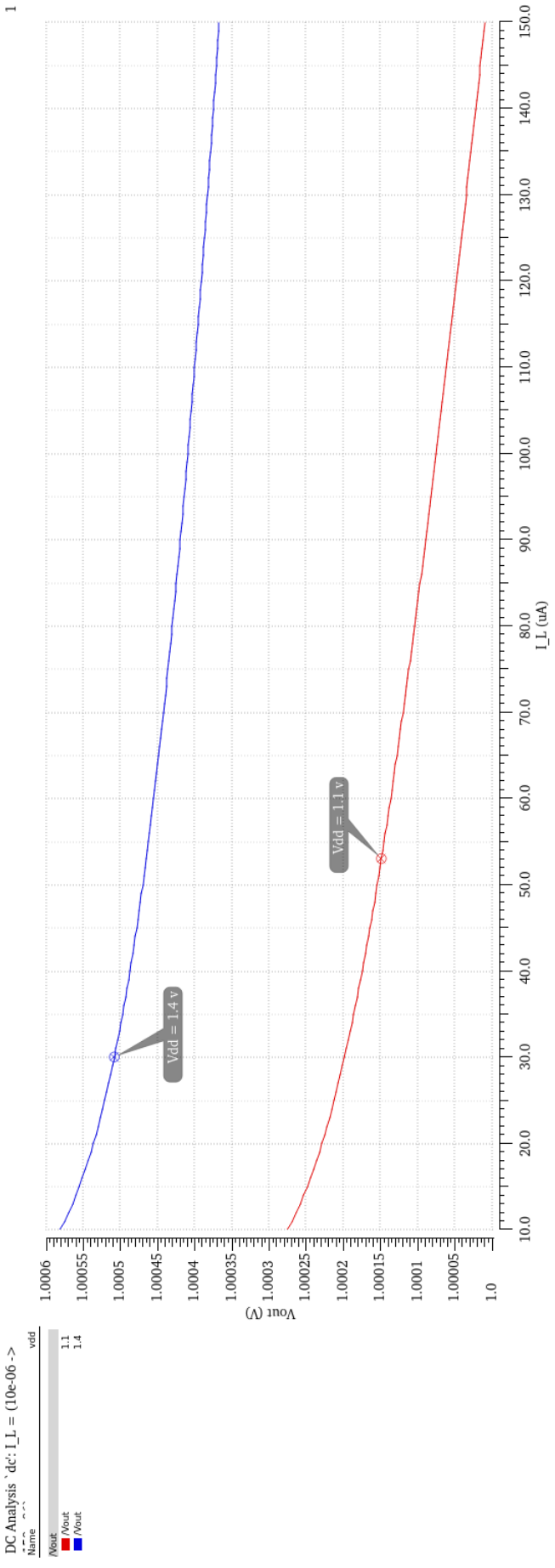


LDO Plots:

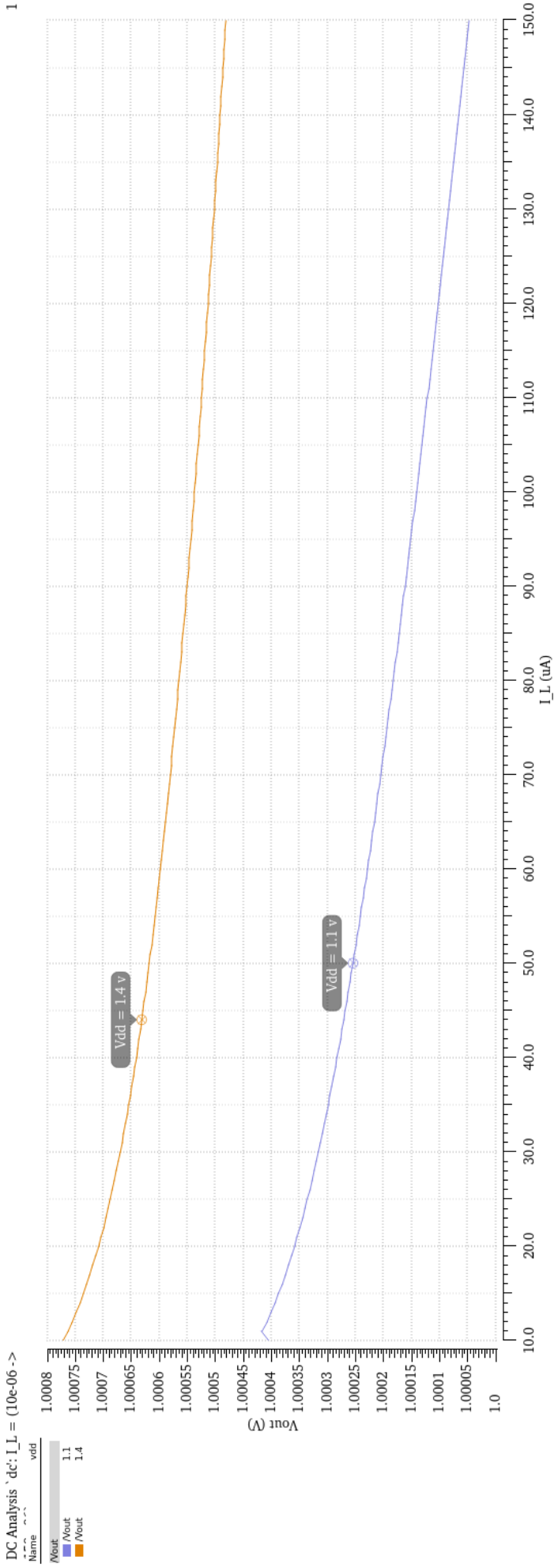
Without RC Exctraction:

A. V_{out} *vs* I_L $\{1.1v, 1.4v\}X\{ss, tt, ff\}X\{$ 0℃, 50℃, 100℃$\}$:

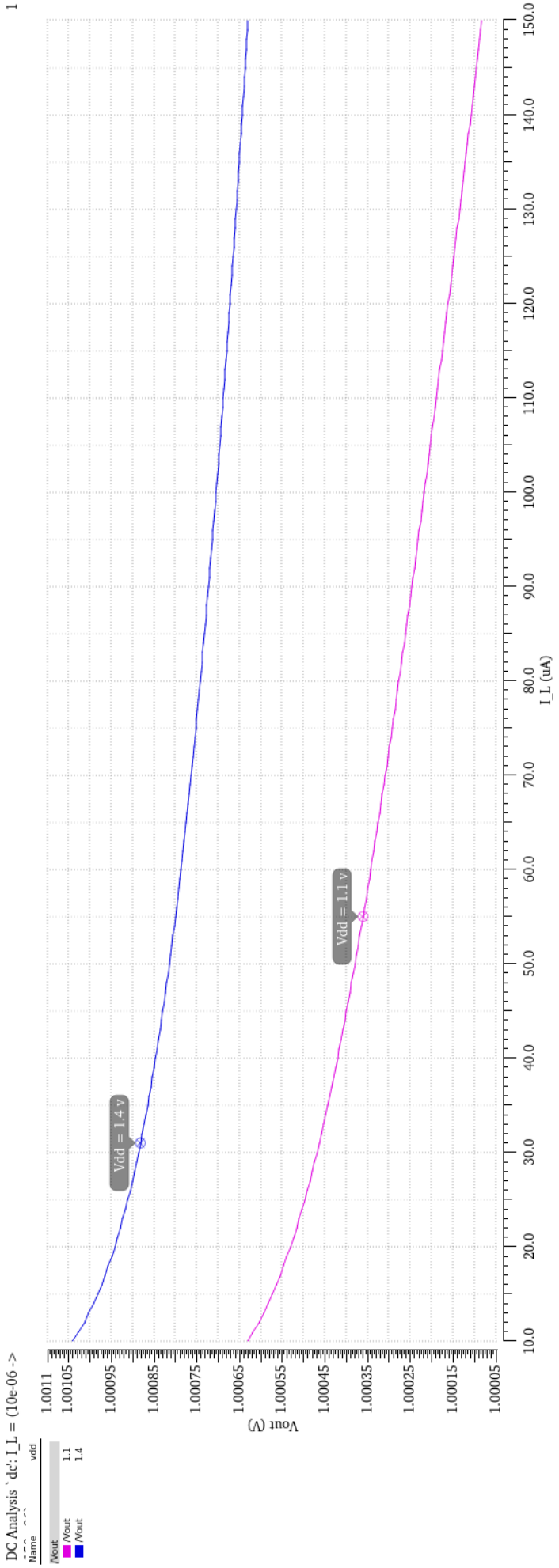
1. $\{V_{dd}, ss, 0℃\}$:



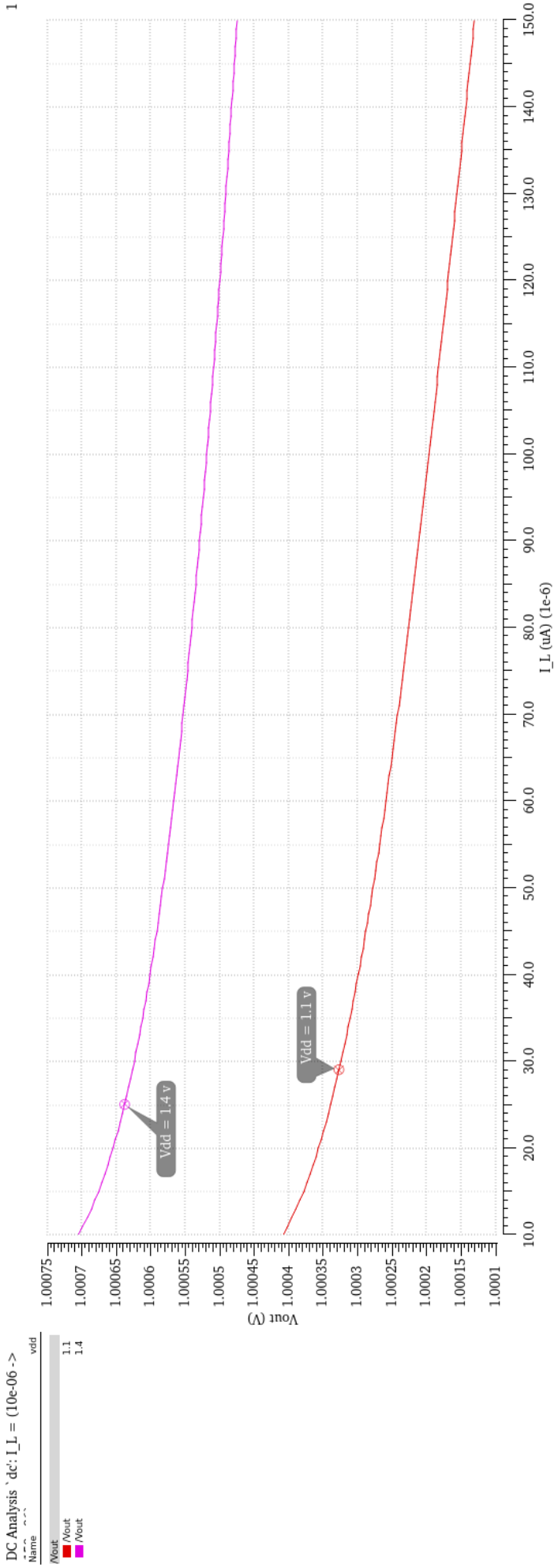
2. $\{V_{dd}, ss, 50℃\}$:


DC Analysis `dc': I_L = (10e-06 ->
Name
vdd
/Vout
/Vout
/Vout
1.1
1.4
Vout (V)
1.0008
1.00075
1.0007
1.00065
1.0006
1.00055
1.0005
1.00045
1.0004
1.00035
1.0003
1.00025
1.0002
1.00015
1.0001
1.00005
1.0
I_L (uA)
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0
Vdd = 1.4 v
Vdd = 1.1 v

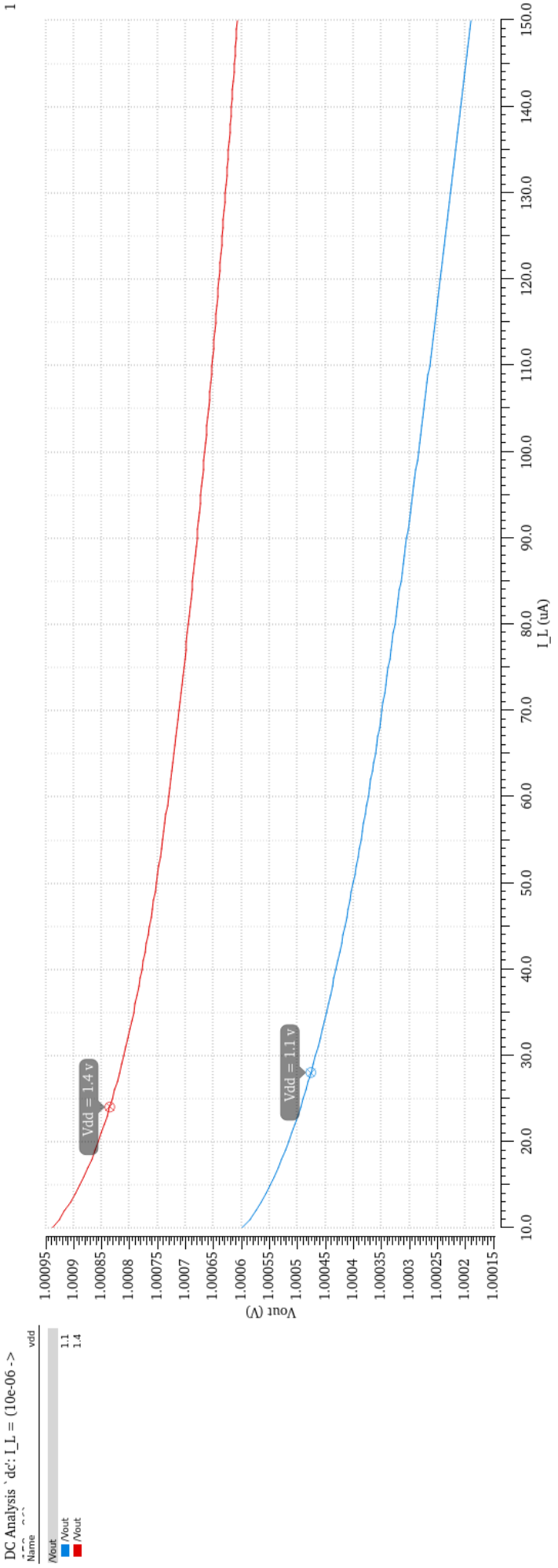
3. $\{V_{dd}, ss, 100℃\}$:


DC Analysis `dc': I_L = (10e-06 ->
Name
vdd
/Vout
/Vout
/Vout
1.1
1.4
Vout (V)
I_L (uA)
Vdd = 1.4 v
Vdd = 1.1 v
1.00111
1.00105
1.00095
1.00085
1.00075
1.00065
1.00055
1.00045
1.00035
1.00025
1.00015
1.00005
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0

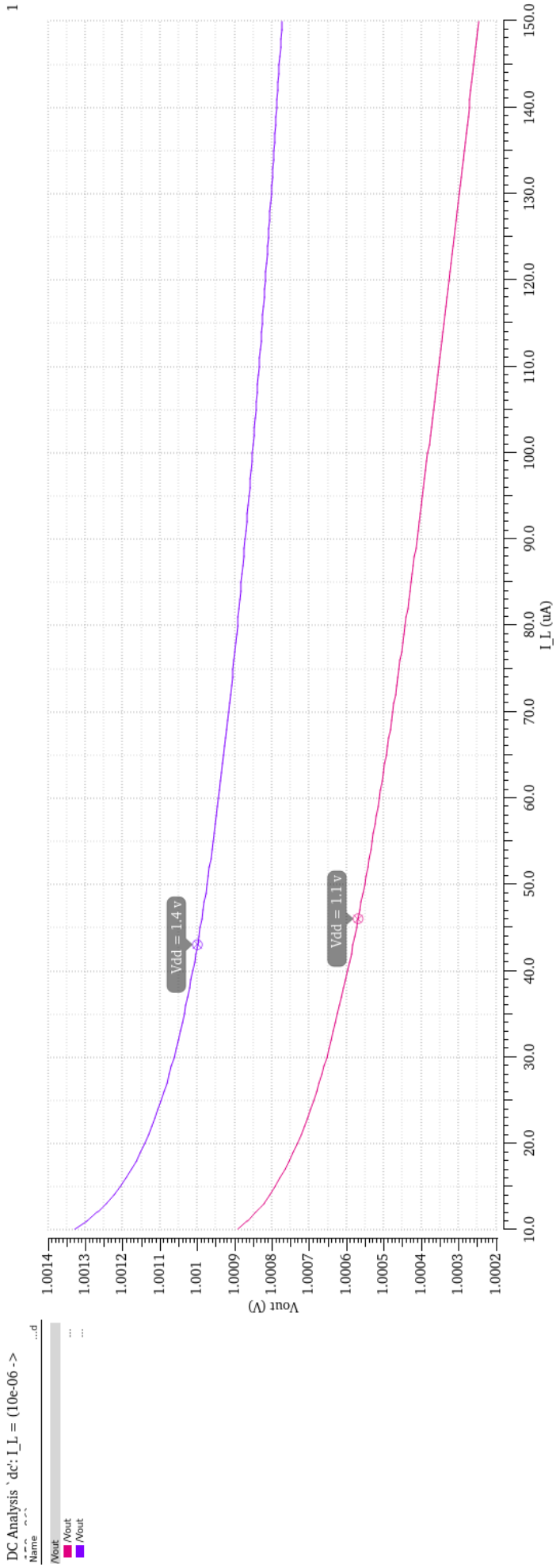
4. $\{V_{dd}, tt, 0℃\}$:


DC Analysis `dc': I_L = (10e-06 ->
Name
vdd
/Vout
/Vout
/Vout
1.1
1.4
Vout (V)
I_L (uA) (1e-6)
Vdd = 1.4 v
Vdd = 1.1 v
1.00075
1.0007
1.00065
1.0006
1.00055
1.0005
1.00045
1.0004
1.00035
1.0003
1.00025
1.0002
1.00015
1.0001
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0

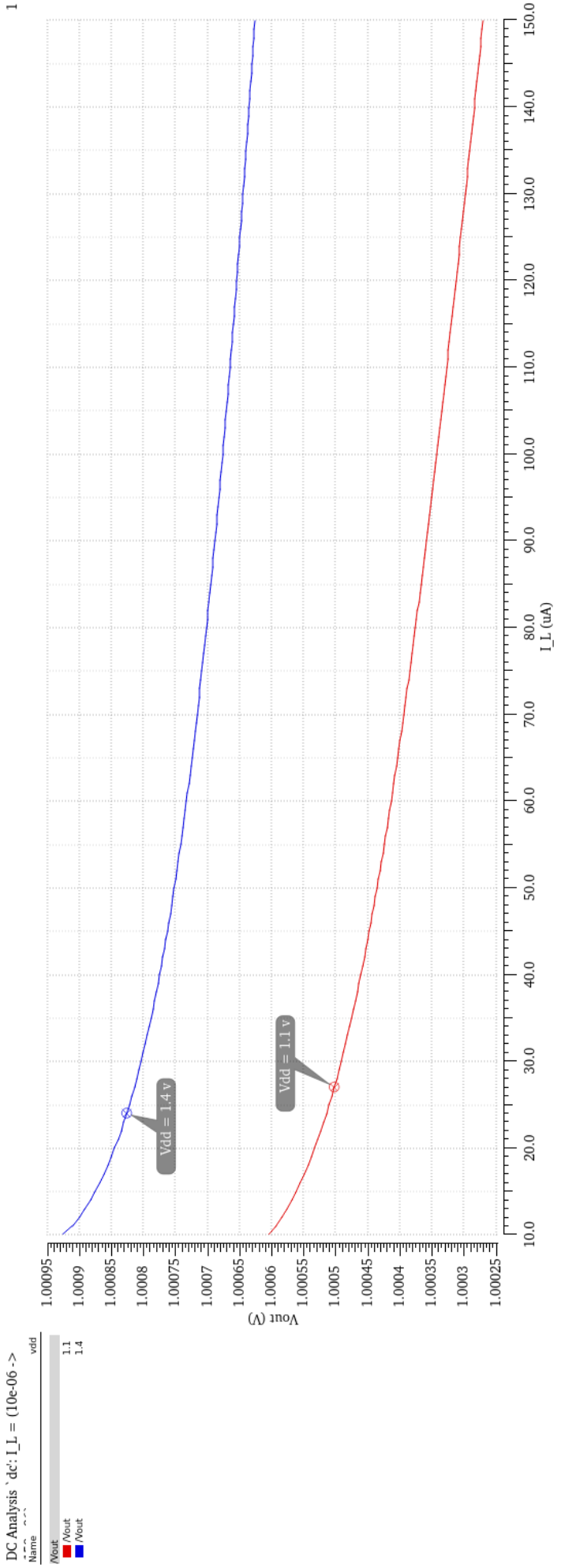
5. $\{V_{dd}, tt, 50℃\}$:


DC Analysis `dc': I_L = (10e-06 ->
Name
vdd
/Vout
1.1
1.4
/Vout
/Vout
Vout (V)
I_L (uA)
Vdd = 1.4 v
Vdd = 1.1 v

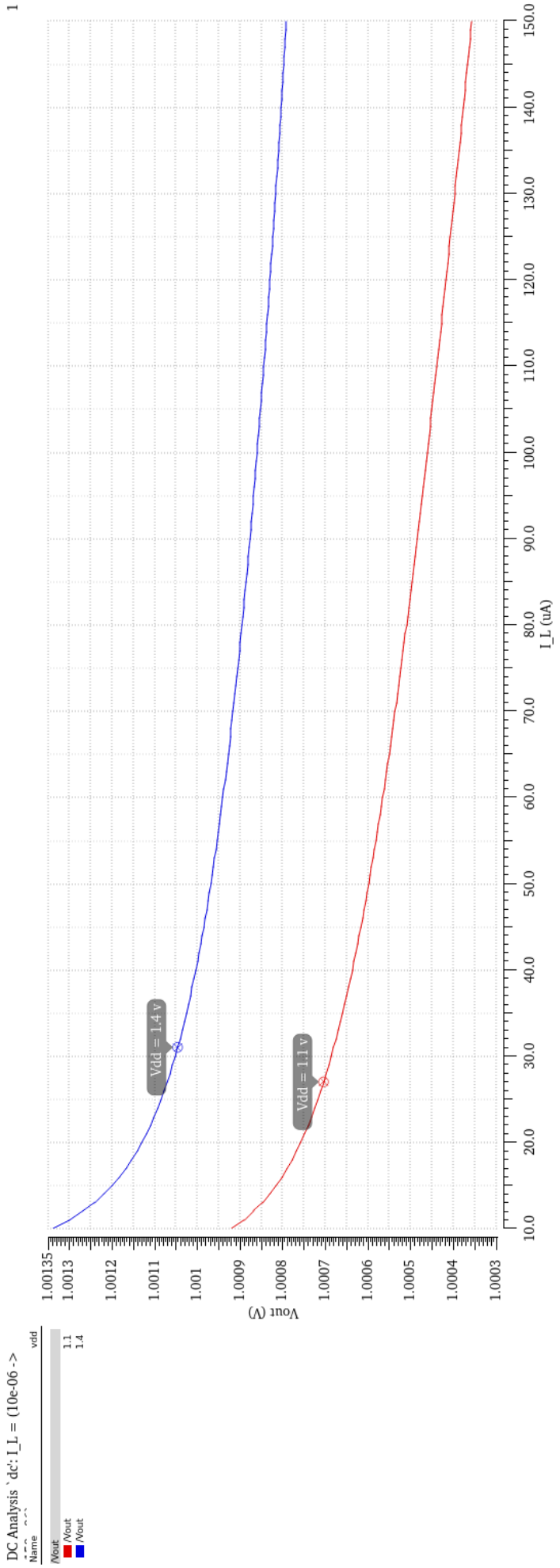
6. $\{V_{dd}, tt, 100℃\}$:


DC Analysis `dc': I_L = (10e-06 ->
Name
/Vout
/Vout
/Vout
Vout (V)
1.0014
1.0013
1.0012
1.0011
1.001
1.0009
1.0008
1.0007
1.0006
1.0005
1.0004
1.0003
1.0002
Vdd = 1.4 v
Vdd = 1.1 v
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0
I_L (uA)

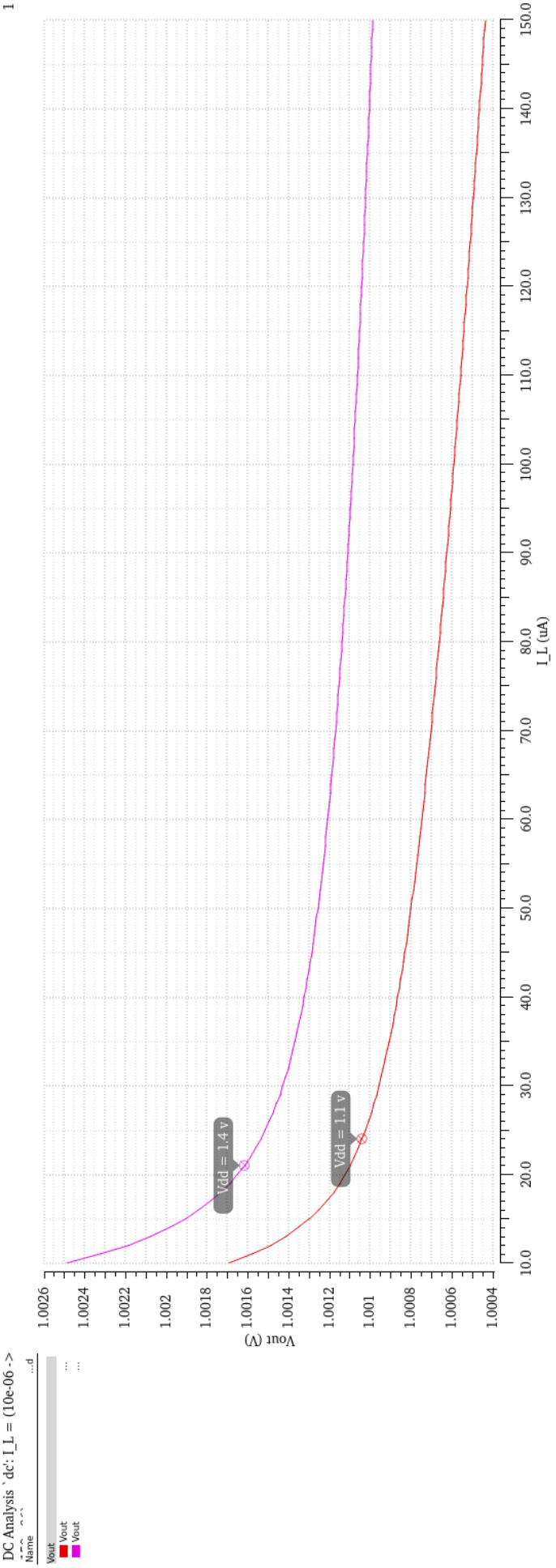
7. {V_{dd}, ff, 0℃}:


DC Analysis `dc': I_L = (10e-06 ->
Name
vdd
/Vout
/Vout
/Vout
1.1
1.4
Vout (V)
I_L (uA)
Vdd = 1.4 v
Vdd = 1.1 v
1.00095
1.0009
1.00085
1.0008
1.00075
1.0007
1.00065
1.0006
1.00055
1.0005
1.00045
1.0004
1.00035
1.0003
1.00025
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0

8. $\{V_{dd}, ff, 50℃\}$:

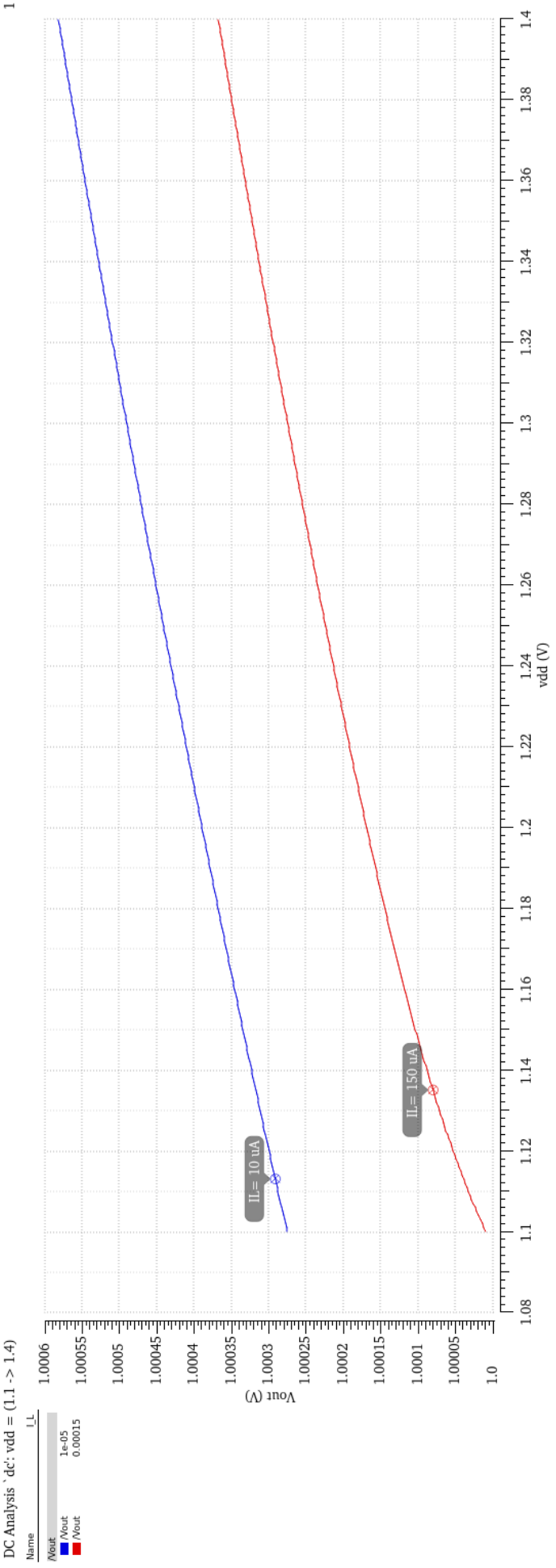

DC Analysis `dc': I_L = (10e-06 ->
Name
vdd
/Vout
/Vout
/Vout
1.1
1.4
Vout (V)
1.00135
1.0013
1.0012
1.0011
1.001
1.0009
1.0008
1.0007
1.0006
1.0005
1.0004
1.0003
I_L (uA)
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0
Vdd = 1.4 v
Vdd = 1.1 v

9. $\{V_{dd}, ff, 100℃\}$:

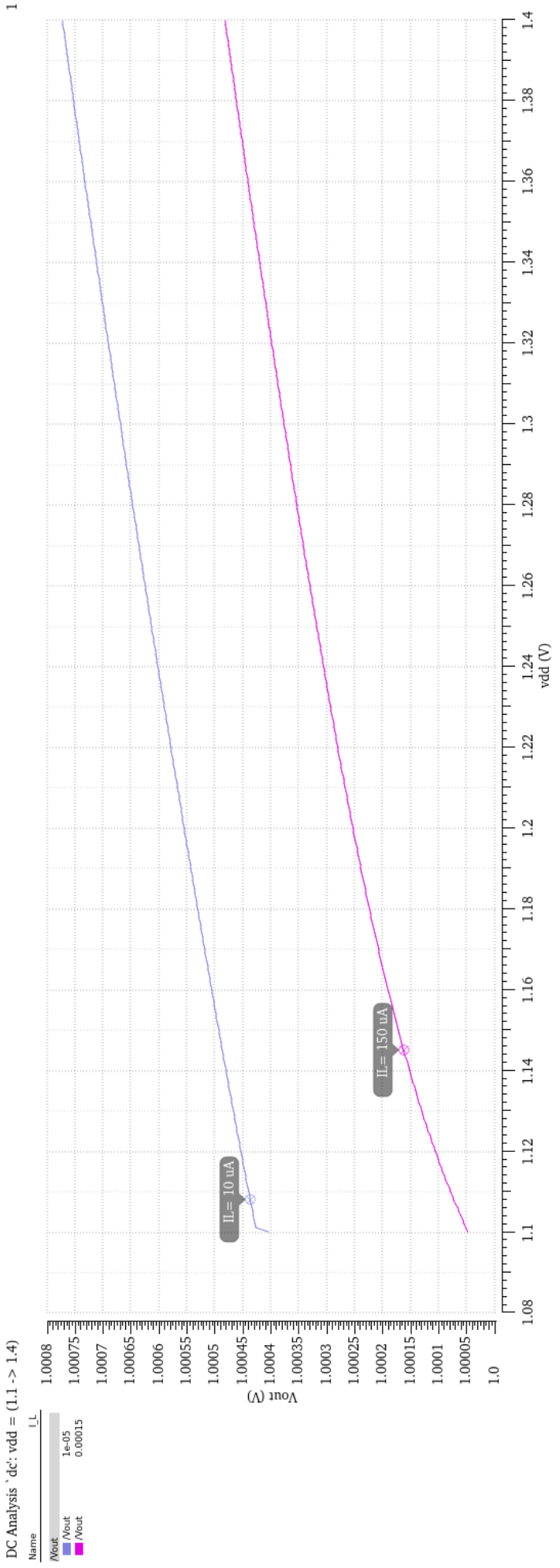

1
DC Analysis `dc': I_L = (10e-06 ->
Name
Vout
Vout
Vout
Vout (V)
1.0026
1.0024
1.0022
1.002
1.0018
1.0016
1.0014
1.0012
1.001
1.0008
1.0006
1.0004
Vdd = 1.4 v
Vdd = 1.1 v
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0
I_L (uA)

B. V_{out} *vs* V_{DD}**:**

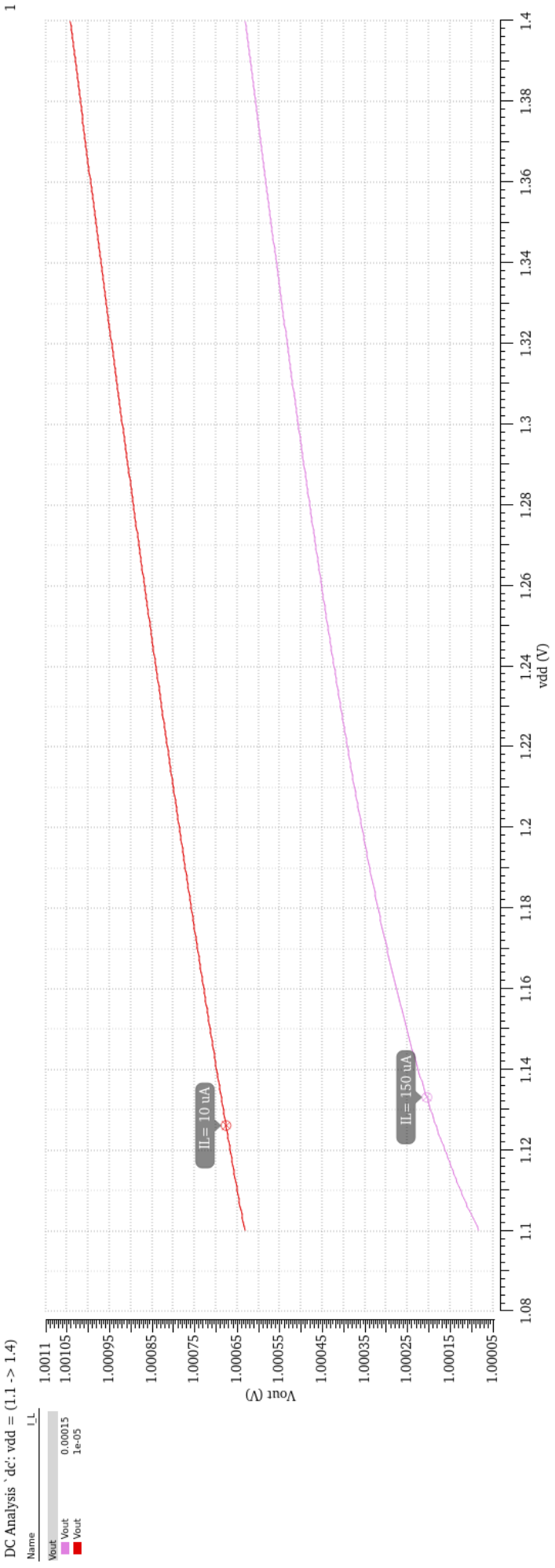
1. $\{V_{dd}, ss, 0℃\}$**:**



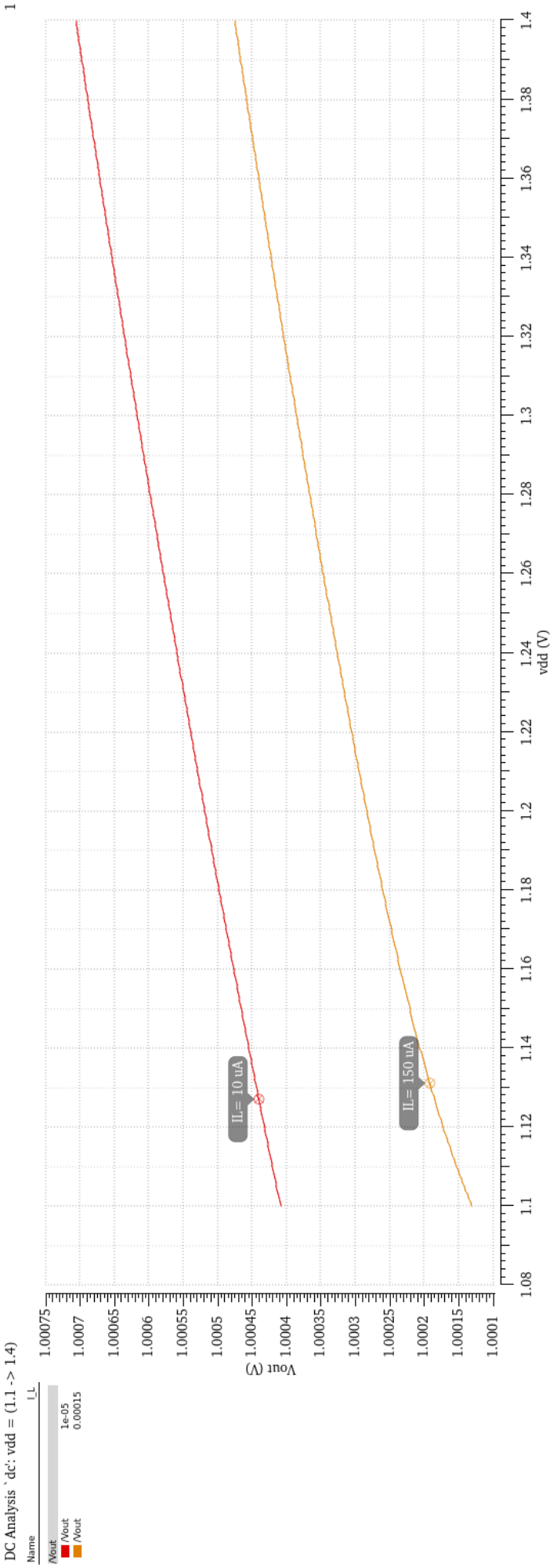
2. $\{V_{dd}, ss, 50℃\}$:


DC Analysis `dc': vdd = (1.1 -> 1.4)
Name
I_L
/Vout
/Vout
/Vout
1e-05
0.00015
Vout (V)
vdd (V)
IL= 10 uA
IL= 150 uA

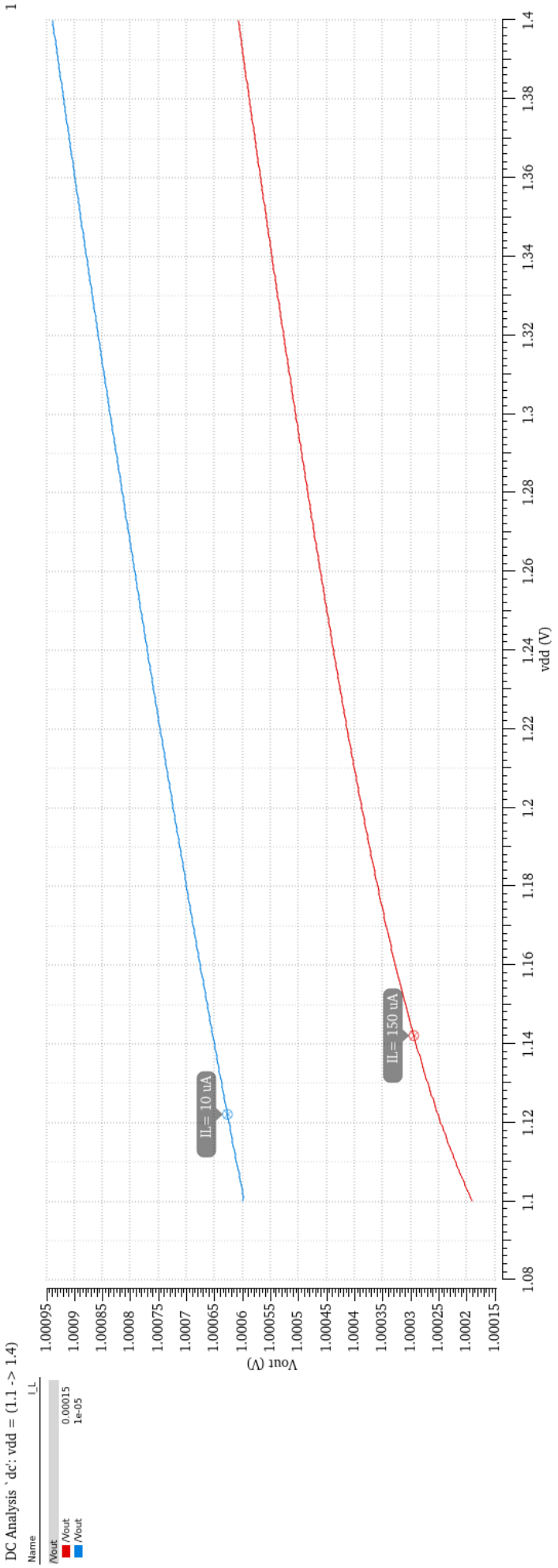
3. $\{V_{dd}, ss, 100℃\}$:


DC Analysis `dc': vdd = (1.1 -> 1.4)
Name
I_L
Vout
Vout
Vout
0.00015
1e-05
Vout (V)
1.0011
1.00105
1.00095
1.00085
1.00075
1.00065
1.00055
1.00045
1.00035
1.00025
1.00015
1.00005
IL= 10 uA
IL= 150 uA
1.08
1.1
1.12
1.14
1.16
1.18
1.2
1.22
1.24
1.26
1.28
1.3
1.32
1.34
1.36
1.38
1.4
vdd (V)

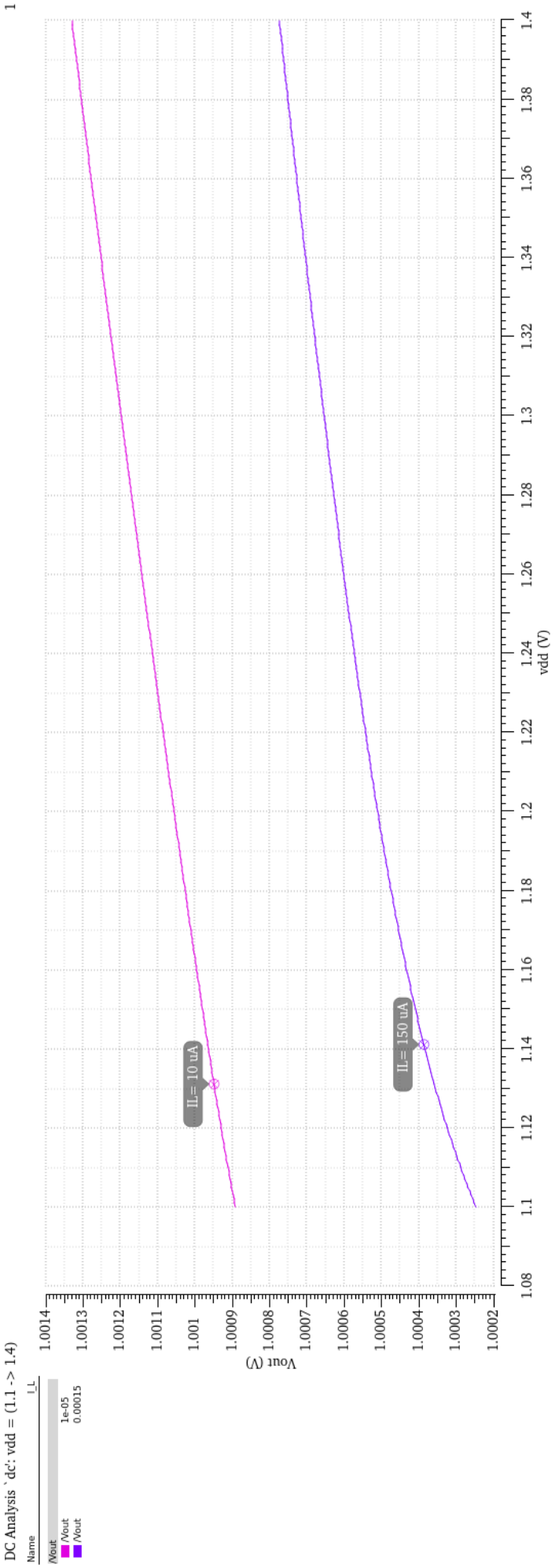
4. $\{V_{dd}, tt, 0℃\}$:


DC Analysis `dc': vdd = (1.1 -> 1.4)
Name
I_L
/Vout
/Vout
/Vout
1e-05
0.00015
IL = 10 uA
IL = 150 uA
Vout (V)
1.00075
1.0007
1.00065
1.0006
1.00055
1.0005
1.00045
1.0004
1.00035
1.0003
1.00025
1.0002
1.00015
1.0001
vdd (V)
1.08
1.1
1.12
1.14
1.16
1.18
1.2
1.22
1.24
1.26
1.28
1.3
1.32
1.34
1.36
1.38
1.4

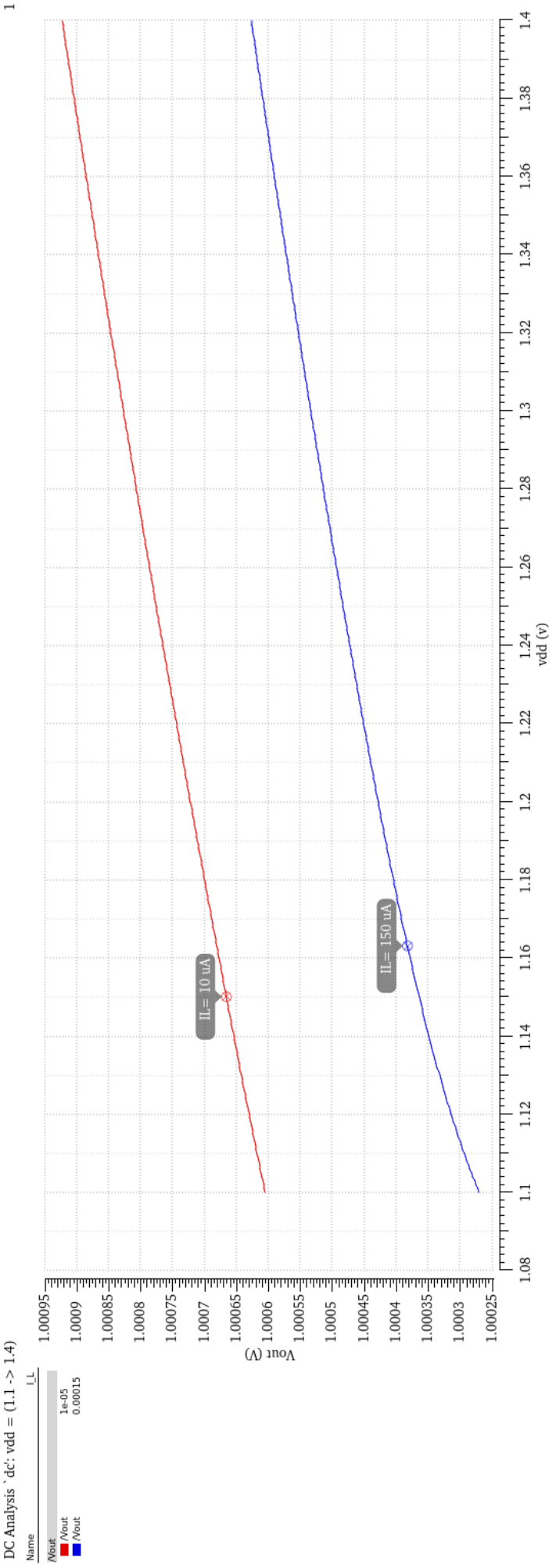
5. $\{V_{dd}, tt, 50℃\}$:


DC Analysis `dc': vdd = (1.1 -> 1.4)
Name
I_L
/Vout
/Vout
/Vout
0.00015
1e-05
IL= 10 uA
IL= 150 uA
Vout (V)
vdd (V)
1.00095
1.0009
1.00085
1.0008
1.00075
1.0007
1.00065
1.0006
1.00055
1.0005
1.00045
1.0004
1.00035
1.0003
1.00025
1.0002
1.00015
1.08
1.1
1.12
1.14
1.16
1.18
1.2
1.22
1.24
1.26
1.28
1.3
1.32
1.34
1.36
1.38
1.4

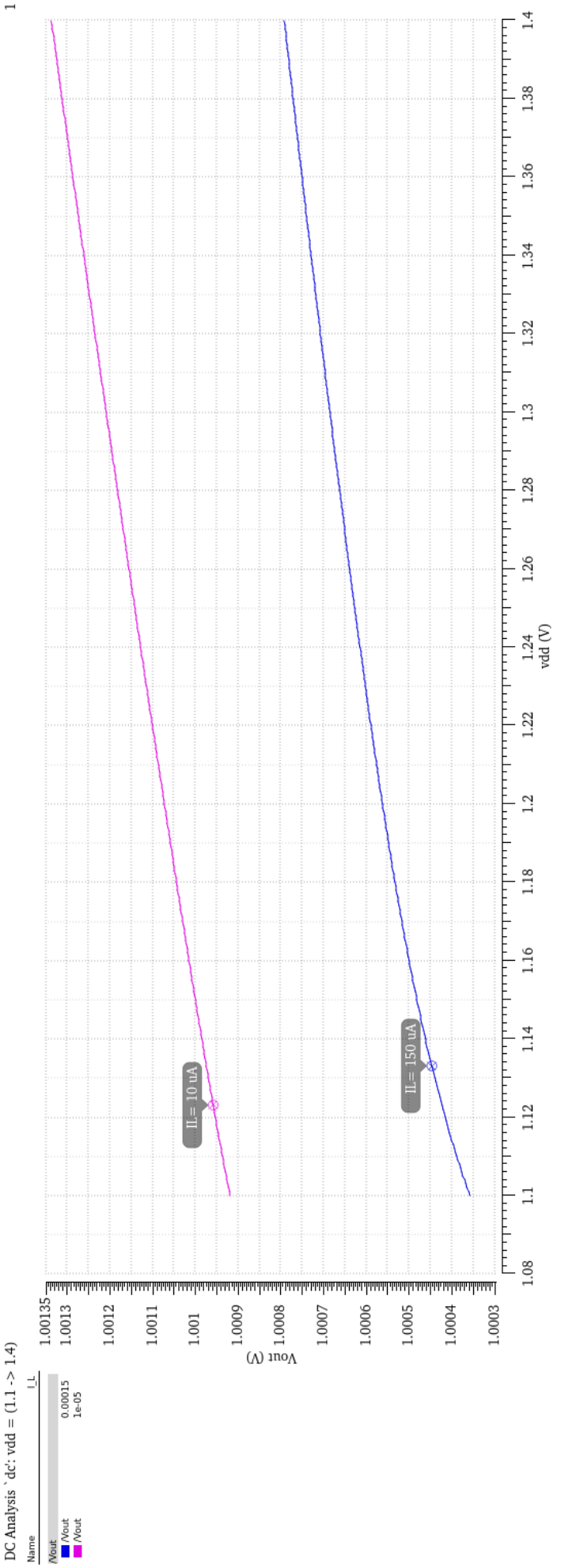
6. $\{V_{dd}, tt, 100℃\}$:


DC Analysis `dc': vdd = (1.1 -> 1.4)
Name
I_L
/Vout
/Vout
/Vout
1e-05
0.00015
Vout (V)
vdd (V)
IL= 10 uA
IL= 150 uA

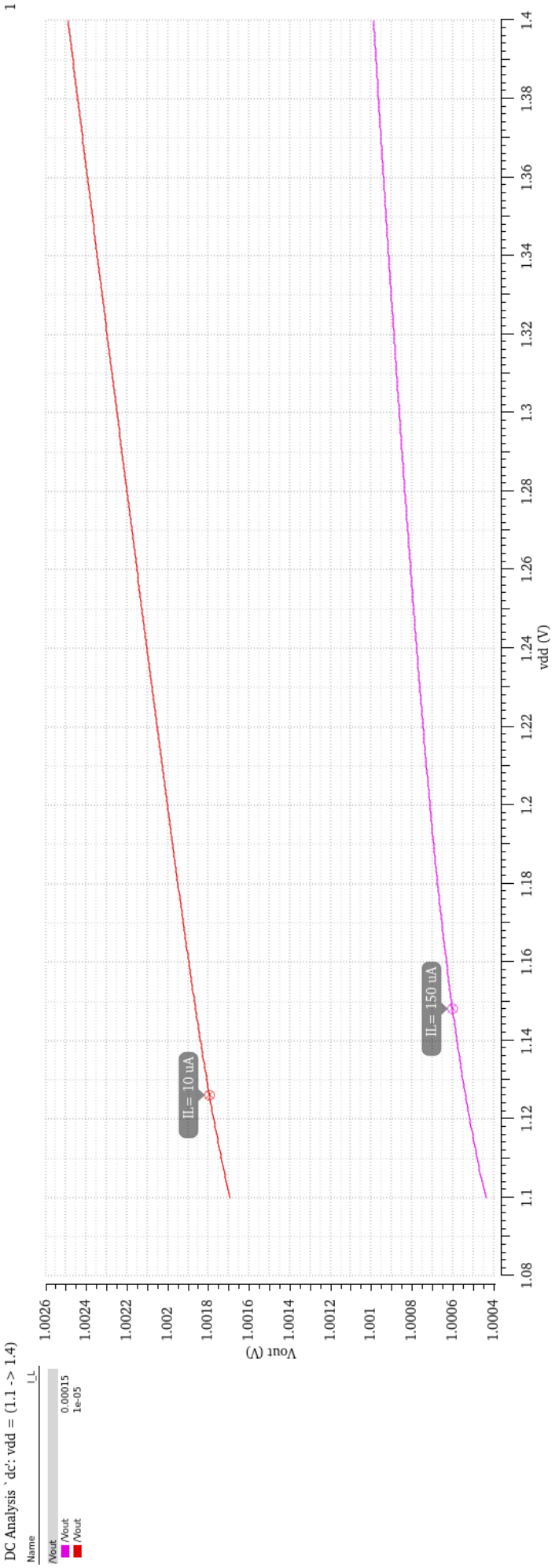
7. $\{V_{dd}, ff, 0℃\}$:


DC Analysis `dc': vdd = (1.1 -> 1.4)
Name
I_L
/Vout
/Vout
/Vout
1e-05
0.00015
Vout (V)
vdd (v)
IL= 10 uA
IL= 150 uA

8. $\{V_{dd}, ff, 50℃\}$:


DC Analysis `dc': vdd = (1.1 -> 1.4)
Name
I_L
/Vout
/Vout
/Vout
0.00015
1e-05
Vout (V)
1.00135
1.0013
1.0012
1.0011
1.001
1.0009
1.0008
1.0007
1.0006
1.0005
1.0004
1.0003
vdd (V)
1.08
1.1
1.12
1.14
1.16
1.18
1.2
1.22
1.24
1.26
1.28
1.3
1.32
1.34
1.36
1.38
1.4
IL= 10 uA
IL= 150 uA

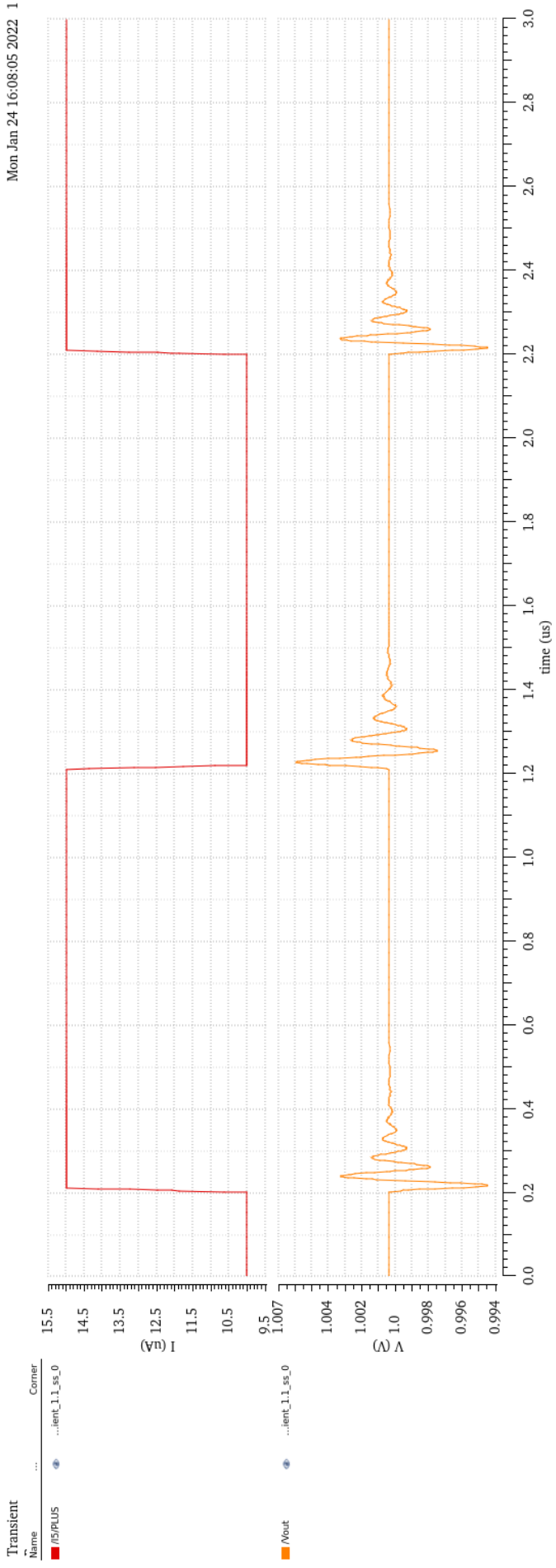
9. $\{V_{dd}, ff, 100℃\}$:


DC Analysis `dc': vdd = (1.1 -> 1.4)
Name
I_L
/Vout
/Vout
/Vout
0.00015
1e-05
Vout (V)
1.0026
1.0024
1.0022
1.002
1.0018
1.0016
1.0014
1.0012
1.001
1.0008
1.0006
1.0004
IL= 10 uA
IL= 150 uA
1.08
1.1
1.12
1.14
1.16
1.18
1.2
1.22
1.24
1.26
1.28
1.3
1.32
1.34
1.36
1.38
1.4
vdd (V)

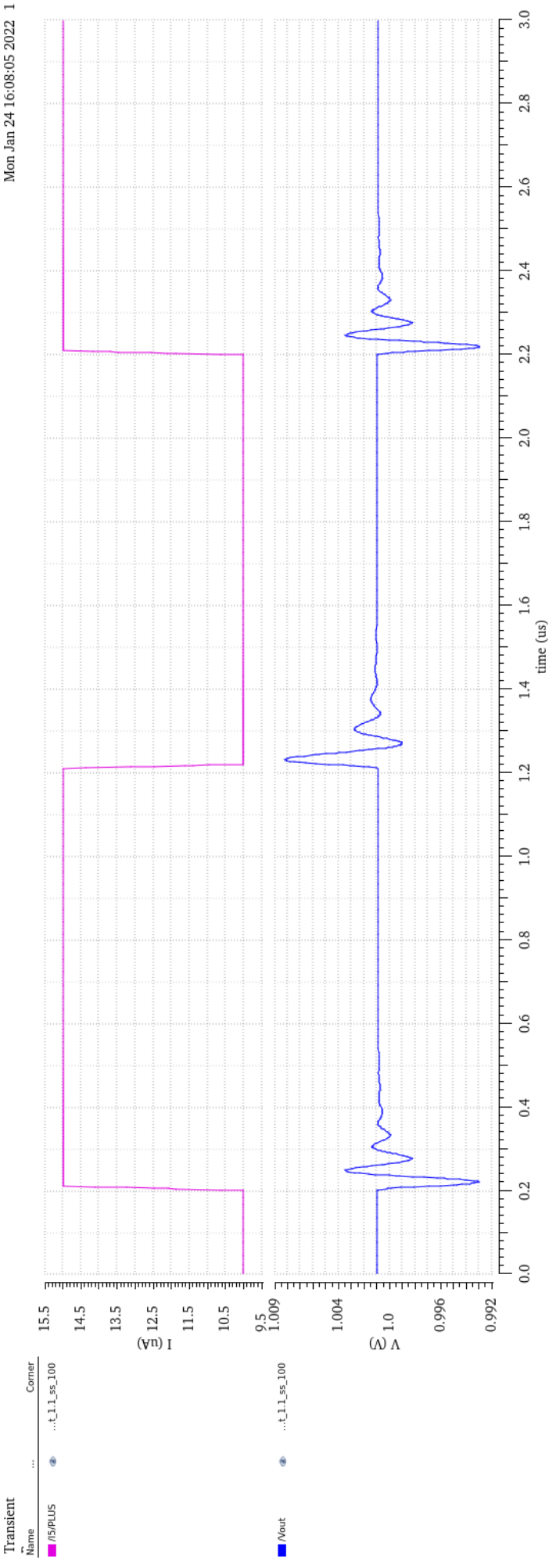
Transient Plots:

A. Current Step $10\,uA - 15uA$:

1. $\{1.1\,v, ss, 0℃\}$:

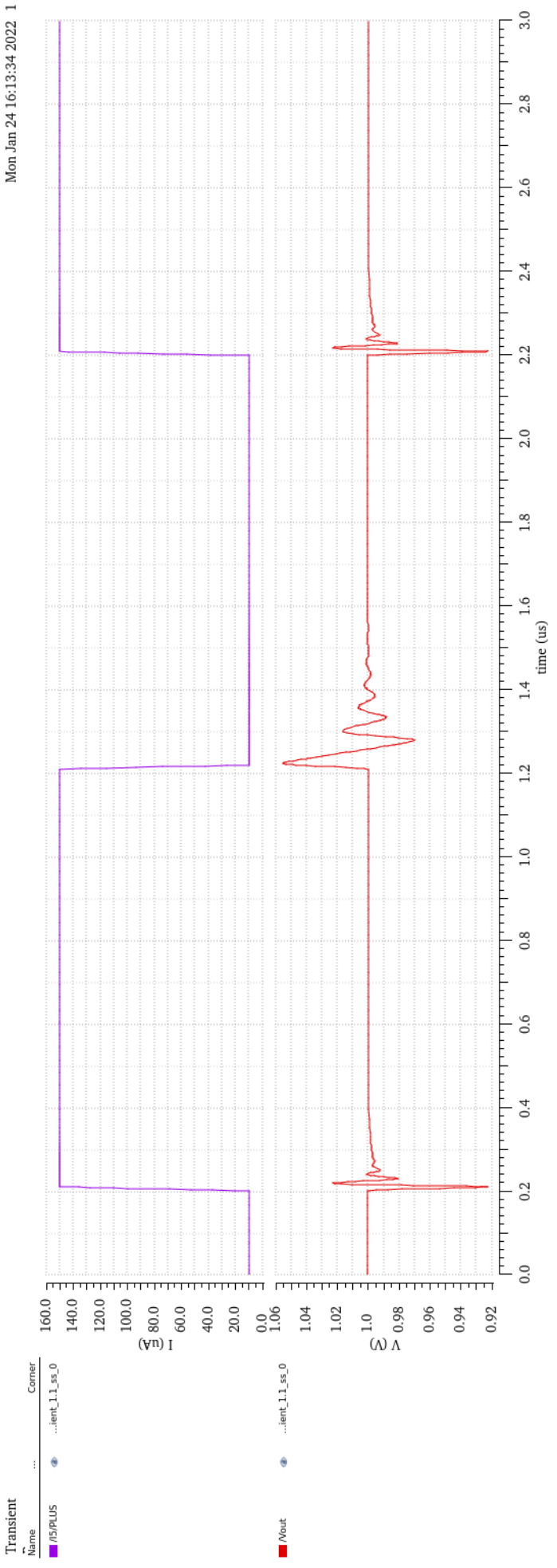


2. $\{\mathbf{1.1}\,\boldsymbol{v}, \boldsymbol{ss}, \mathbf{100}℃\}$**:**

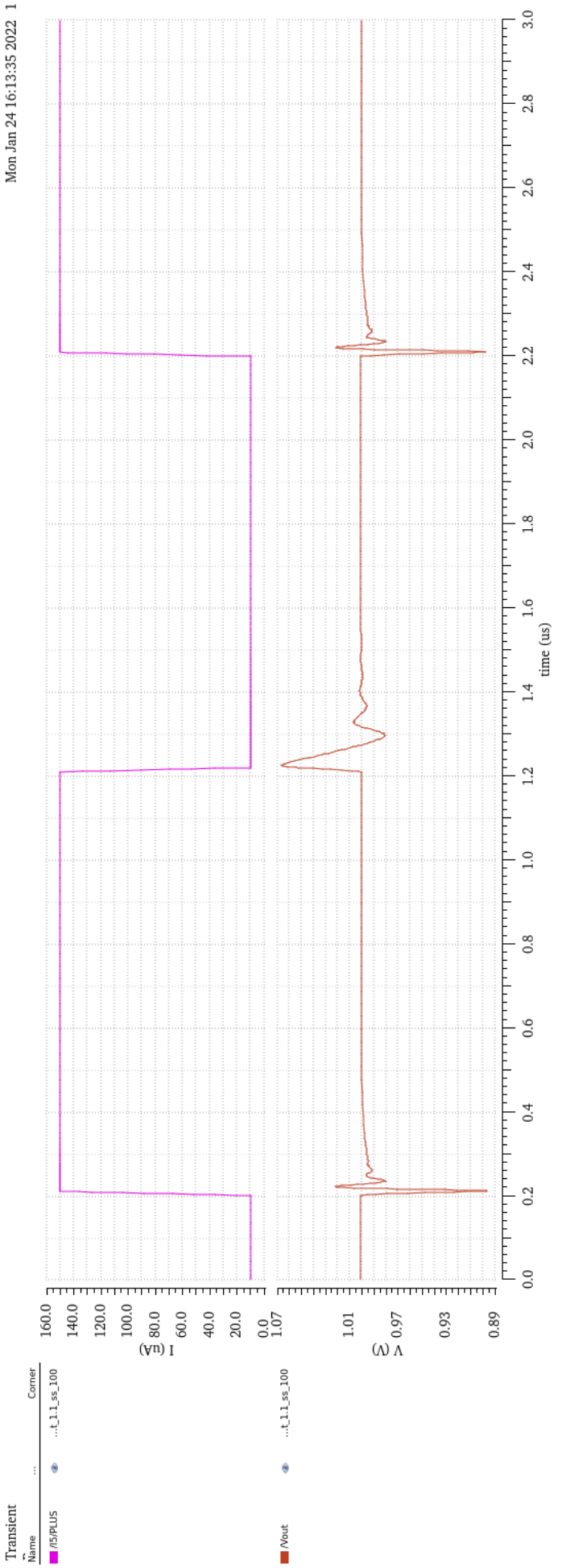


B. Current Step $10\ uA - 150\ uA$:

1. $\{1.1\ v, ss, 0℃\}$:



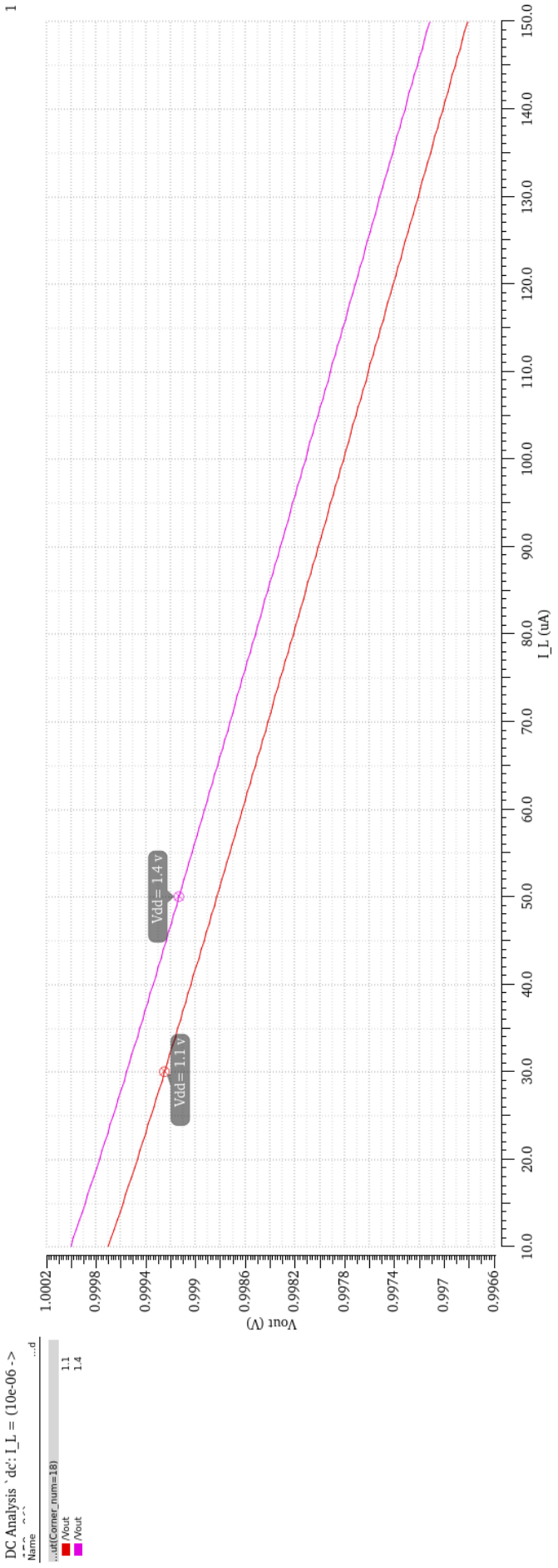
2. $\{1.1\,v, ss, 100℃\}$:


Mon Jan 24 16:13:35 2022 1
Transient
Name
Corner
/I5/PLUS
...t_1.1_ss_100
/Vout
...t_1.1_ss_100
I (uA)
V (V)
time (us)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
2.2
2.4
2.6
2.8
3.0
160.0
140.0
120.0
100.0
80.0
60.0
40.0
20.0
0.0
1.07
1.01
0.97
0.93
0.89

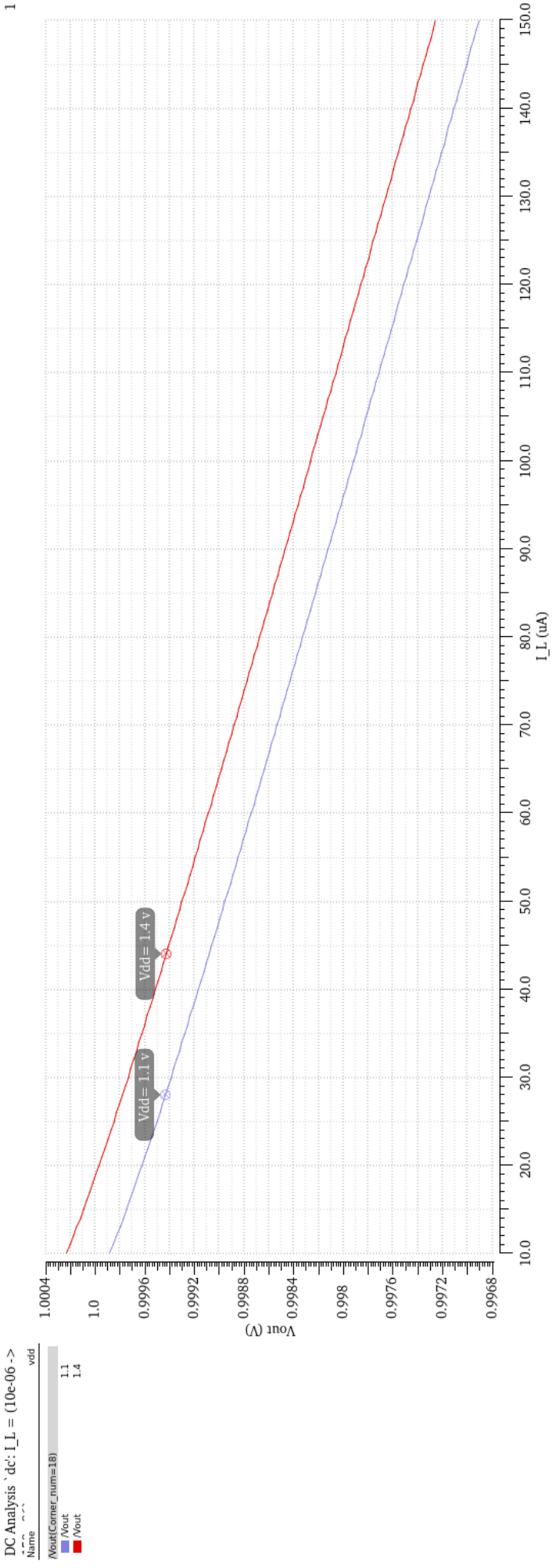
With RC Extracted Netlist:

V_{out} vs I_L :

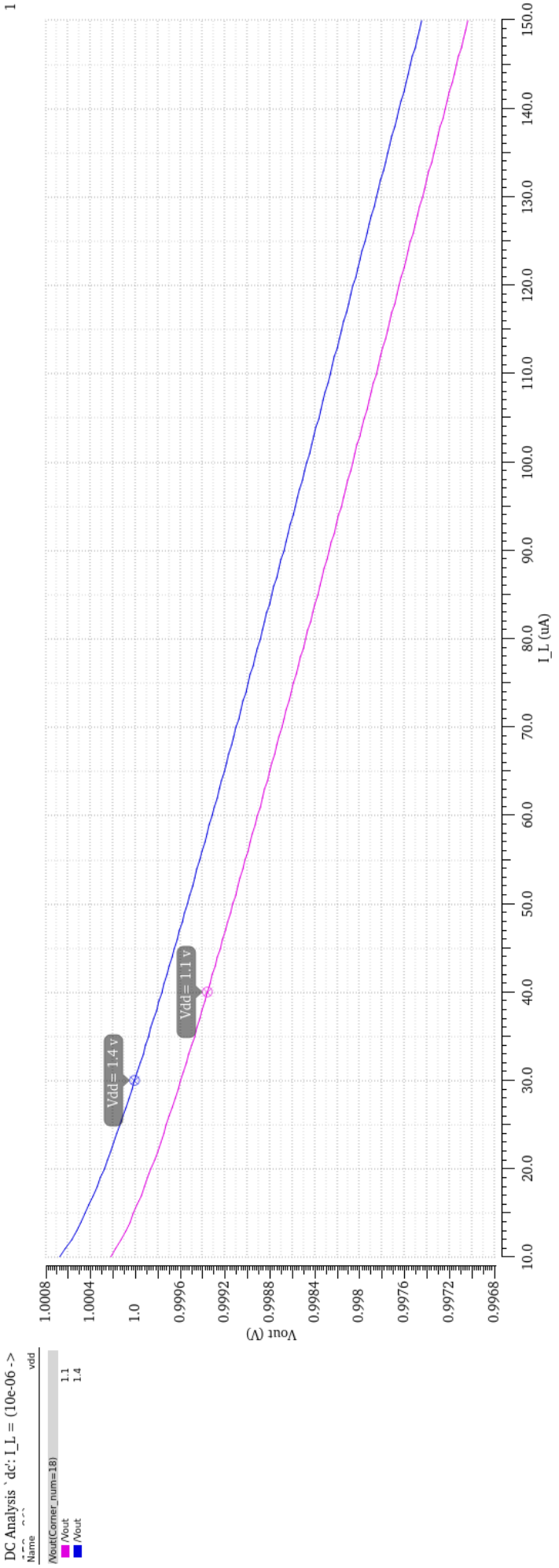
1. $\{V_{dd}, ss, 0℃\}$:



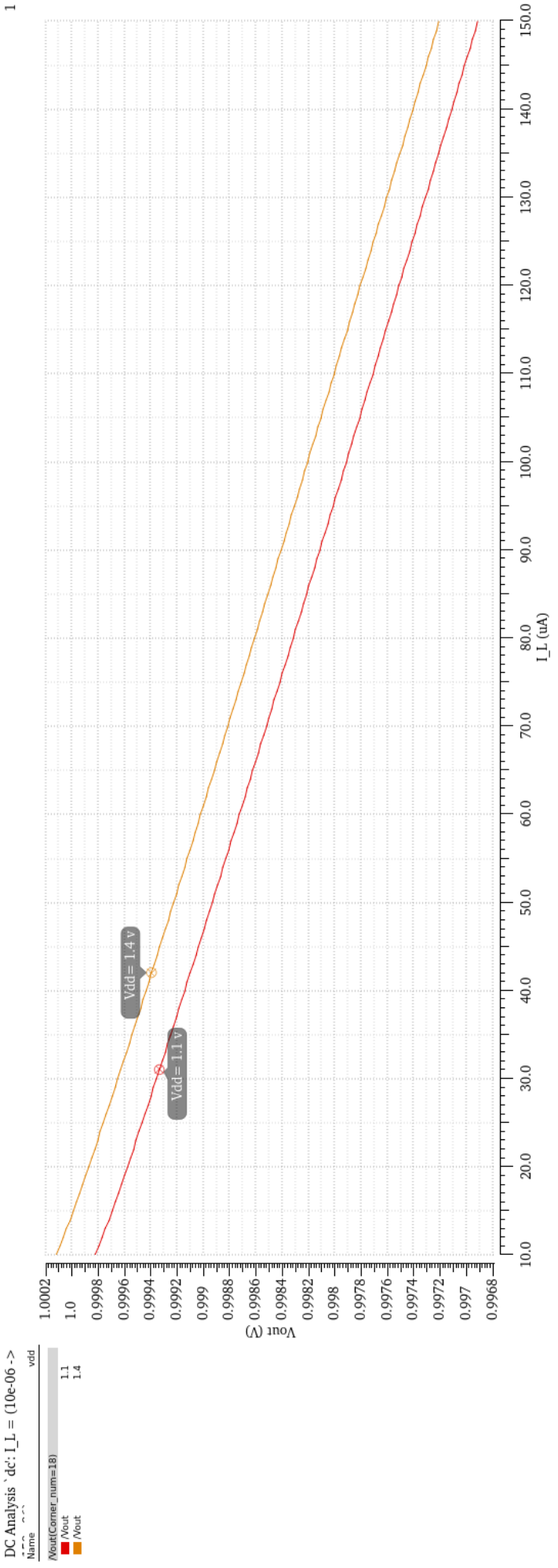
2. $\{V_{dd}, ss, 50℃\}$:


DC Analysis ` dc': I_L = (10e-06 ->
Name
vdd
/Vout(Corner_num=18)
/Vout
/Vout
1.1
1.4
Vdd = 1.4 v
Vdd = 1.1 v
Vout (V)
1.0004
1.0
0.9996
0.9992
0.9988
0.9984
0.998
0.9976
0.9972
0.9968
I_L (uA)
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0

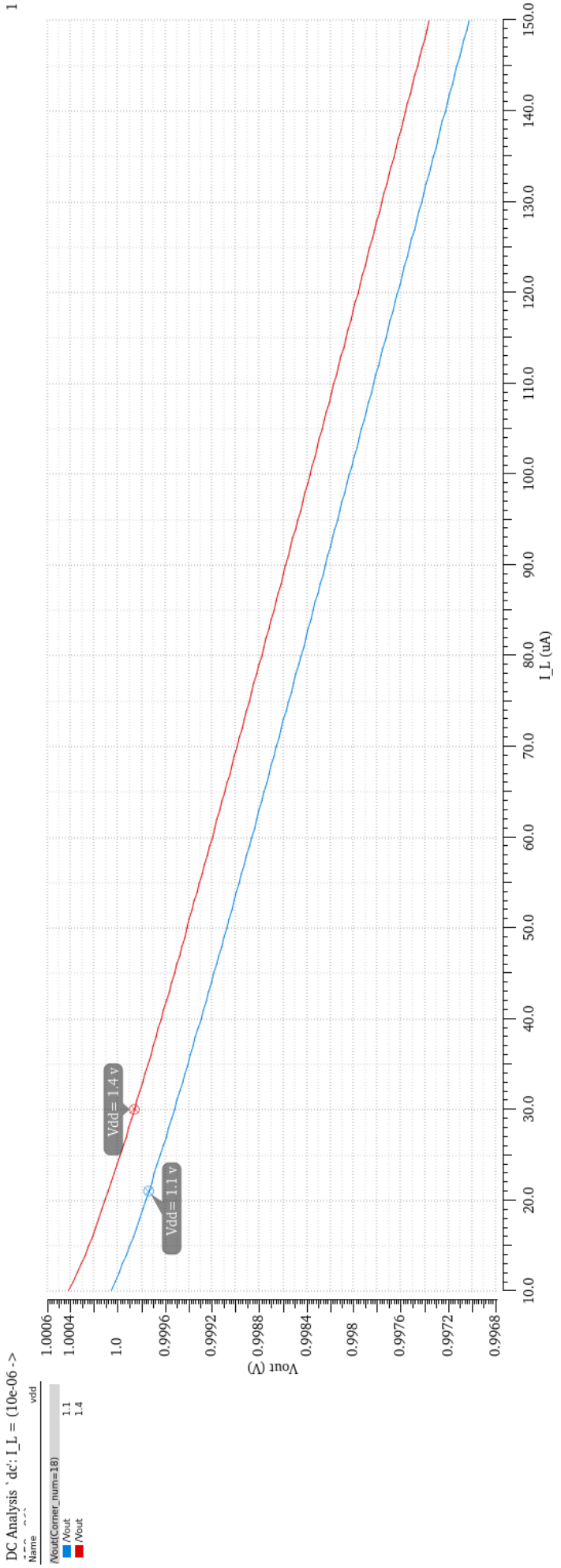
3. $\{V_{dd}, ss, 100℃\}$:


DC Analysis `dc': I_L = (10e-06 ->
Name
vdd
/Vout(Corner_num=18)
/Vout
/Vout
1.1
1.4
Vdd = 1.4 v
Vdd = 1.1 v
Vout (V)
1.0008
1.0004
1.0
0.9996
0.9992
0.9988
0.9984
0.998
0.9976
0.9972
0.9968
I_L (uA)
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0

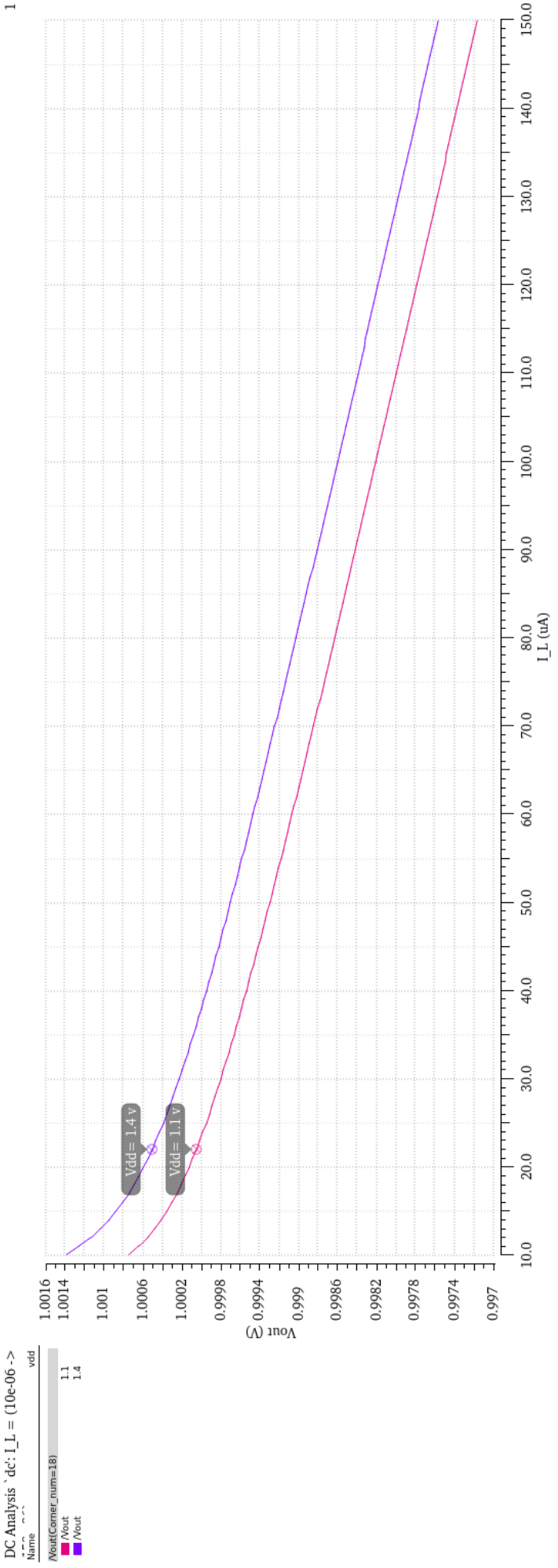
4. $\{V_{dd}, tt, 0℃\}$**:**


DC Analysis `dc': I_L = (10e-06 ->
Name
vdd
/Vout(Corner_num=18)
/Vout
/Vout
1.1
1.4
Vdd = 1.4 V
Vdd = 1.1 V
Vout (V)
I_L (uA)
1.0002
1.0
0.9998
0.9996
0.9994
0.9992
0.999
0.9988
0.9986
0.9984
0.9982
0.998
0.9978
0.9976
0.9974
0.9972
0.997
0.9968
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0

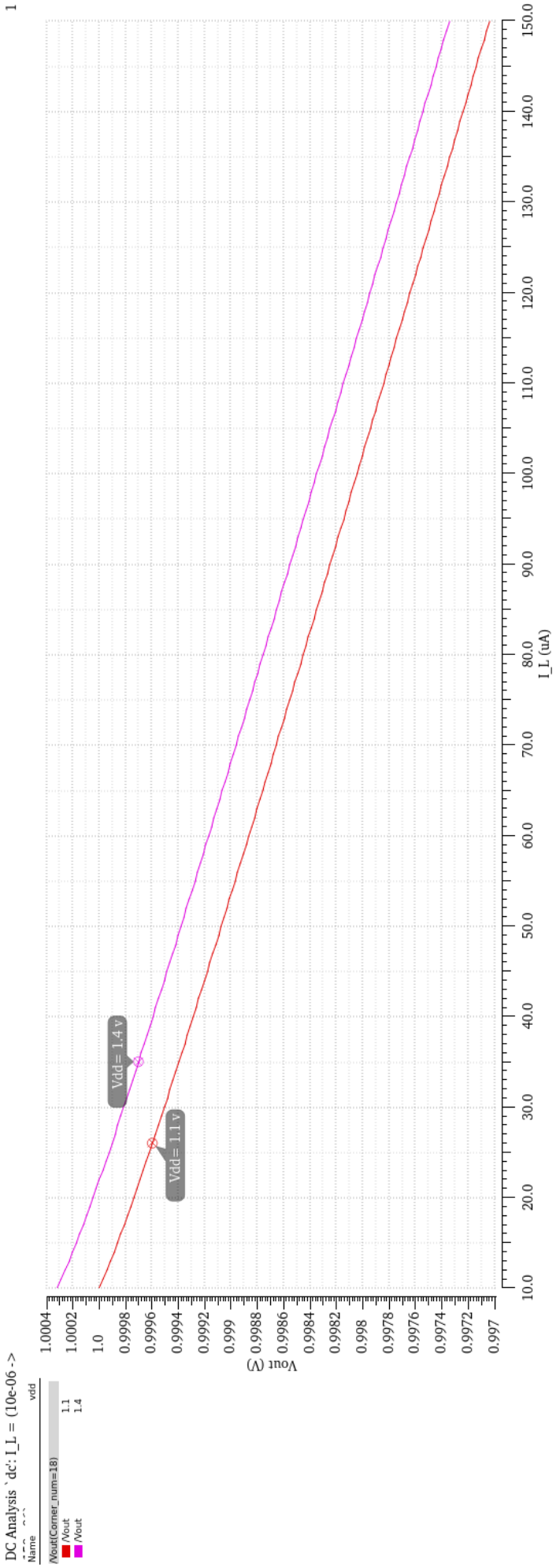
5. $\{V_{dd}, tt, 50℃\}$:


DC Analysis `dc': I_L = (10e-06 ->
Name
vdd
/Vout(Corner_num=18)
/Vout
/Vout
1.1
1.4
Vdd= 1.4 v
Vdd= 1.1 v
Vout (V)
I_L (uA)
1.0006
1.0004
1.0
0.9996
0.9992
0.9988
0.9984
0.998
0.9976
0.9972
0.9968
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0

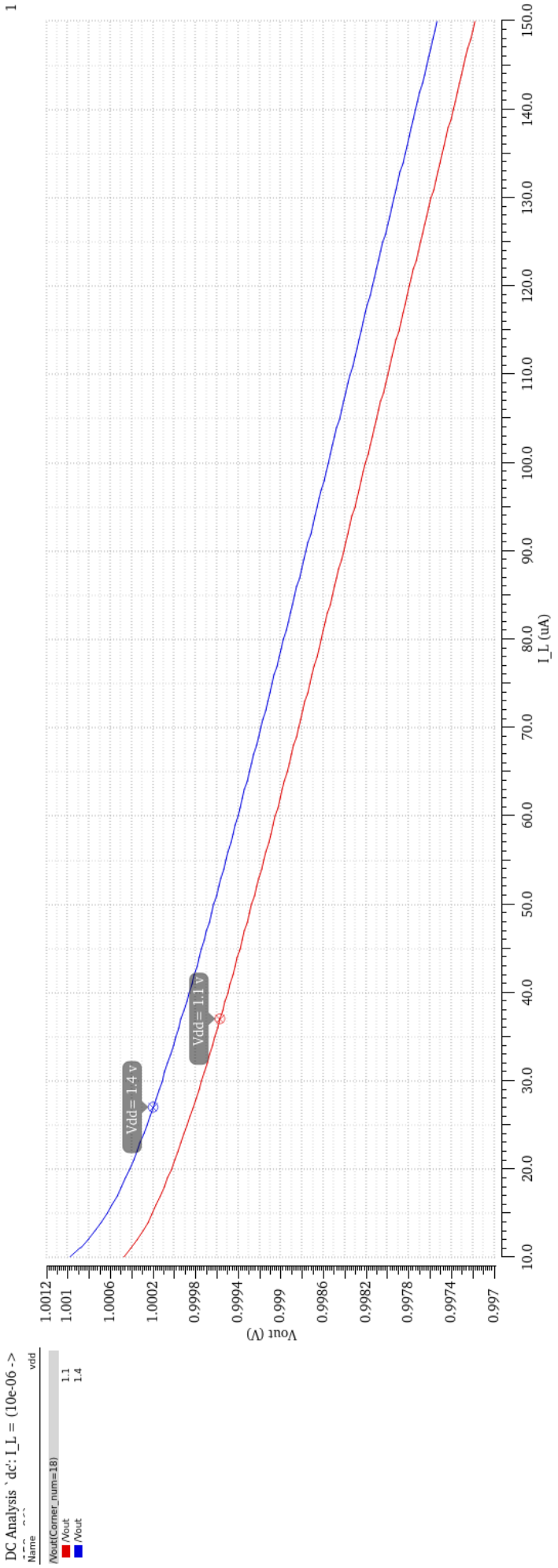
6. $\{V_{dd}, tt, 100℃\}$:


DC Analysis `dc': I_L = (10e-06 ->
Name
vdd
/VoutI(Corner_num=18)
/Vout
/Vout
1.1
1.4
Vout (V)
I_L (uA)
Vdd = 1.4 v
Vdd = 1.1 v
1.0016
1.0014
1.001
1.0006
1.0002
0.9998
0.9994
0.999
0.9986
0.9982
0.9978
0.9974
0.997
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0

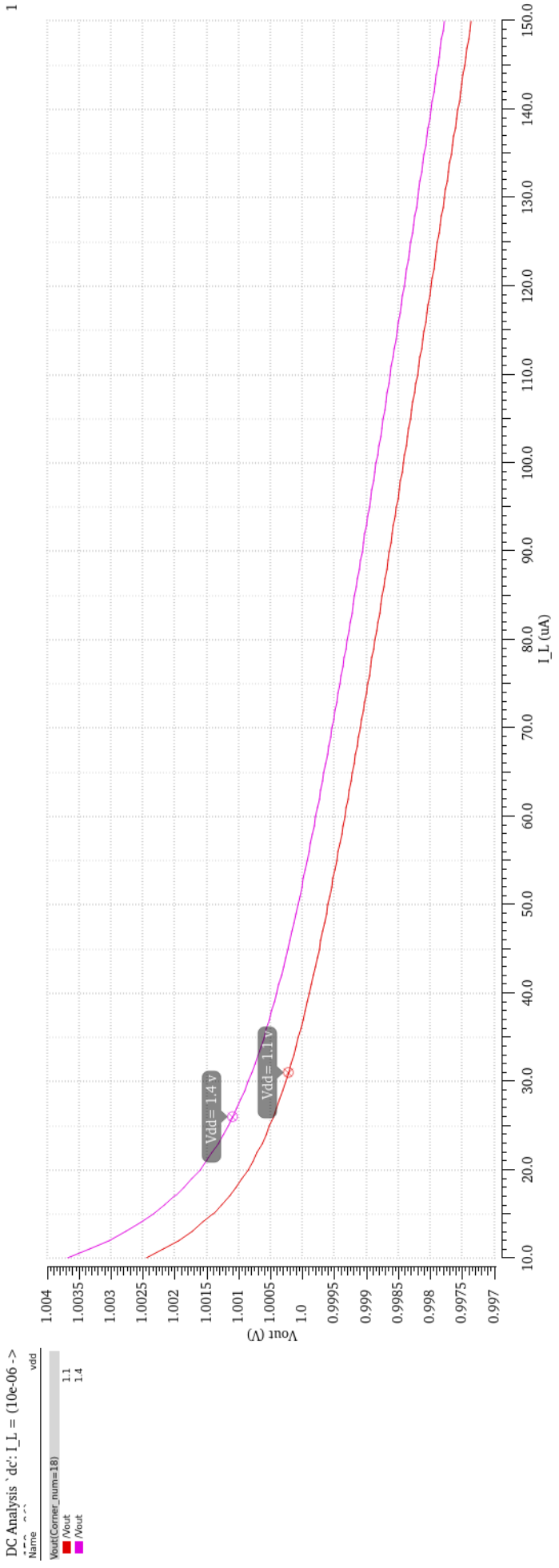
7. $\{V_{dd}, ff, 0℃\}$**:**


DC Analysis `dc': I_L = (10e-06 ->
Name
vdd
/Mout(Corner_num=18)
/Mout
/Mout
1.1
1.4
Vout (V)
I_L (uA)
Vdd= 1.4 v
Vdd= 1.1 v

8. $\{V_{dd}, ff, 50℃\}$:

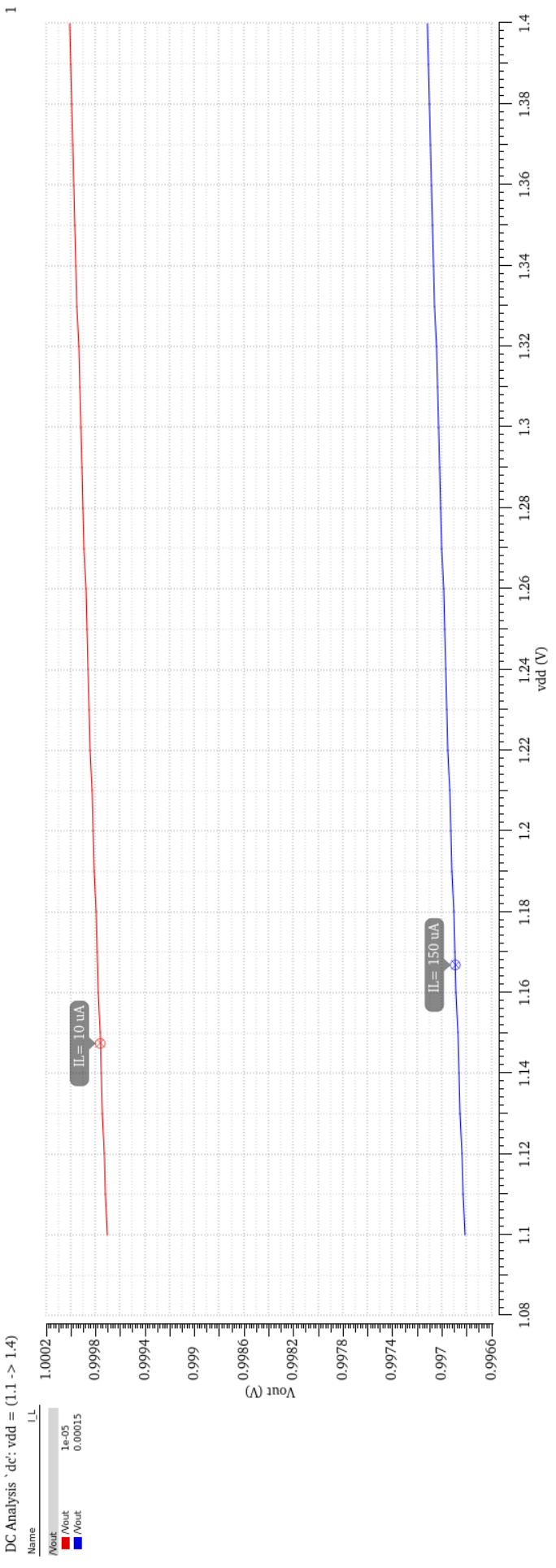

DC Analysis `dc': I_L = (10e-06 ->
Name
vdd
/Vout(Corner_num=18)
/Vout
/Vout
1.1
1.4
Vdd = 1.4 v
Vdd = 1.1 v
Vout (V)
I_L (uA)
1.0012
1.001
1.0006
1.0002
0.9998
0.9994
0.999
0.9986
0.9982
0.9978
0.9974
0.997
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0

9. $\{V_{dd}, ff, 100℃\}$**:**

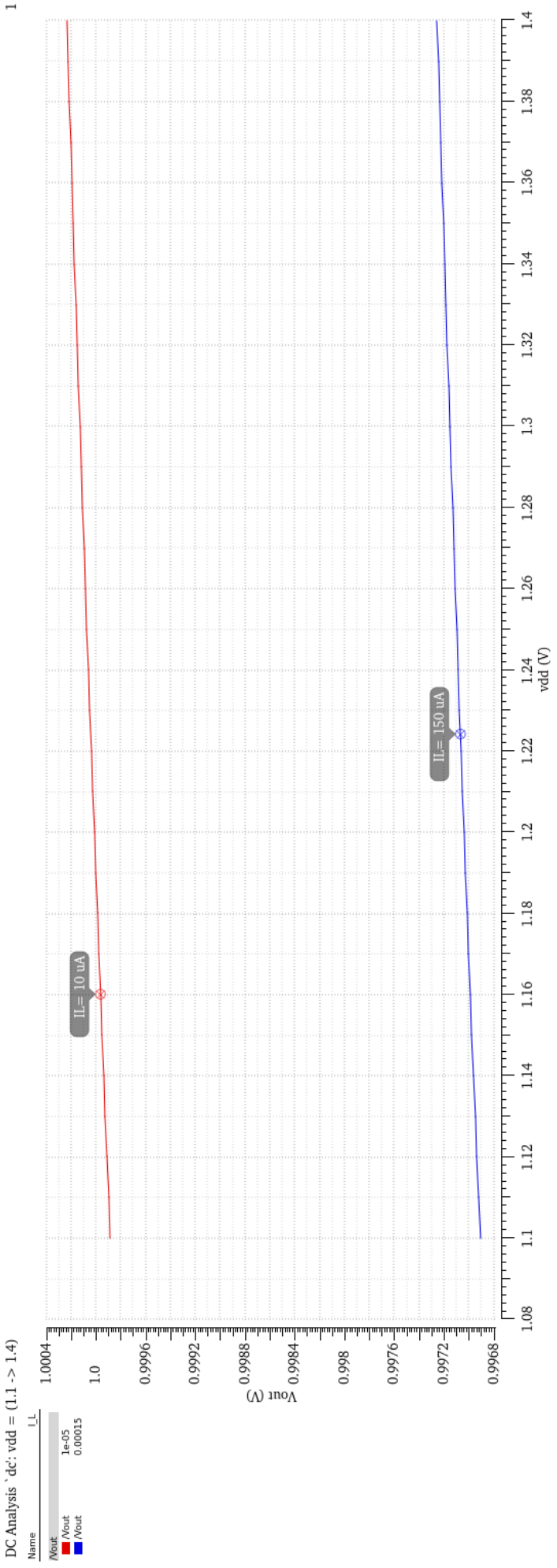

1
DC Analysis `dc': I_L = (10e-06 ->
Name
vdd
Vout(Corner_num=18)
1.1
/Vout
1.4
/Vout
Vout (V)
1.004
1.0035
1.003
1.0025
1.002
1.0015
1.001
1.0005
1.0
0.9995
0.999
0.9985
0.998
0.9975
0.997
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0
I_L (uA)
Vdd= 1.4 v
Vdd= 1.1 v

V_{out} vs V_{DD} :

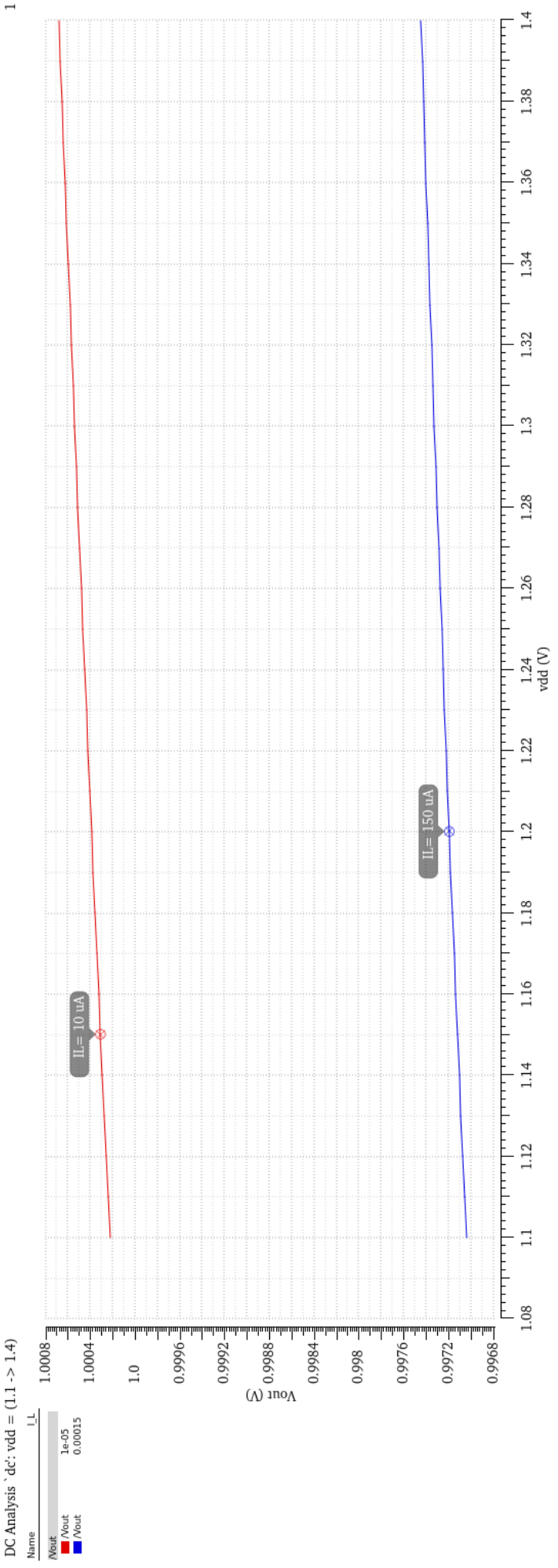
1. $\{V_{dd}, ss, 0℃\}$:



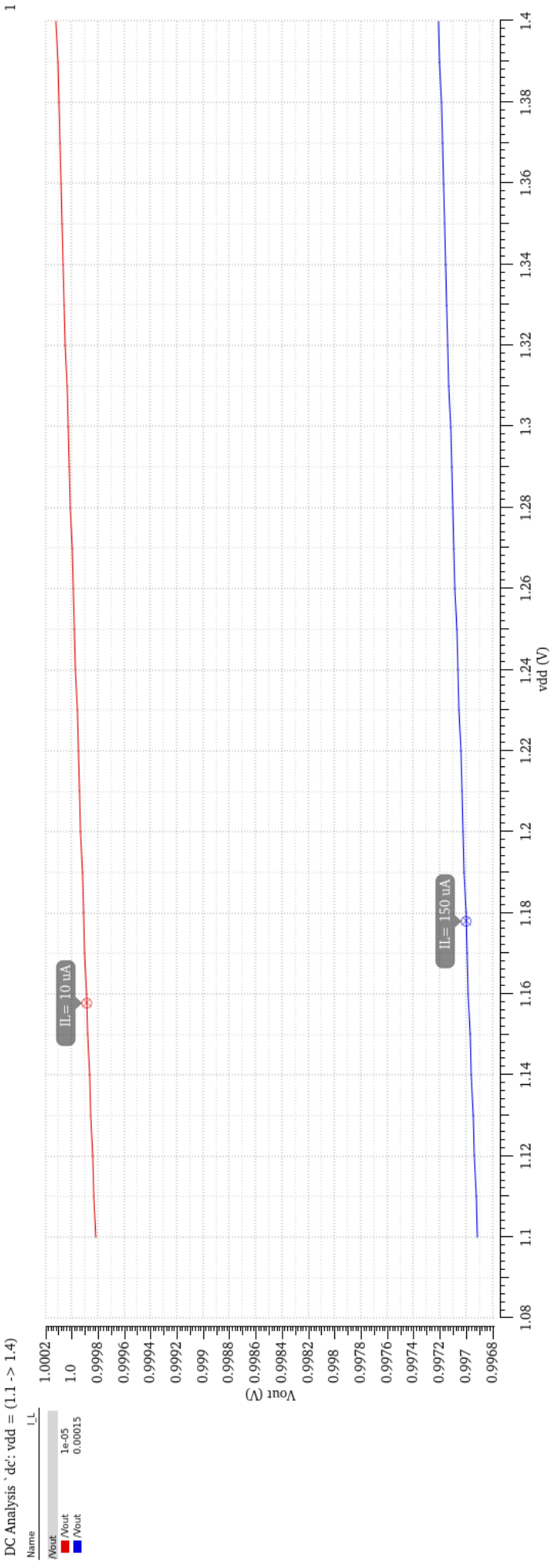
2. $\{V_{dd}, ss, 50℃\}$:


DC Analysis `dc': vdd = (1.1 -> 1.4)
Name
/Vout
/Vout
/Vout
1e-05
0.00015
IL= 10 uA
IL= 150 uA
Vout (V)
vdd (V)
1.0004
1.0
0.9996
0.9992
0.9988
0.9984
0.998
0.9976
0.9972
0.9968
1.08
1.1
1.12
1.14
1.16
1.18
1.2
1.22
1.24
1.26
1.28
1.3
1.32
1.34
1.36
1.38
1.4

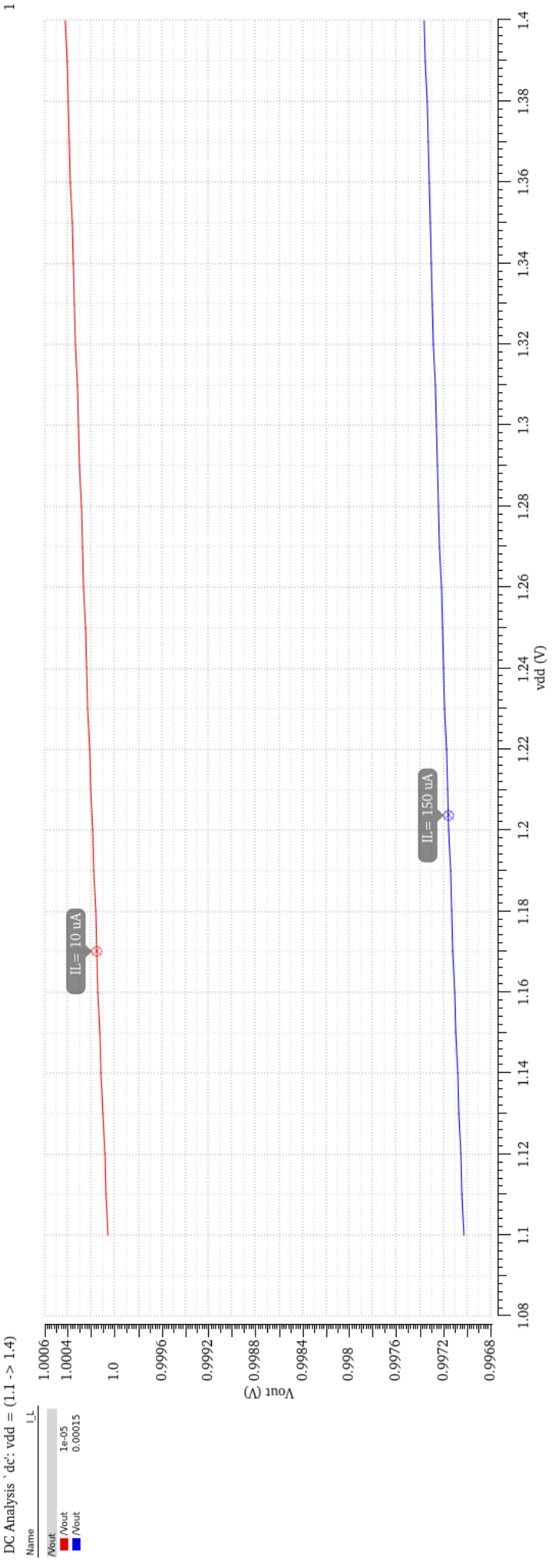
3. $\{V_{dd}, ss, 100℃\}$:


DC Analysis `dc': vdd = (1.1 -> 1.4)
Name
/Vout
/Vout
/Vout
1e-05
0.00015
IL= 10 uA
IL= 150 uA
Vout (V)
vdd (V)
1.0008
1.0004
1.0
0.9996
0.9992
0.9988
0.9984
0.998
0.9976
0.9972
0.9968
1.08
1.1
1.12
1.14
1.16
1.18
1.2
1.22
1.24
1.26
1.28
1.3
1.32
1.34
1.36
1.38
1.4

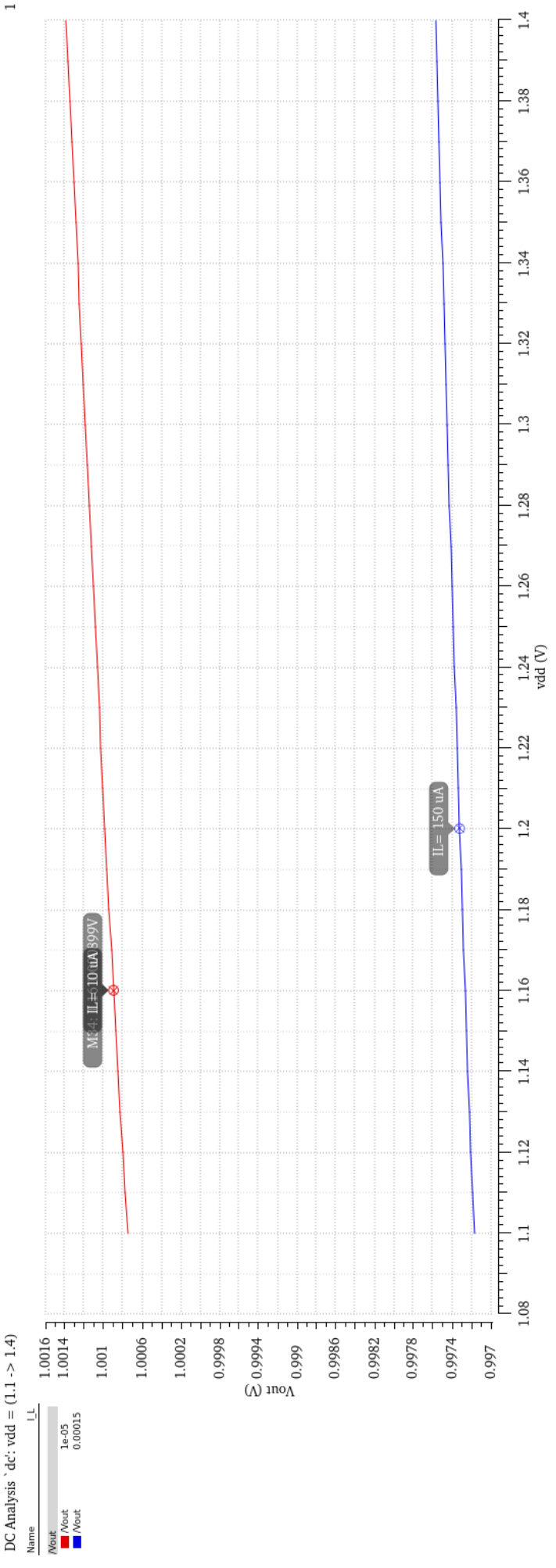
4. $\{V_{dd}, tt, 0℃\}$:


DC Analysis `dc': vdd = (1.1 -> 1.4)
Name
I_L
/Vout
/Vout
/Vout
1e-05
0.00015
IL= 10 uA
IL= 150 uA
Vout (V)
vdd (V)
1.0002
1.0
0.9998
0.9996
0.9994
0.9992
0.999
0.9988
0.9986
0.9984
0.9982
0.998
0.9978
0.9976
0.9974
0.9972
0.997
0.9968
1.08
1.1
1.12
1.14
1.16
1.18
1.2
1.22
1.24
1.26
1.28
1.3
1.32
1.34
1.36
1.38
1.4

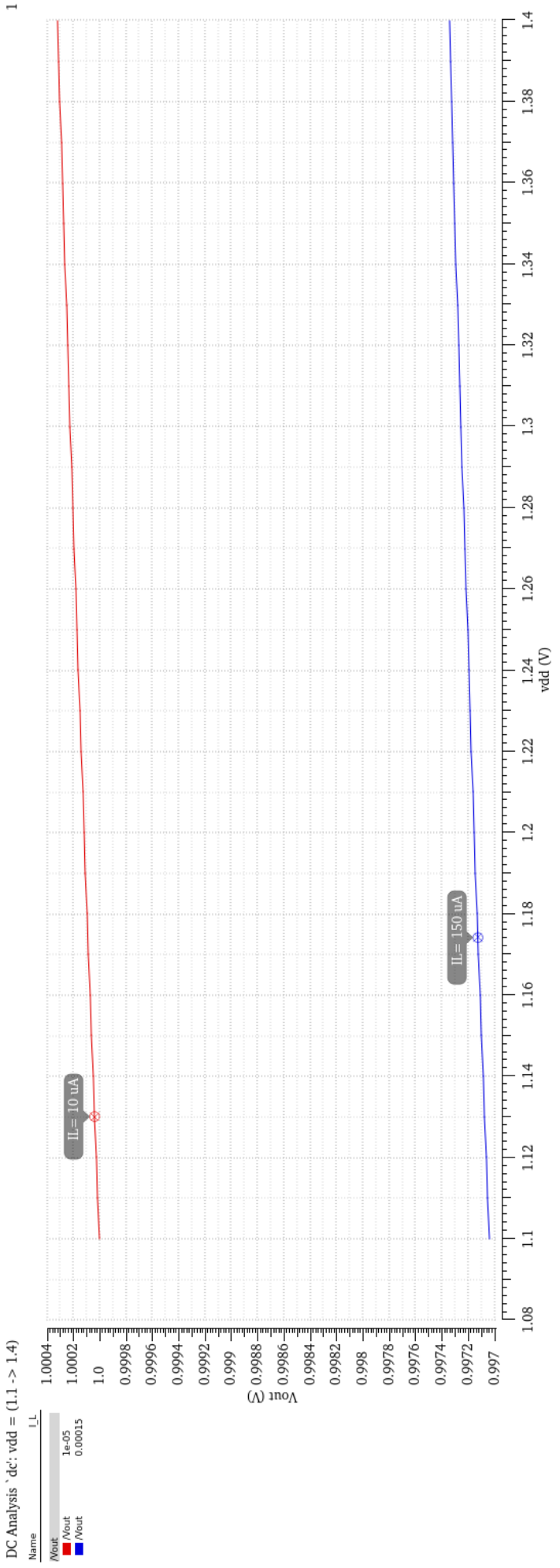
5. $\{V_{dd}, tt, 50℃\}$:


DC Analysis `dc': vdd = (1.1 -> 1.4)
Name
I_L
/Vout
/Vout
/Vout
1e-05
0.00015
Vout (V)
vdd (V)
IL = 10 uA
IL = 150 uA

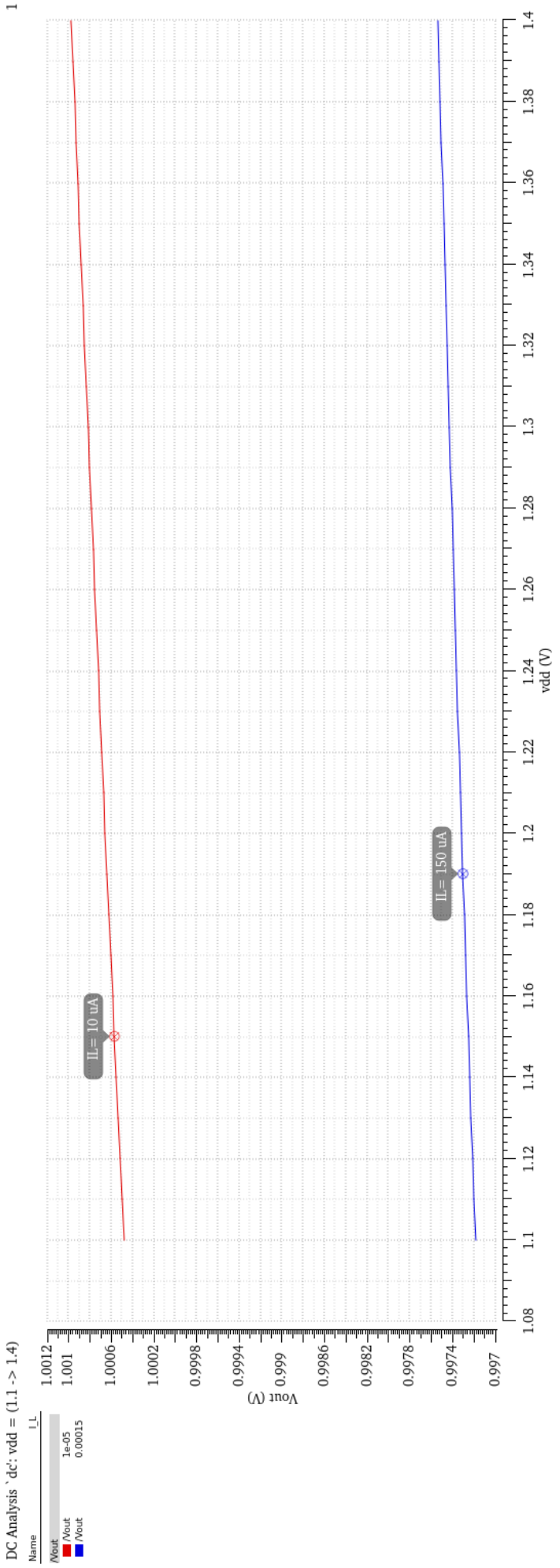
6. $\{V_{dd}, tt, 100℃\}$:


DC Analysis `dc': vdd = (1.1 -> 1.4)
Name
/Vout
/Vout
/Vout
1e-05
0.00015
Vout (V)
1.0016
1.0014
1.001
1.0006
1.0002
0.9998
0.9994
0.999
0.9986
0.9982
0.9978
0.9974
0.997
vdd (V)
1.08
1.1
1.12
1.14
1.16
1.18
1.2
1.22
1.24
1.26
1.28
1.3
1.32
1.34
1.36
1.38
1.4
IL= 150 uA

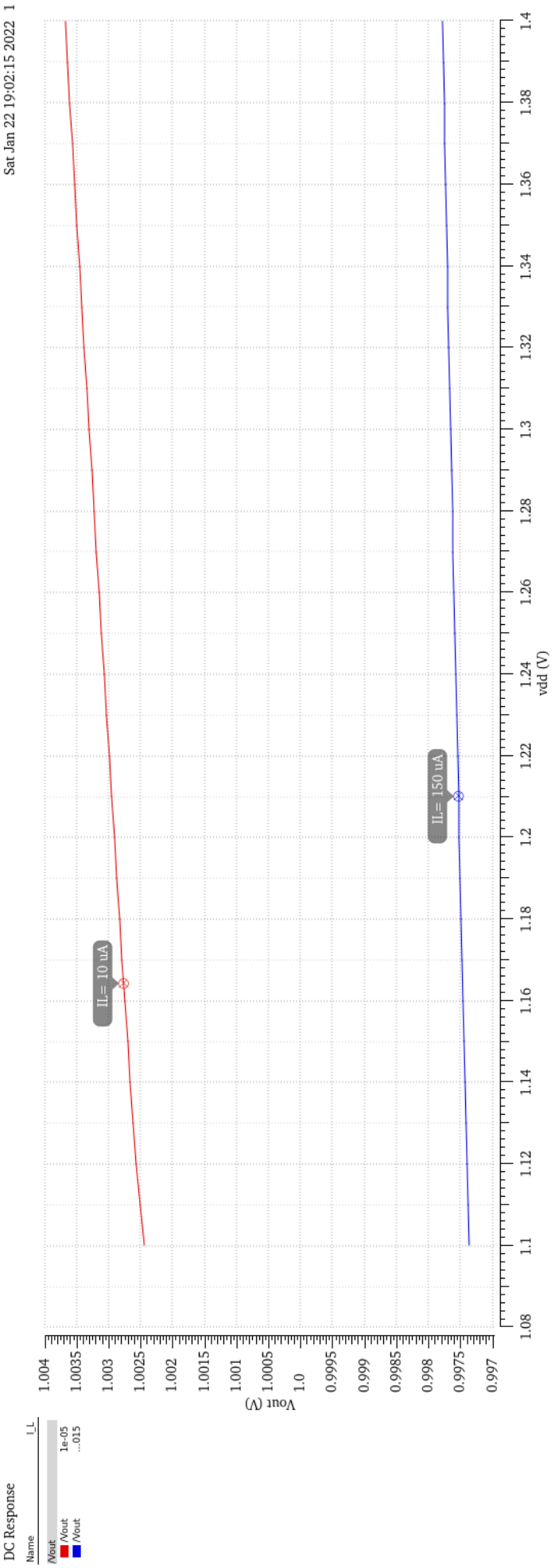
7. $\{V_{dd}, ff, 0℃\}$:


DC Analysis `dc': vdd = (1.1 -> 1.4)
Name
I_L
/Vout
/Vout
/Vout
1e-05
0.00015
IL= 10 uA
IL= 150 uA
Vout (V)
vdd (V)
1.0004
1.0002
1.0
0.9998
0.9996
0.9994
0.9992
0.999
0.9988
0.9986
0.9984
0.9982
0.998
0.9978
0.9976
0.9974
0.9972
0.997
1.08
1.1
1.12
1.14
1.16
1.18
1.2
1.22
1.24
1.26
1.28
1.3
1.32
1.34
1.36
1.38
1.4

8. $\{V_{dd}, ff, 50℃\}$:


DC Analysis `dc': vdd = (1.1 -> 1.4)
Name
I_L
/Vout
/Vout
/Vout
1e-05
0.00015
IL= 10 uA
IL= 150 uA
Vout (V)
vdd (V)
1.0012
1.001
1.0006
1.0002
0.9998
0.9994
0.999
0.9986
0.9982
0.9978
0.9974
0.997
1.08
1.1
1.12
1.14
1.16
1.18
1.2
1.22
1.24
1.26
1.28
1.3
1.32
1.34
1.36
1.38
1.4

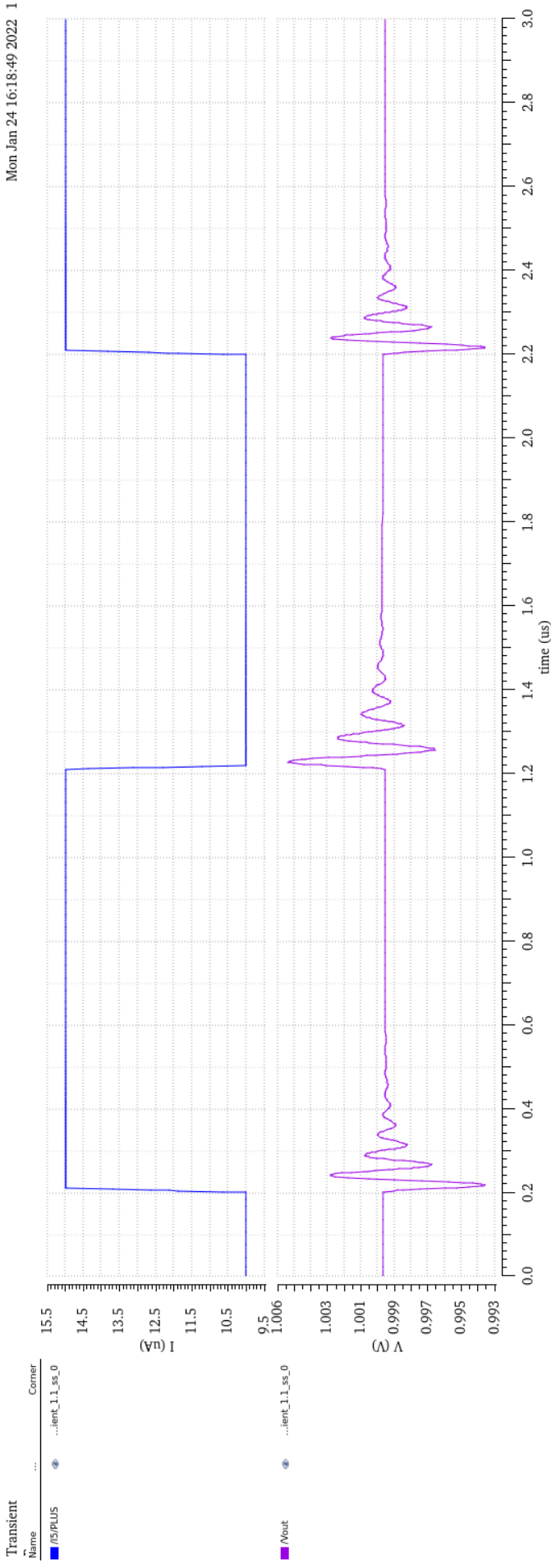
9. $\{V_{dd}, ff, 100℃\}$:


Sat Jan 22 19:02:15 2022 1
IL= 10 uA
IL= 150 uA
Vout (V)
vdd (V)
1.004
1.0035
1.003
1.0025
1.002
1.0015
1.001
1.0005
1.0
0.9995
0.999
0.9985
0.998
0.9975
0.997
1.08
1.1
1.12
1.14
1.16
1.18
1.2
1.22
1.24
1.26
1.28
1.3
1.32
1.34
1.36
1.38
1.4
DC Response
Name
/Vout
/Vout
/Vout
1e-05
...015

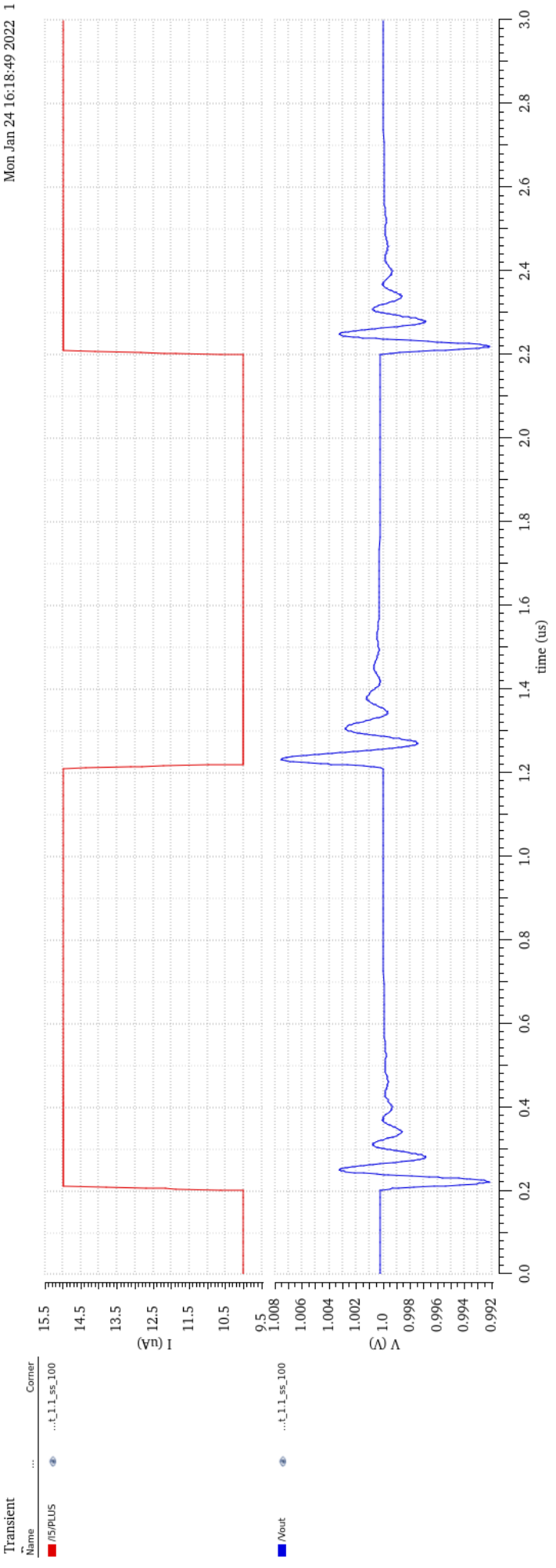
Transient Plots:

A. Current Step 10 uA – 15 uA:

1. $\{1.1\,v, ss, 0℃\}$:

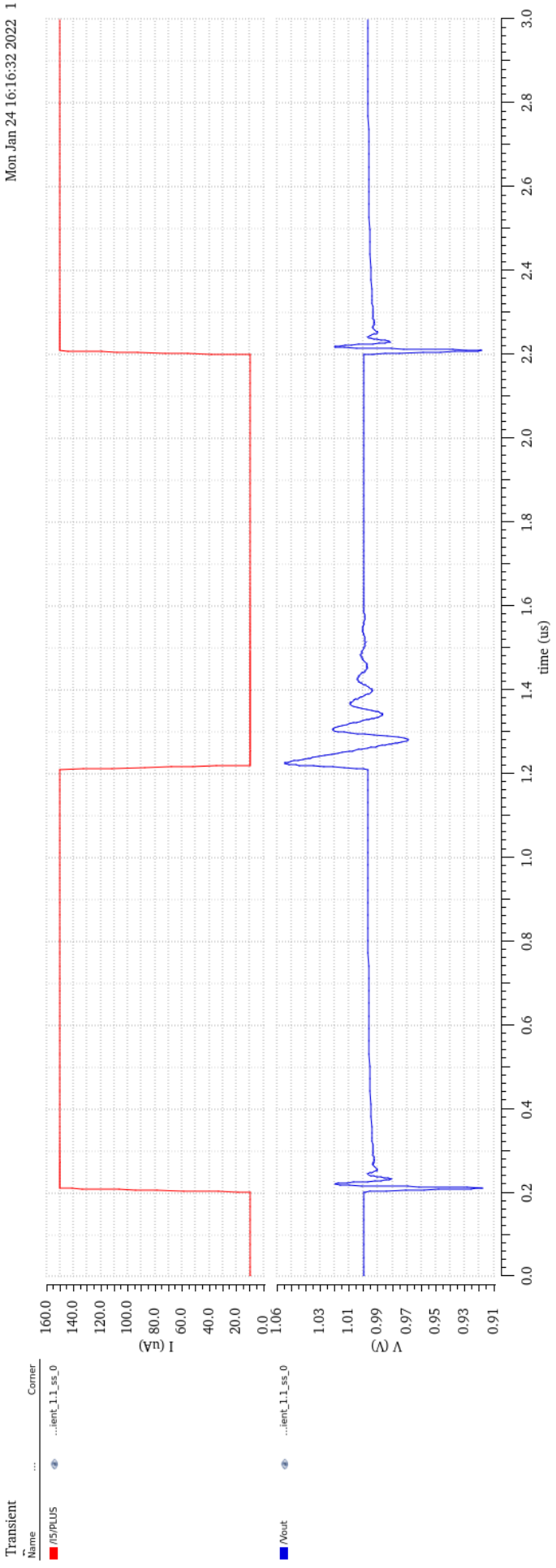


2. $\{1.1\,v, ss, 100℃\}$**:**

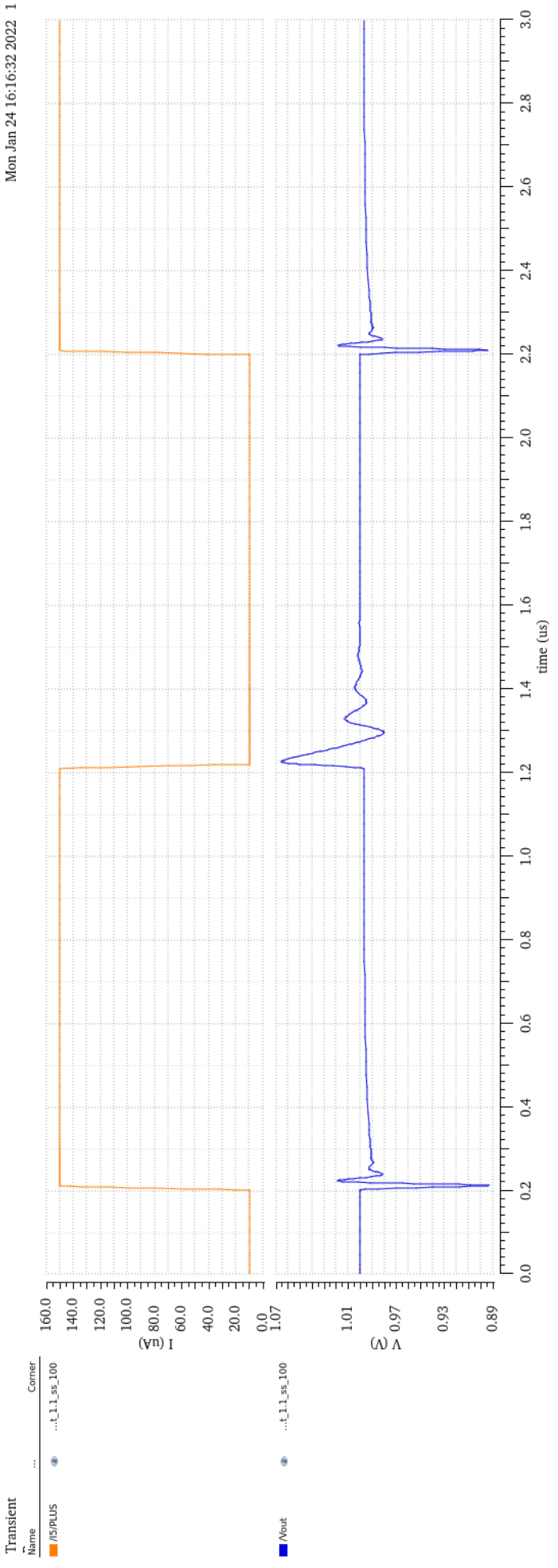

Mon Jan 24 16:18:49 2022 1
Transient
Name
Corner
/I5/PLUS
...t_1.1_ss_100
/Vout
...t_1.1_ss_100
I (uA)
V (V)
time (us)
15.5
14.5
13.5
12.5
11.5
10.5
9.5
1.008
1.006
1.004
1.002
1.0
0.998
0.996
0.994
0.992
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
2.2
2.4
2.6
2.8
3.0

B. Current Step 10 uA – 150 uA:

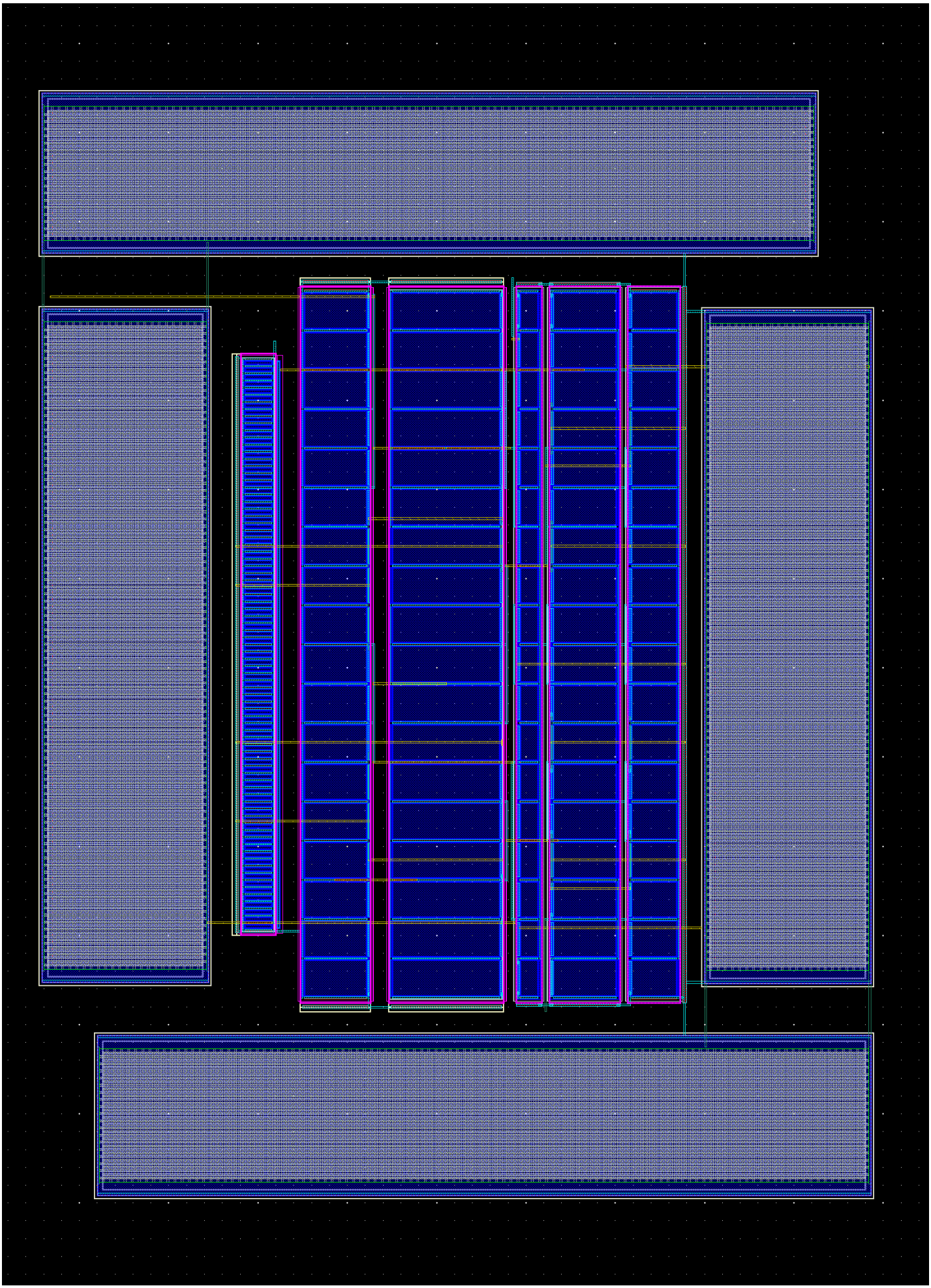
1. $\{1.1\,v, ss, 0℃\}$**:**



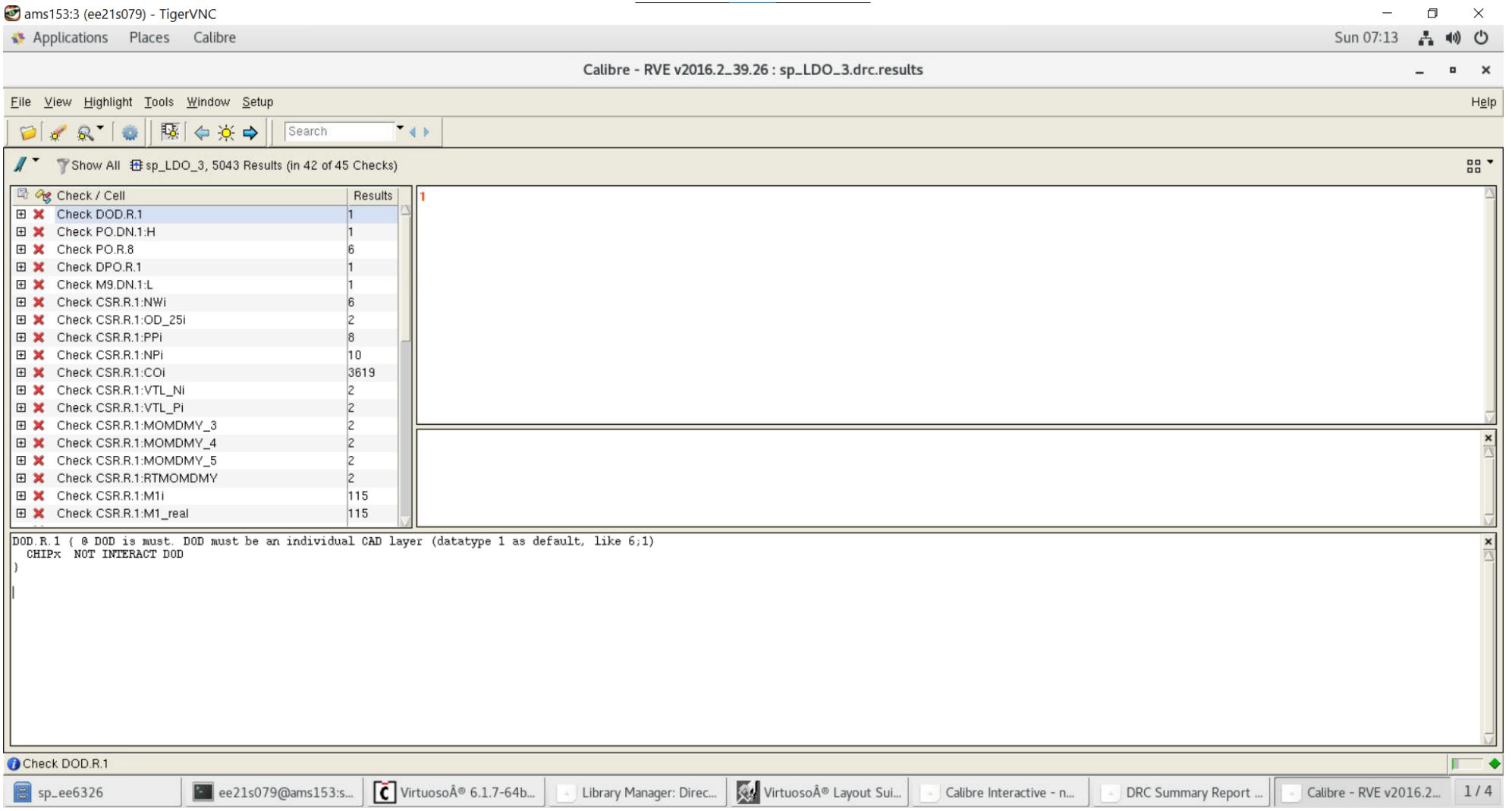
2. $\{1.1\,v, ss, 100℃\}$**:**


Mon Jan 24 16:16:32 2022 1
Transient
Name
Corner
/I5/PLUS
...t_1.1_ss_100
/Vout
...t_1.1_ss_100
I (uA)
V (V)
time (us)

Layout of LDO:



DRC:


ams153:3 (ee21s079) - TigerVNC
Applications Places Calibre
Sun 07:13
Calibre - RVE v2016.2_39.26 : sp_LDO_3.drc.results
File View Highlight Tools Window Setup
Help
Search
Show All
sp_LDO_3, 5043 Results (in 42 of 45 Checks)
Check / Cell
Results
Check DOD.R.1 1
Check PO.DN.1:H 1
Check PO.R.8 6
Check DPO.R.1 1
Check M9.DN.1:L 1
Check CSR.R.1:NWi 6
Check CSR.R.1:OD_25i 2
Check CSR.R.1:PPi 8
Check CSR.R.1:NPi 10
Check CSR.R.1:COi 3619
Check CSR.R.1:VTL_Ni 2
Check CSR.R.1:VTL_Pi 2
Check CSR.R.1:MOMDMY_3 2
Check CSR.R.1:MOMDMY_4 2
Check CSR.R.1:MOMDMY_5 2
Check CSR.R.1:RTMOMDMY 2
Check CSR.R.1:M1i 115
Check CSR.R.1:M1_real 115
1
DOD.R.1 { @ DOD is must. DOD must be an individual CAD layer (datatype 1 as default, like 6;1)
CHIPx NOT INTERACT DOD
}
Check DOD.R.1
sp_ee6326
ee21s079@ams153:s...
VirtuosoÂ® 6.1.7-64b...
Library Manager: Direc...
VirtuosoÂ® Layout Sui...
Calibre Interactive - n...
DRC Summary Report ...
Calibre - RVE v2016.2...
1 / 4

LVS:

Comparison Results ×

Layout Cell / Type	Source Cell	Nets	Instances	Ports
sp_LDO_3	sp_LDO_3	20L, 20S	41L, 41S	5L, 5S

Cell sp_LDO_3 Summary (Clean)

```
                  CELL COMPARISON RESULTS ( TOP LEVEL )



                       #      ###################      ¯   ¯
                      #       #                 #       |   |
                     #   #     #     CORRECT     #       |   |
                      # #      #                 #       \___/
                       #       ###################


  Warning:  Unbalanced smashed mosfets were matched.
  Warning:  Ambiguity points were found and resolved arbitrarily.

LAYOUT CELL NAME:         sp_LDO_3
SOURCE CELL NAME:         sp_LDO_3

------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
-------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              5         5

 Nets:              20        20
```

Table:

	Schematic				*RC Extracted Netlist*			
	IL= 10uA		**IL= 150uA**		**IL= 10uA**		**IL= 150uA**	
Corners	***Vout***	***I_OpAmp***	***Vout***	***I_OpAmp***	***Vout***	***I_OpAmp***	***Vout***	***I_OpAmp***
	(mV)	*(uA)*	*(mV)*	*(uA)*	*(mV)*	*(uA)*	*(mV)*	*(uA)*
{Vdd= 1.1v, ss, 0}	1.000276	6.006249	1.00001	6.00961	999.70792	6.05072	996.8155	6.0539
{Vdd= 1.1v, ss, 50}	1.0004	6.00887	1.000047	6.01326	999.88922	6.05	996.9092	6.05429
{Vdd= 1.1v, ss, 100}	1.000632	6.0106	1.000082	6.01887	1.0002209	6.04998	997.0357	6.05704
{Vdd= 1.1v, tt, 0}	1.000409	6.00785	1.000132	6.01164	999.8227	6.05262	996.9149	6.05621
{Vdd= 1.1v, tt, 50}	1.0006	6.00951	1.00019	6.01567	1.0000622	6.05148	997.0264	6.05691
{Vdd= 1.1v, tt, 100}	1.000892	6.00479	1.000247	6.02282	1.0007469	6.04774	997.1712	6.0613
{Vdd= 1.1v, ff, 0}	1.000605	6.00883	1.000271	6.01404	1.0000034	6.0538	997.0413	6.05858
{Vdd= 1.1v, ff, 50}	1.000919	6.00579	1.000357	6.01899	1.000478	6.04999	997.1848	6.060177
{Vdd= 1.1v, ff, 100}	1.00169	5.9767	1.000437	6.02953	1.00244	6.02952	997.3648	6.06822
{Vdd= 1.4v, ss, 0}	1.000581	6.015575	1.000367	6.01895	1.0000017	6.06	997.1206	6.0632
{Vdd= 1.4v, ss, 50}	1.000773	6.018429	1.000482	6.02317	1.0002365	6.0597	997.2575	6.06413
{Vdd= 1.4v, ss, 100}	1.00104	6.01995	1.000631	6.02984	1.0006815	6.0598	997.4468	6.0679
{Vdd= 1.4v, tt, 0}	1.000706	6.0167	1.000475	6.02059	1.0001189	6.06146	997.2093	6.0651
{Vdd= 1.4v, tt, 50}	1.000927	6.01809	1.000608	6.0251	1.0004225	6.0603	997.3625	6.06628
{Vdd= 1.4v, tt, 100}	1.001329	6.00852	1.000774	6.03316	1.001385	6.05359	997.5688	6.07158
{Vdd= 1.4v, ff, 0}	1.000927	6.01723	1.000627	6.02299	1.0003224	6.06239	997.3458	6.06745
{Vdd= 1.4v, ff, 50}	1.001336	6.01043	1.000792	6.02833	1.0009754	6.0563	997.535	6.06948
{Vdd= 1.4v, ff, 100}	1.00249	5.96594	1.00099	6.03965	1.003687	6.024221	997.7841	6.07841

Vout	**MAX**	**MIN**
Current Consumption	**MAX**	**MIN**

Monte Carlo at $\{1.2V, tt, 50℃\}$:

Mean: ***999.950 mV***

Standard Deviation: ***1.68298 mV***