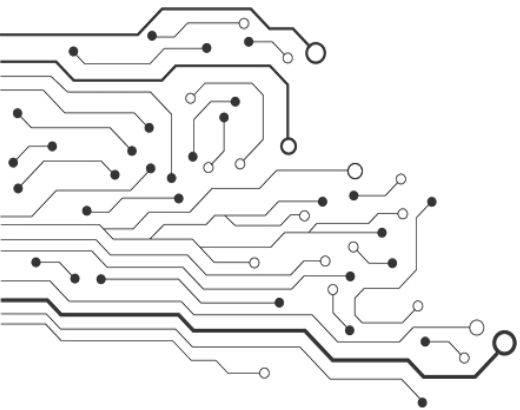
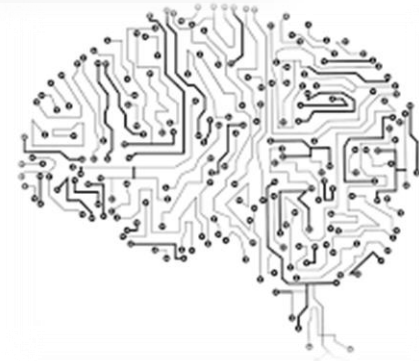


OrCAD - PCB Editor



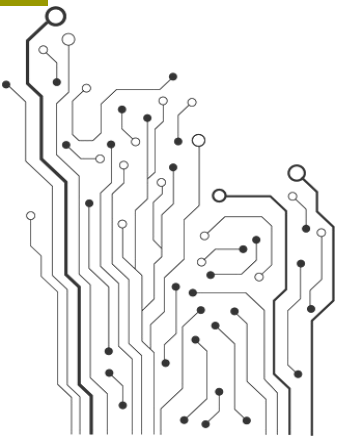
Dr. Sarwan Singh
NIELIT Chandigarh





Agenda

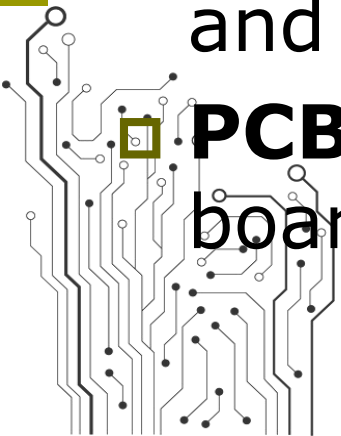
□ Gerber file

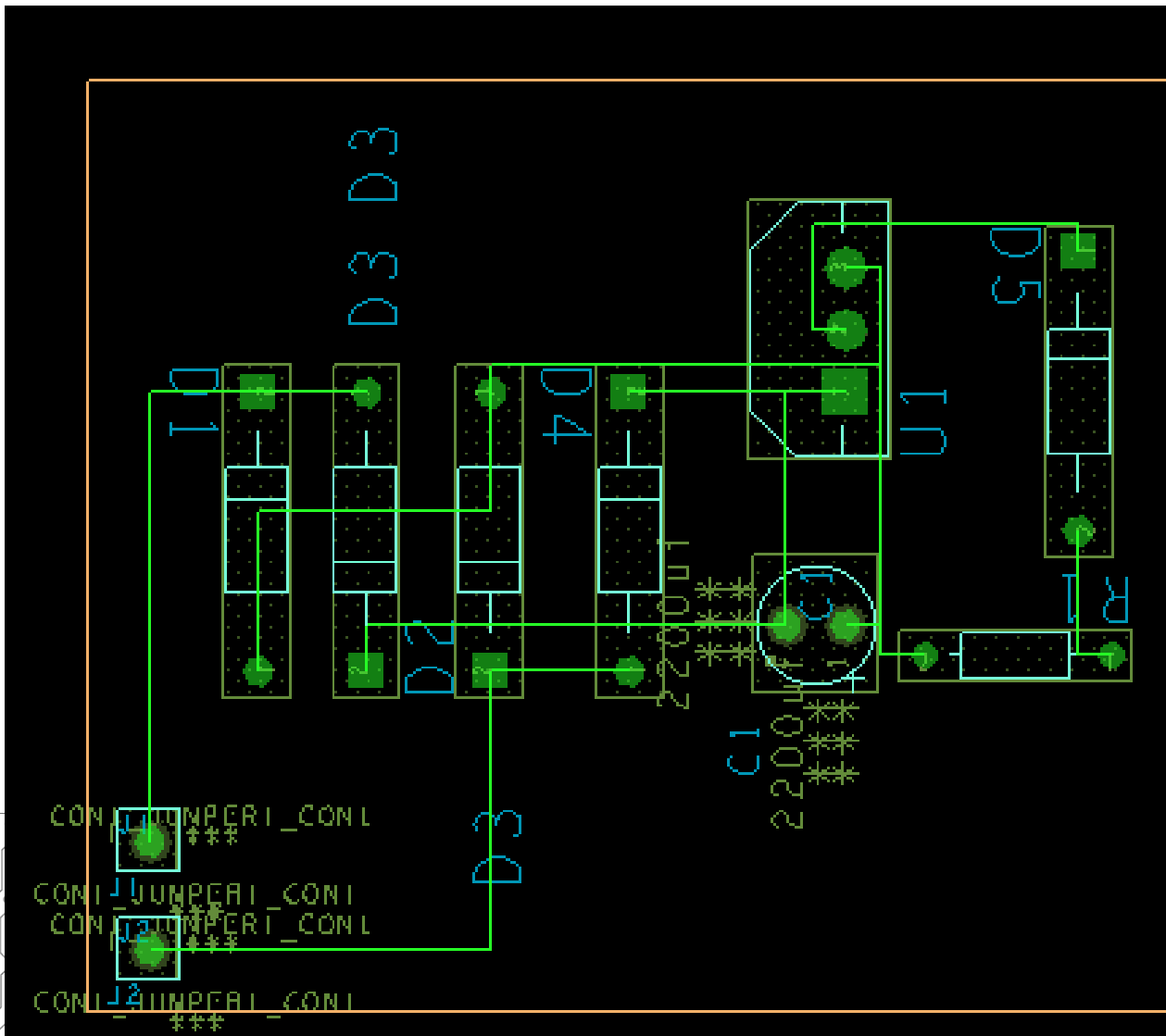




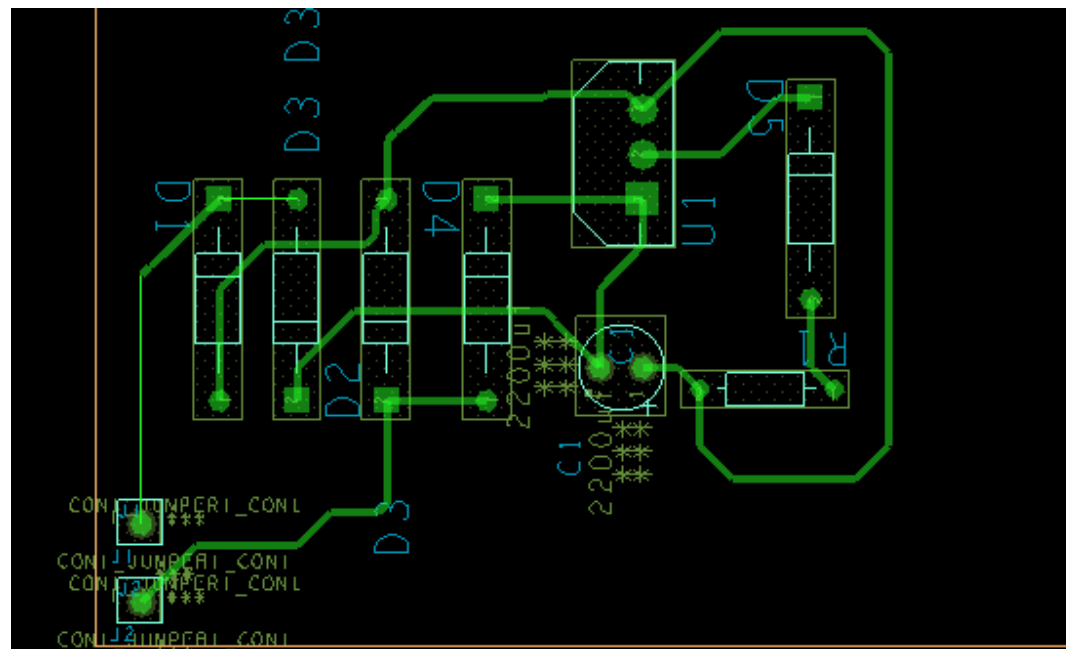
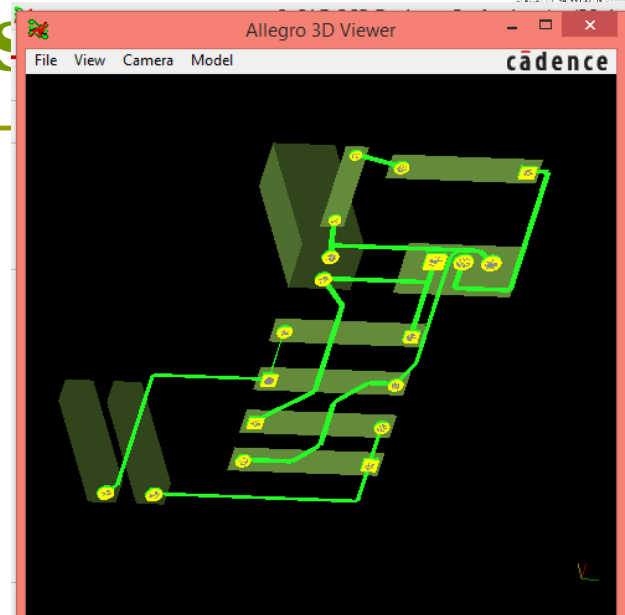
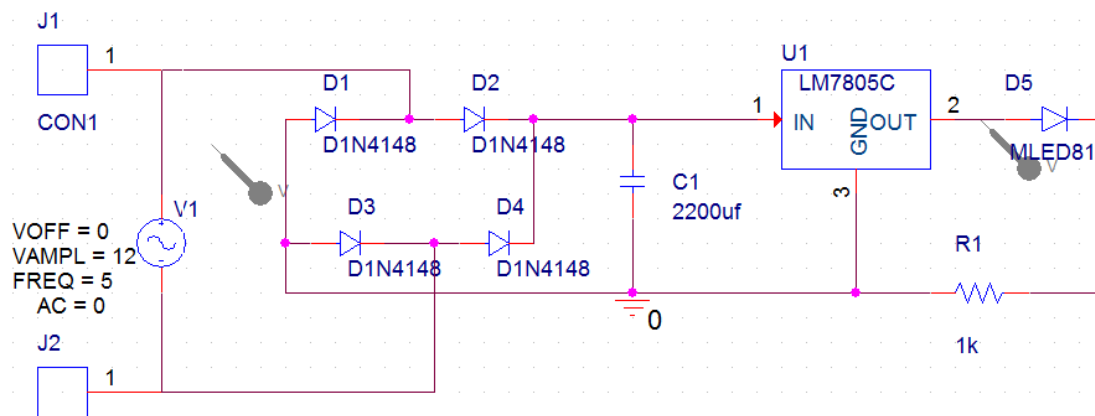
PSpice comprises three main applications

- ❑ **Capture** is used to draw a circuit on the screen, known formally as schematic capture. It offers great flexibility compared with a traditional pencil and paper drawing, as design changes can be incorporated and errors corrected quickly and easily
- ❑ **PSpice** simulates the captured circuit. You can analyse its behaviour in many ways and confirm that it performs as specified.
- ❑ **PCB Editor** is used to design printed circuit boards



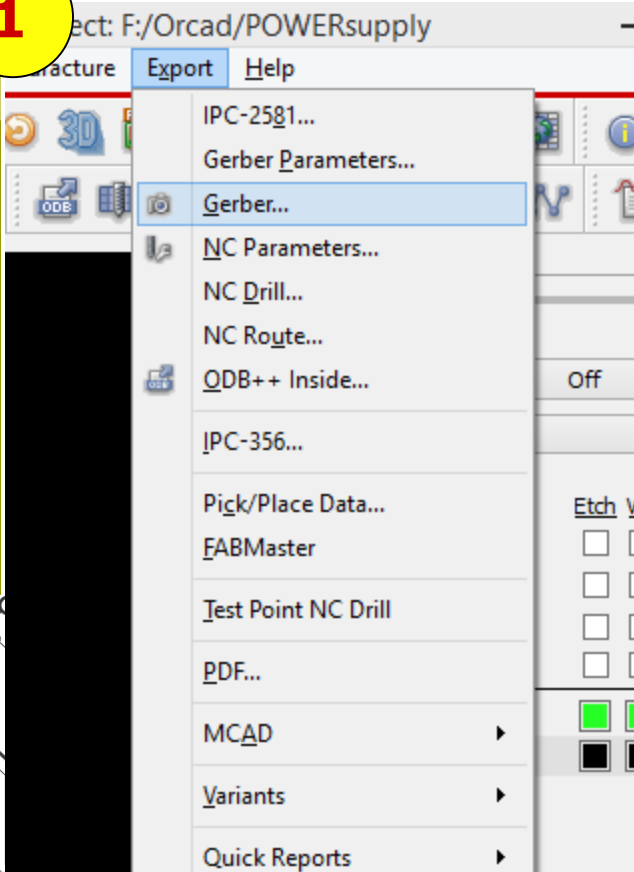


Adding jumper at Vin

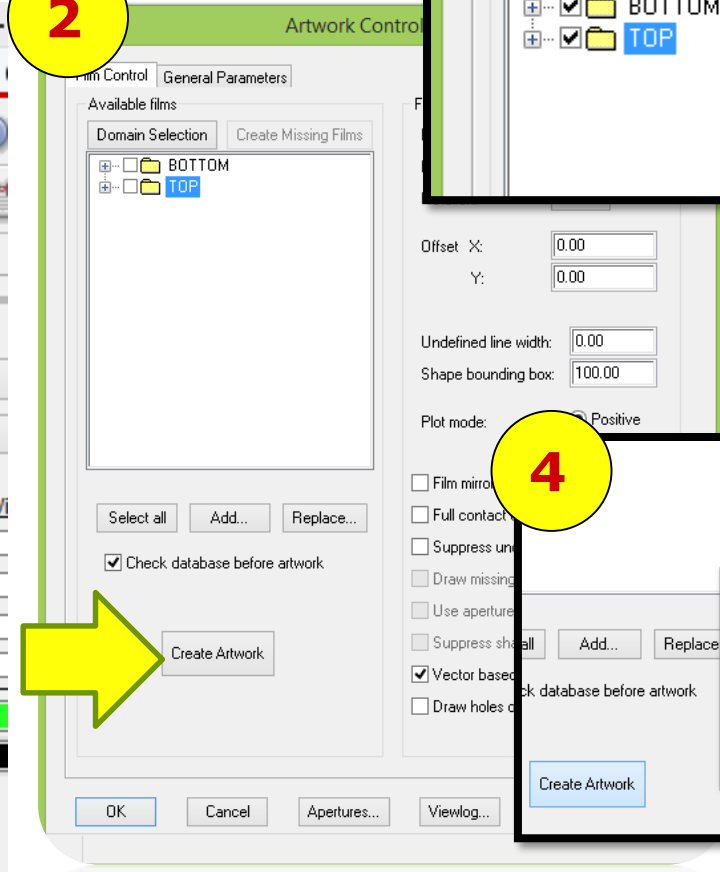


Exporting Gerber file

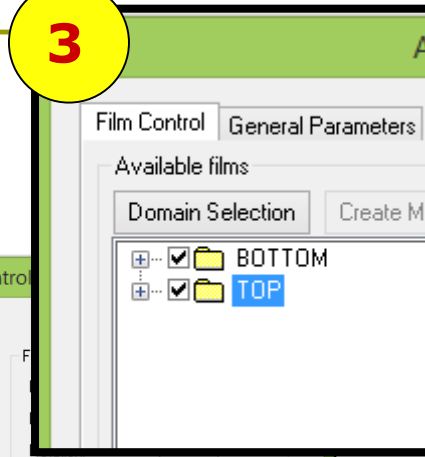
1



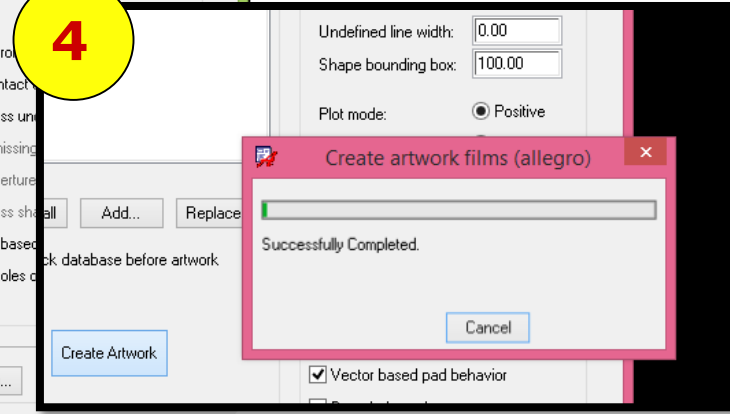
2



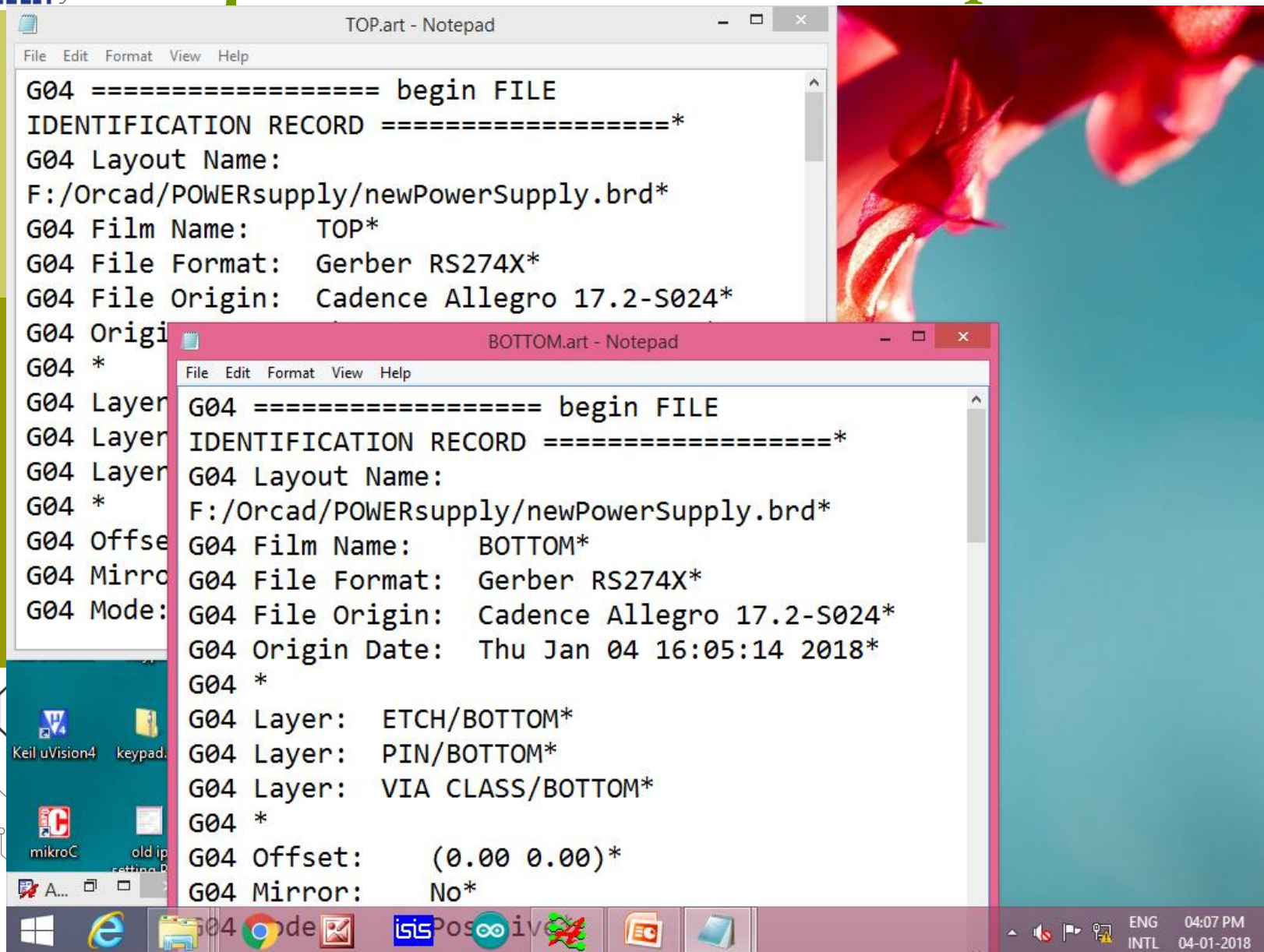
3



4



Output Gerber files — top.art, bottom.art



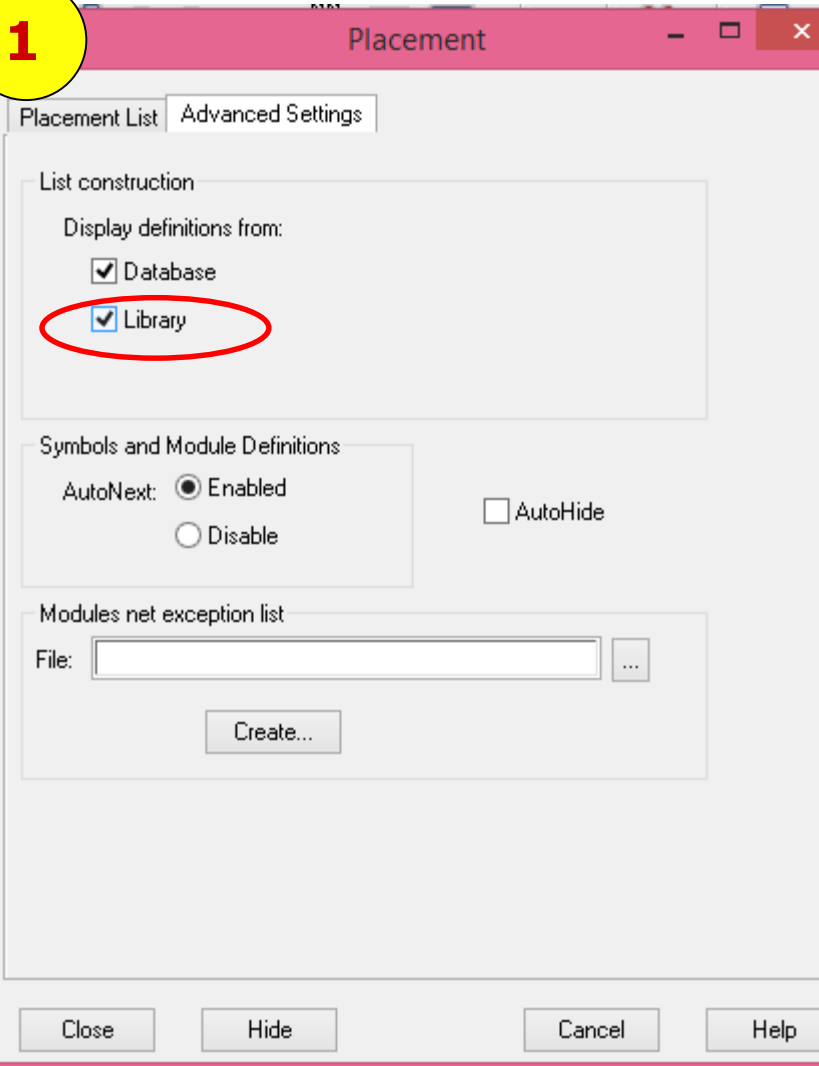
```
TOP.art - Notepad
File Edit Format View Help
G04 ===== begin FILE
IDENTIFICATION RECORD =====*
G04 Layout Name:
F:/Orcad/POWERsupply/newPowerSupply.brd*
G04 Film Name: TOP*
G04 File Format: Gerber RS274X*
G04 File Origin: Cadence Allegro 17.2-S024*
G04 Origin Date: Thu Jan 04 16:05:14 2018*
G04 *
G04 Layer: ETCH/TOP*
G04 Layer: PIN/TOP*
G04 Layer: VIA CLASS/TOP*
G04 *
G04 Offset: (0.00 0.00)*
G04 Mirror: No*

BOTTOM.art - Notepad
File Edit Format View Help
G04 ===== begin FILE
IDENTIFICATION RECORD =====*
G04 Layout Name:
F:/Orcad/POWERsupply/newPowerSupply.brd*
G04 Film Name: BOTTOM*
G04 File Format: Gerber RS274X*
G04 File Origin: Cadence Allegro 17.2-S024*
G04 Origin Date: Thu Jan 04 16:05:14 2018*
G04 *
G04 Layer: ETCH/BOTTOM*
G04 Layer: PIN/BOTTOM*
G04 Layer: VIA CLASS/BOTTOM*
G04 *
G04 Offset: (0.00 0.00)*
G04 Mirror: No*
```

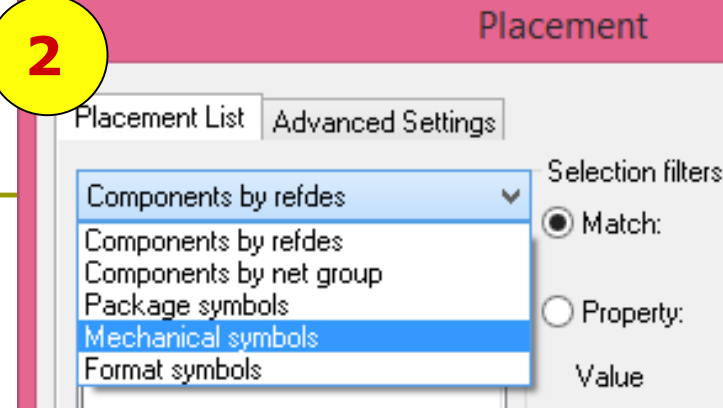
Mechanical symbols

Place > components manually

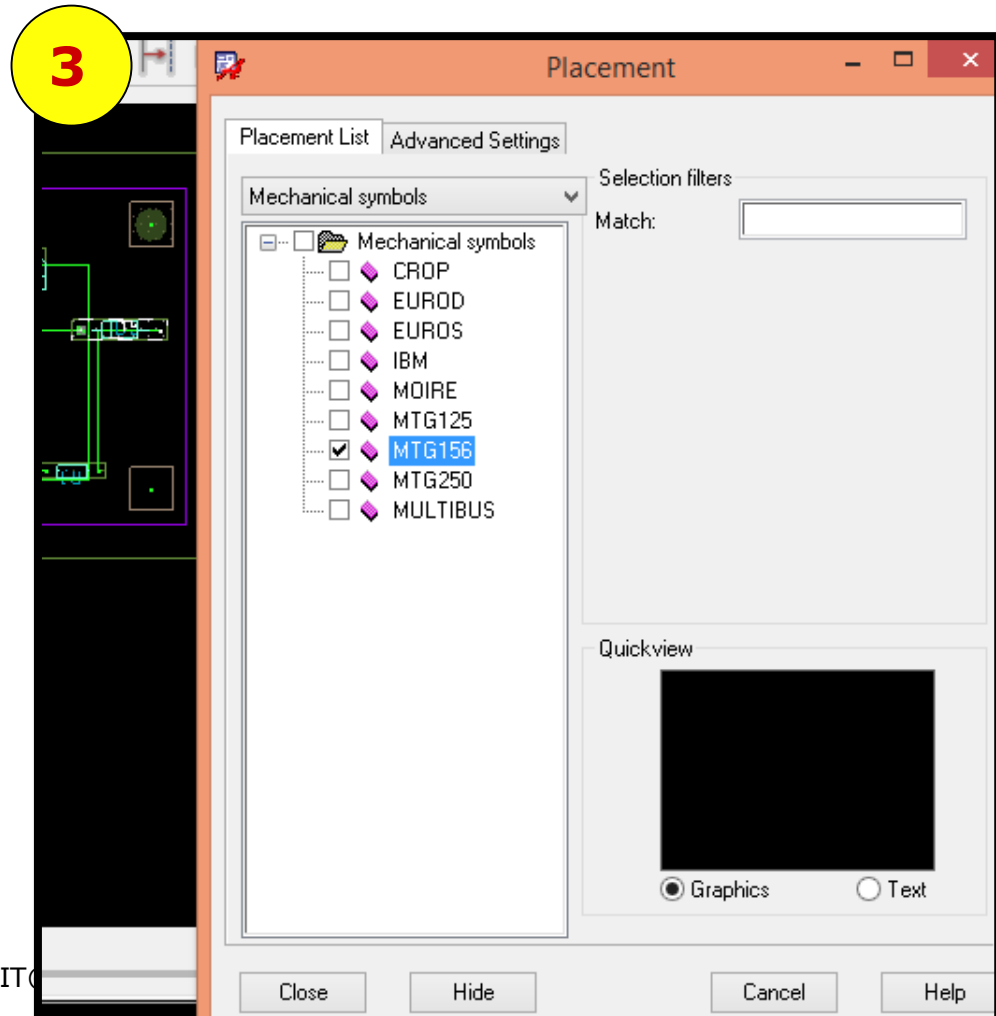
1



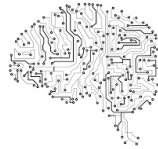
2



3

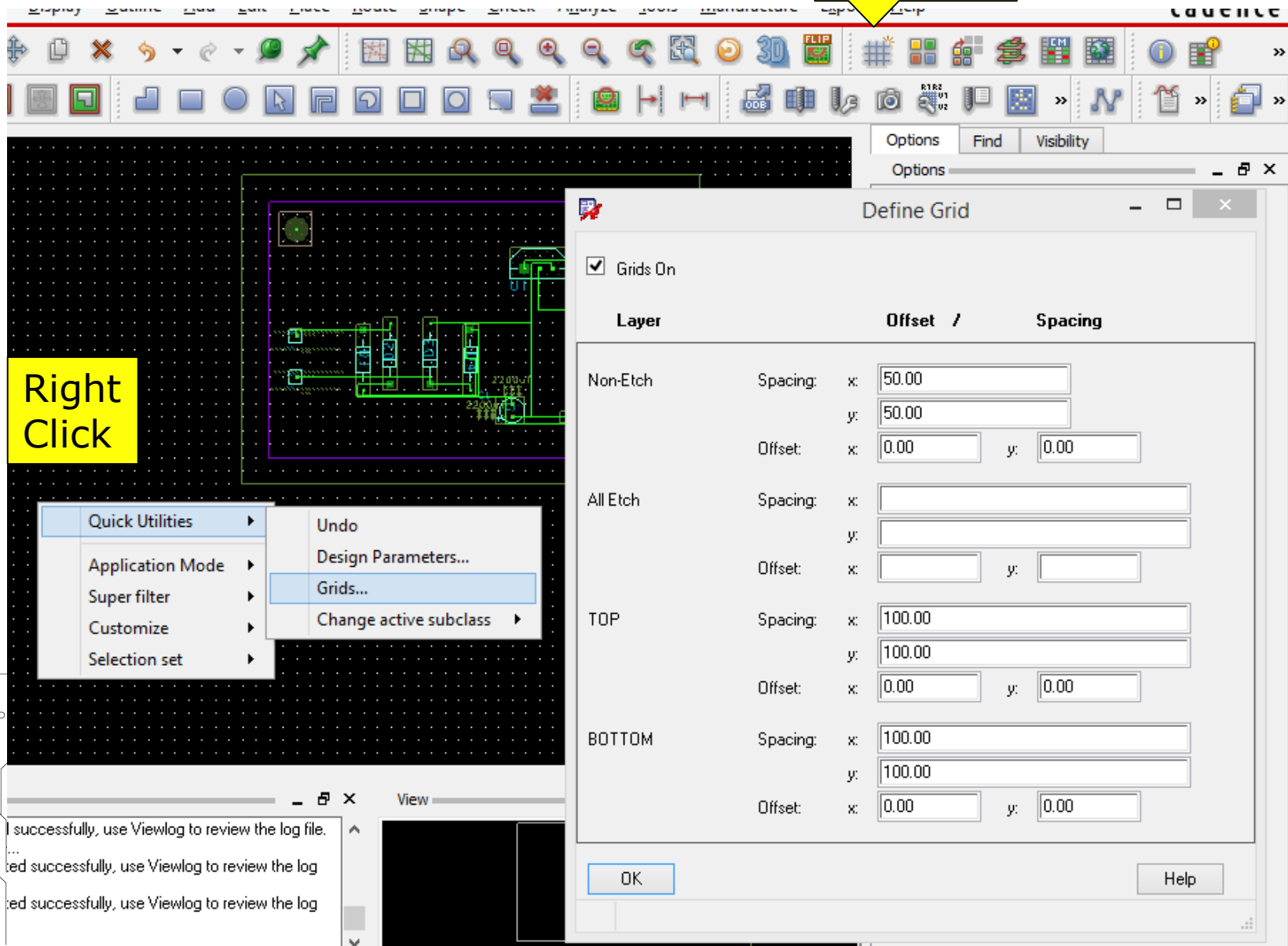


GridLines



Gridlines
Toggle

Right
Click



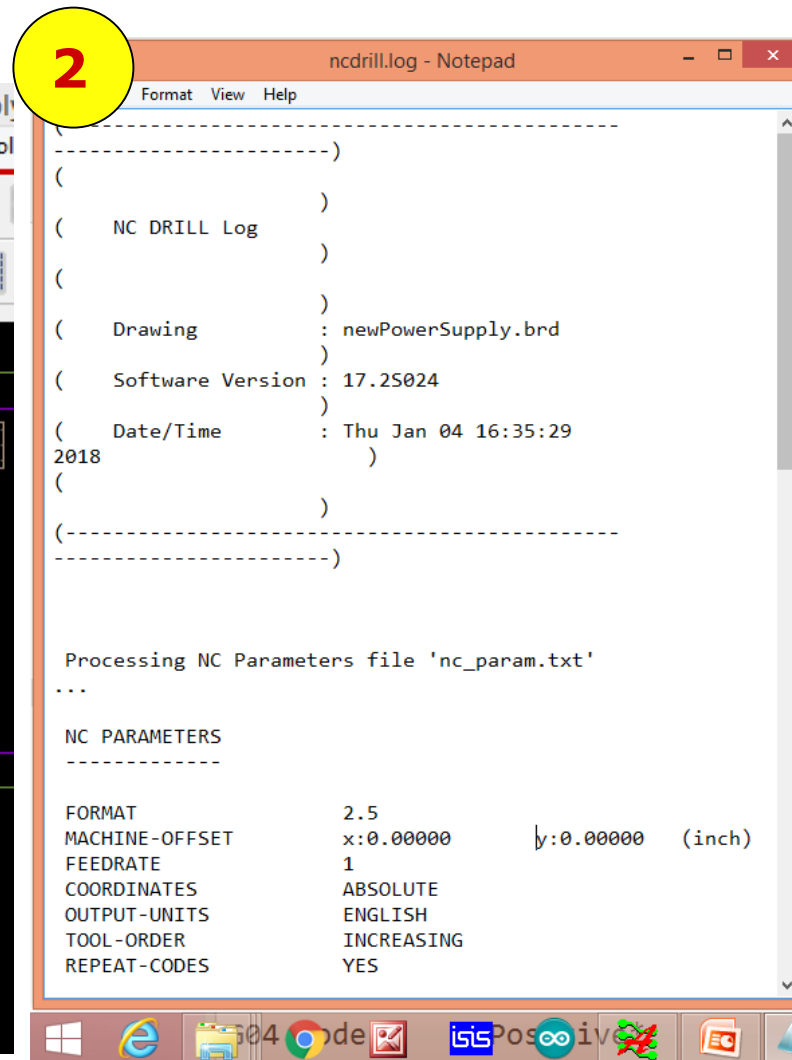
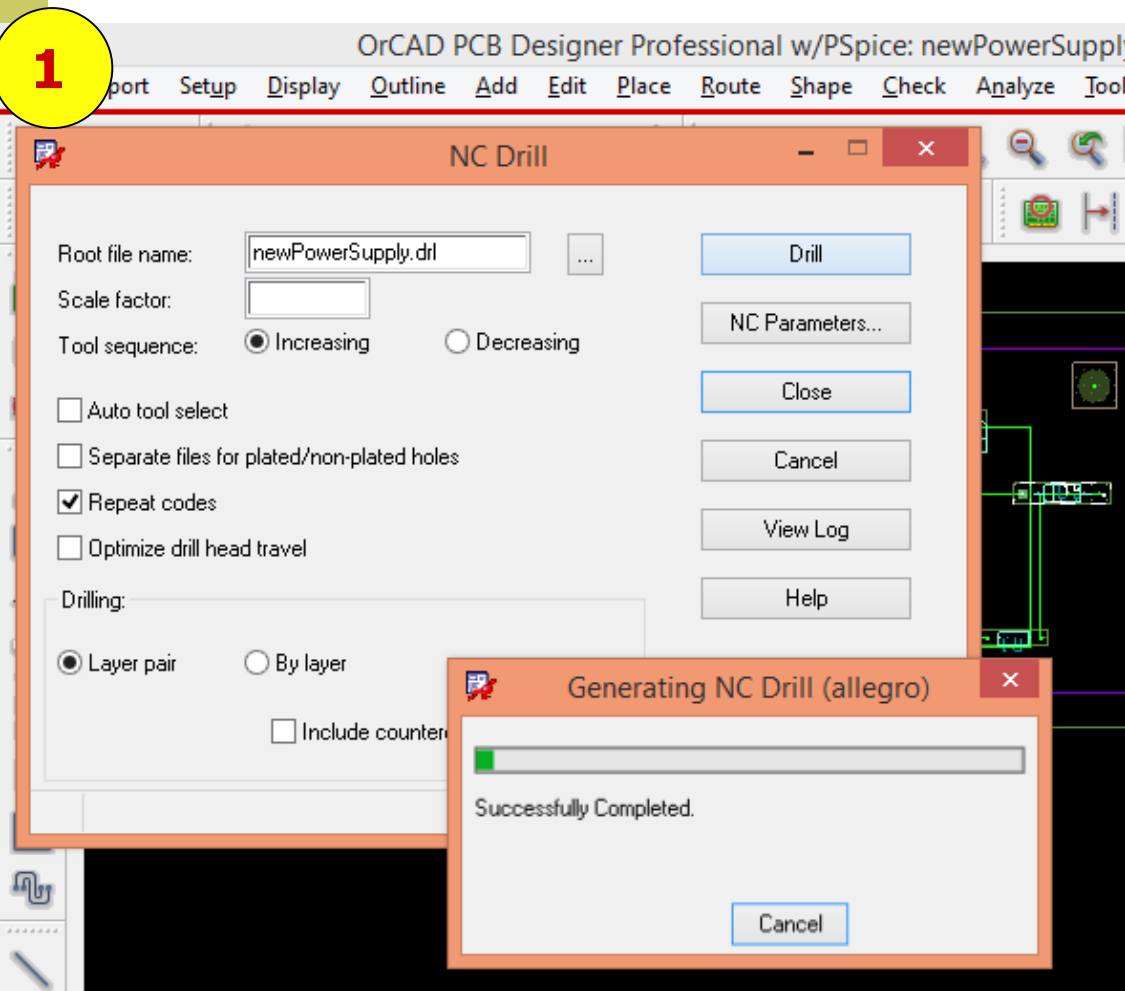
The screenshot shows a PCB design software interface. A right-click context menu is open over a grid area, with the 'Grids...' option highlighted. The 'Define Grid' dialog box is also open, showing the 'Grids On' checkbox checked. The dialog box contains a table with grid settings for different layers.

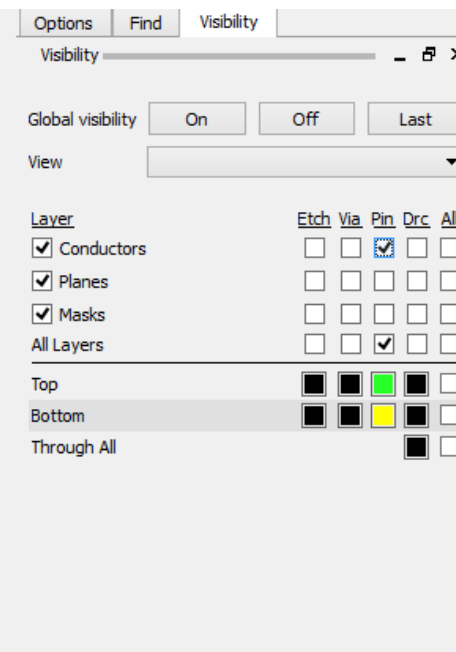
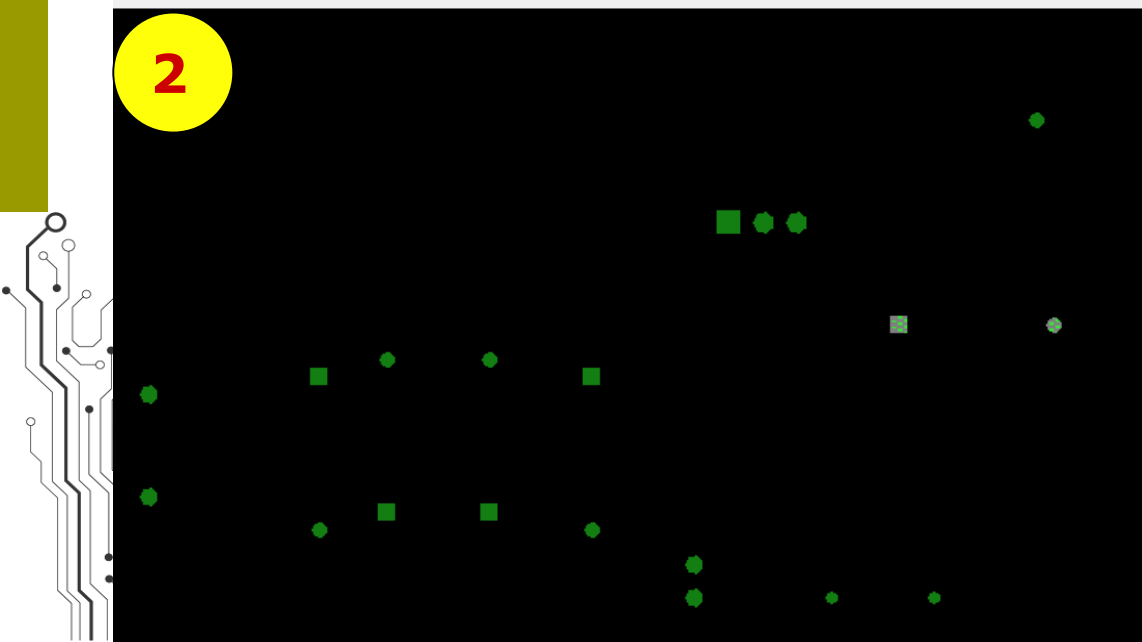
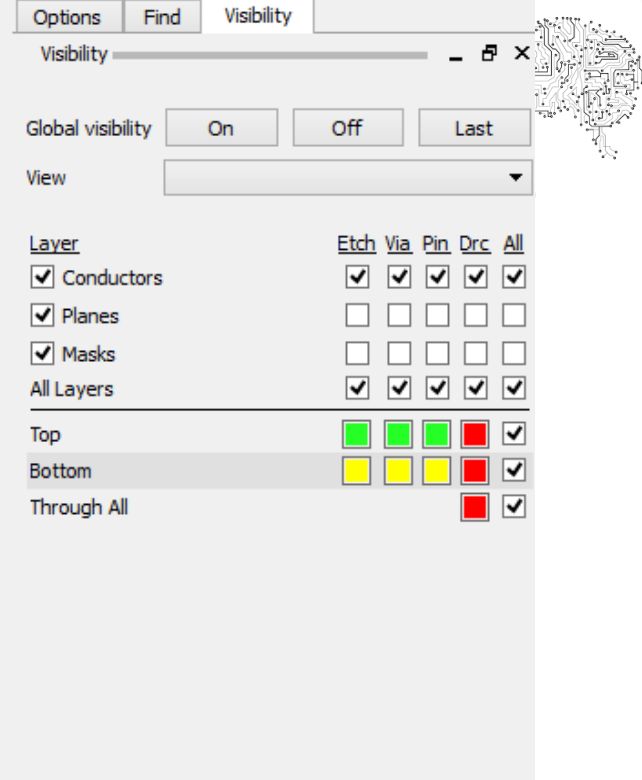
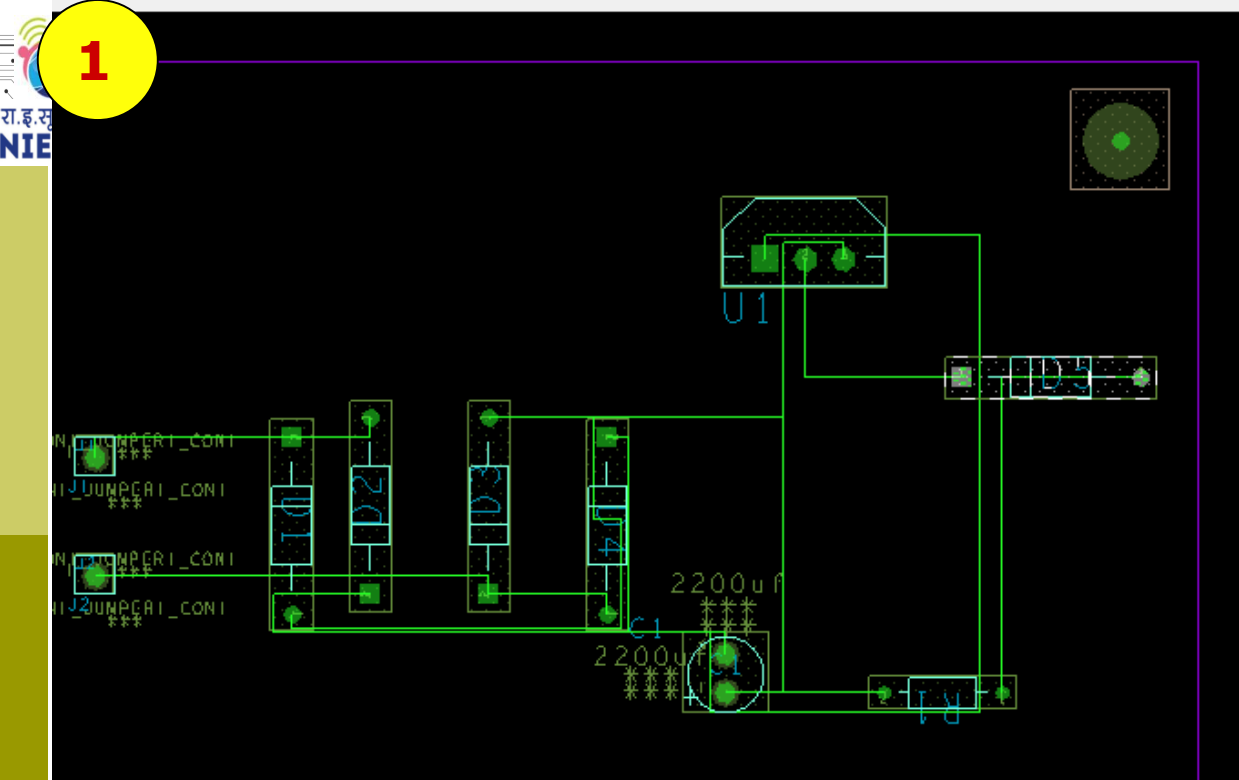
Layer	Offset / Spacing
Non-Etch	Spacing: x: 50.00, y: 50.00 Offset: x: 0.00, y: 0.00
All Etch	Spacing: x: , y: Offset: x: , y:
TOP	Spacing: x: 100.00, y: 100.00 Offset: x: 0.00, y: 0.00
BOTTOM	Spacing: x: 100.00, y: 100.00 Offset: x: 0.00, y: 0.00

At the bottom of the interface, there is a status bar with the text: "successfully, use Viewlog to review the log file."

Drill log

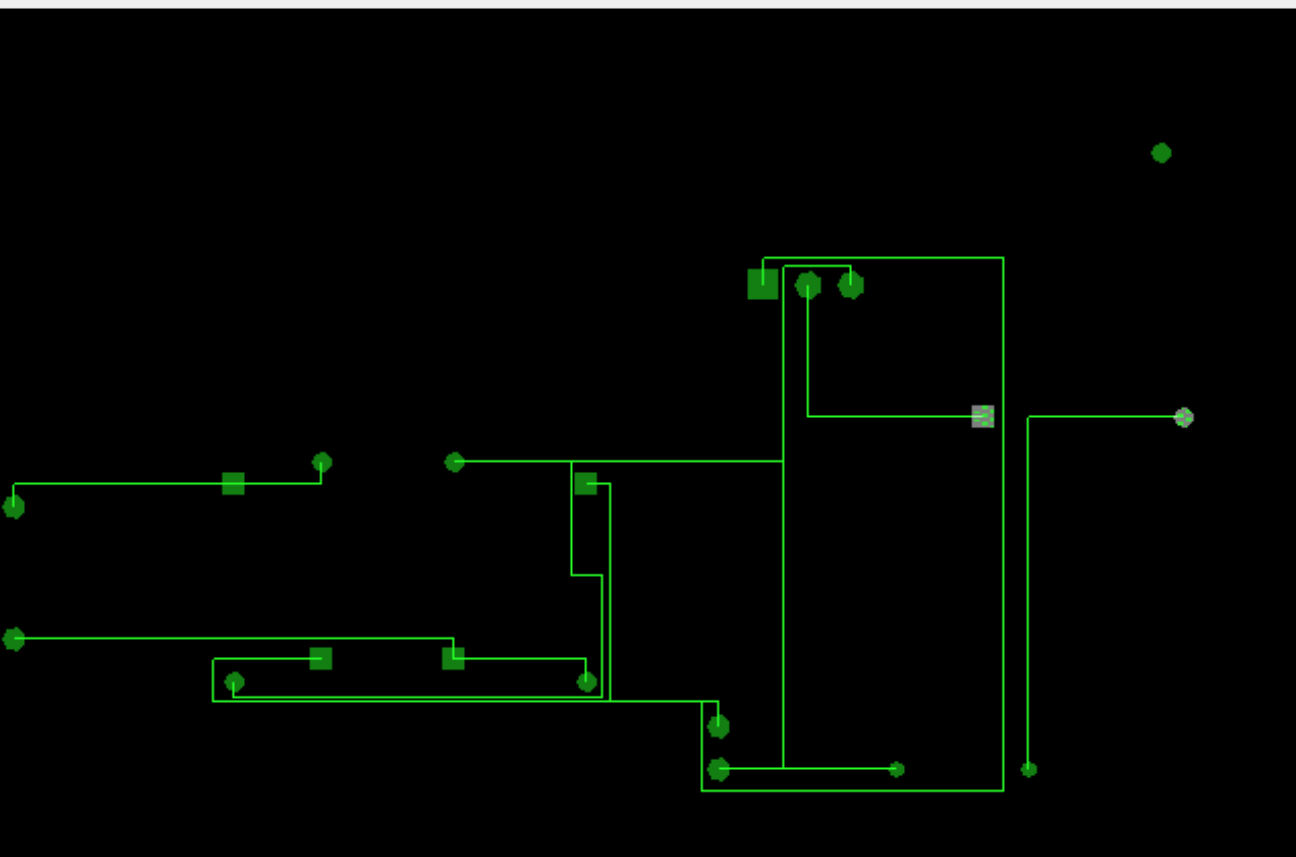
Export > NC Drill





File Edit Format View Help

```
;LEADER: 12
;HEADER:
;CODE : ASCII
;FILE : newPowerSupply-1-2.drl for ... layers TOP and BOTTOM
;DESIGN: newPowerSupply.brd
; Holesize 1. = 28.000000 Tolerance = +0.000000/-0.000000 PLATED MILS Quantity = 2
; Holesize 2. = 34.000000 Tolerance = +0.000000/-0.000000 PLATED MILS Quantity = 10
; Holesize 3. = 36.000000 Tolerance = +0.000000/-0.000000 PLATED MILS Quantity = 4
; Holesize 4. = 50.000000 Tolerance = +0.000000/-0.000000 PLATED MILS Quantity = 3
; Holesize 5. = 156.000000 Tolerance = +0.000000/-0.000000 NON_PLATED MILS Quantity = 1
%
G90
X0530000Y1190000
X0500000Y1190000
***
```



Options Find Visibility

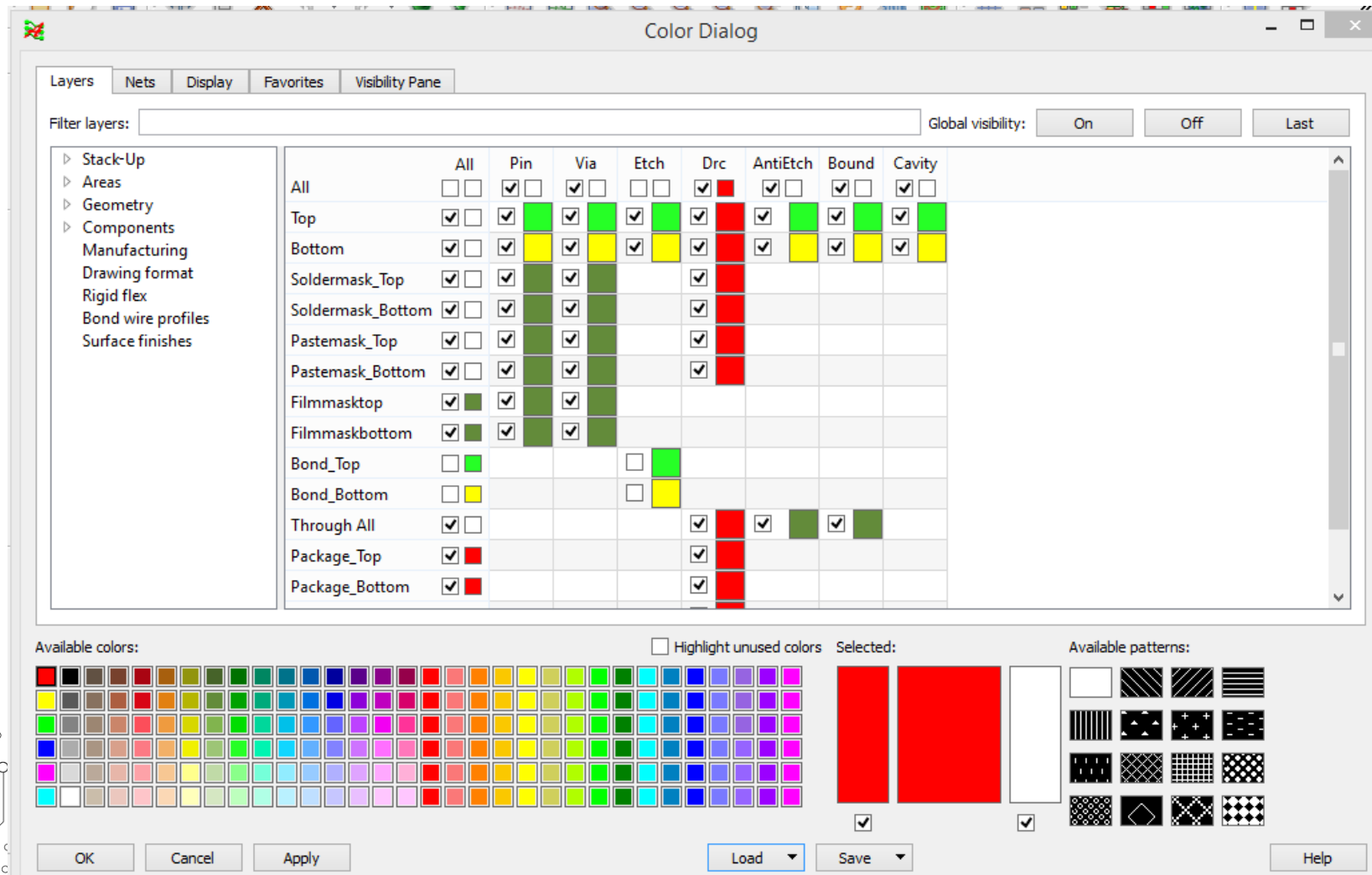
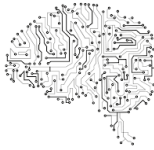
Visibility

Global visibility

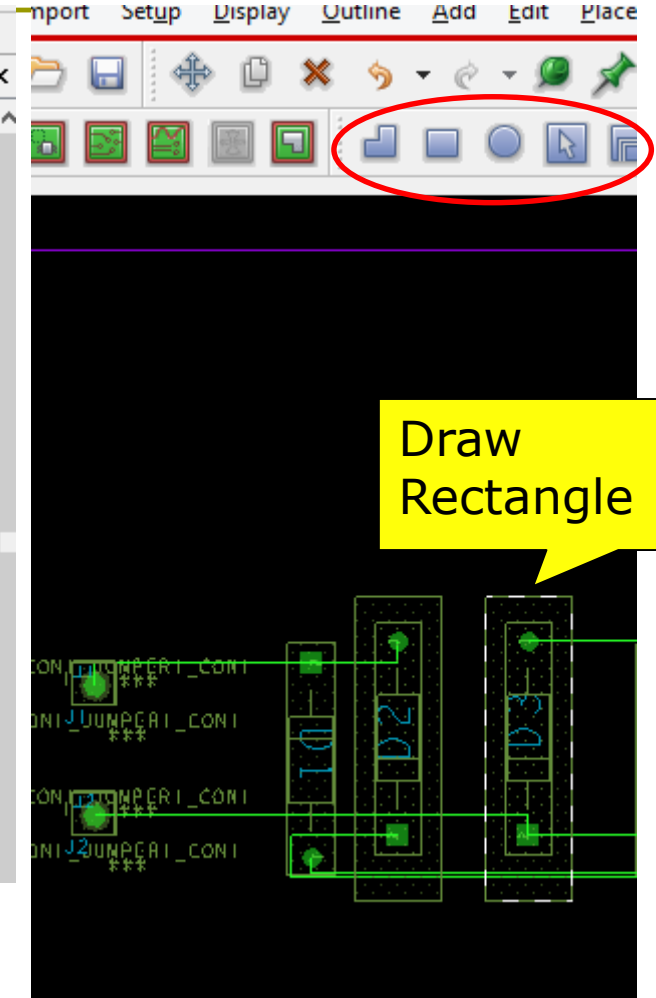
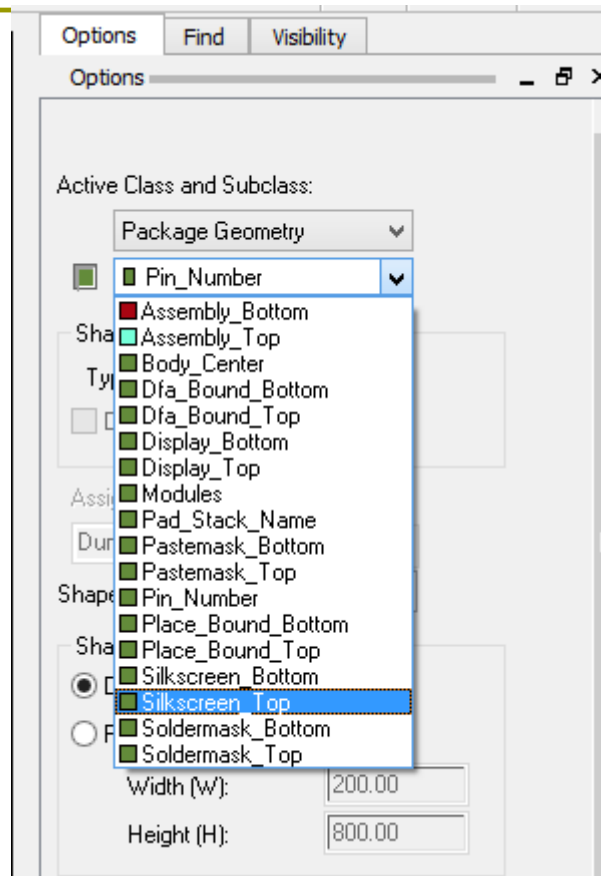
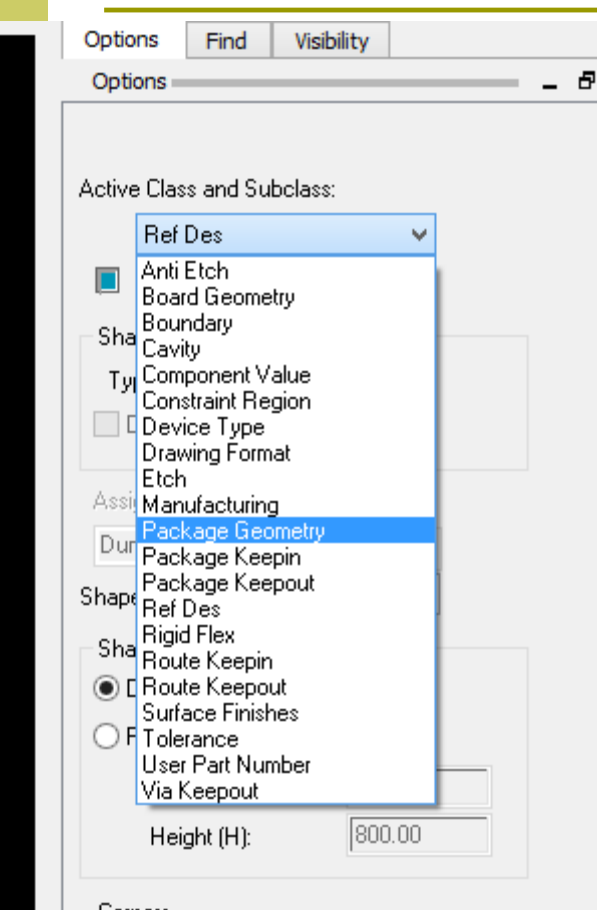
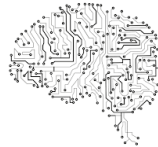
View

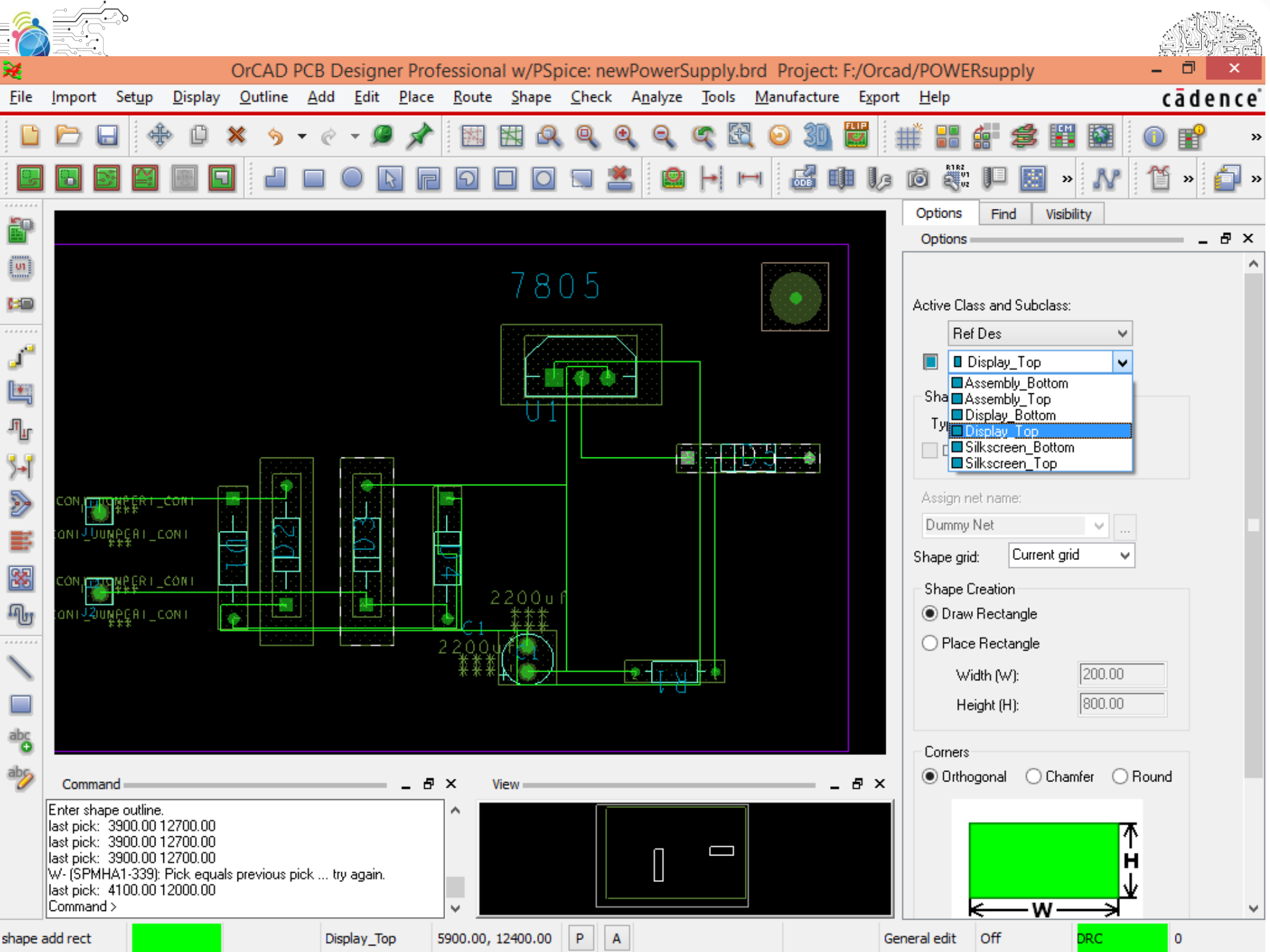
Layer	Etch	Via	Pin	Drc	All
<input checked="" type="checkbox"/> Conductors	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/> Planes	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
<input checked="" type="checkbox"/> Masks	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
All Layers	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Top	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Bottom	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Through All	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

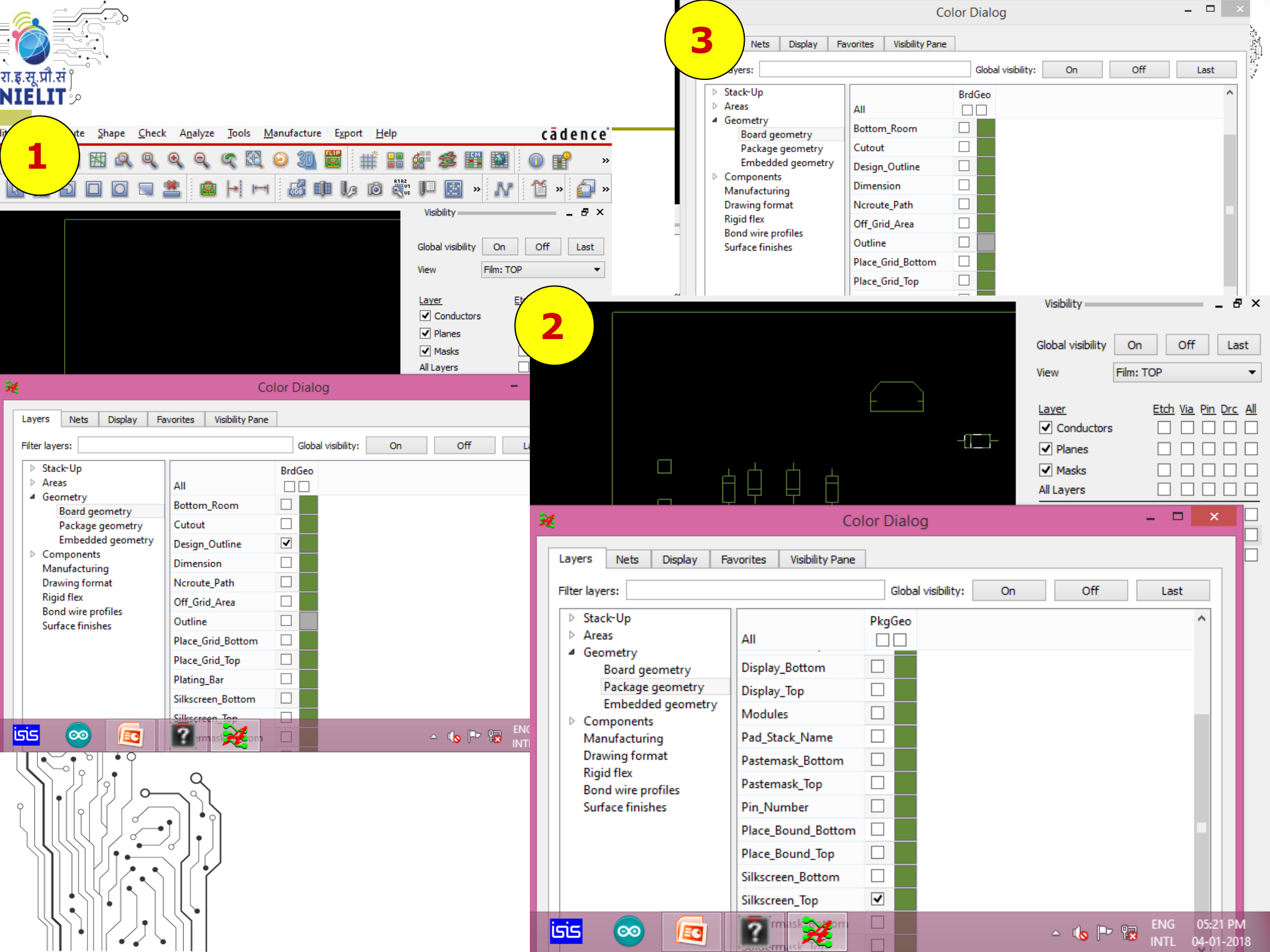
Setup > colors



Silk screen



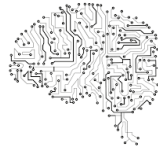




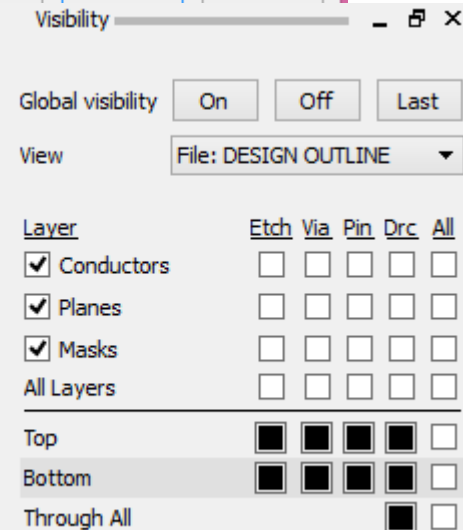
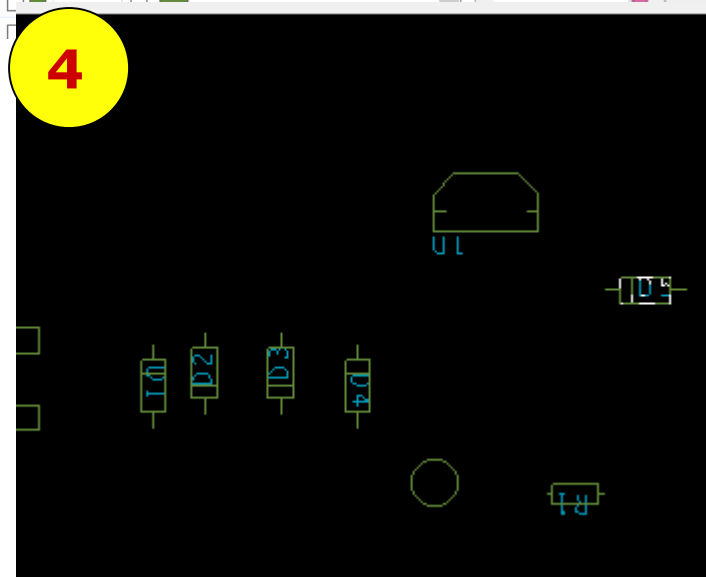
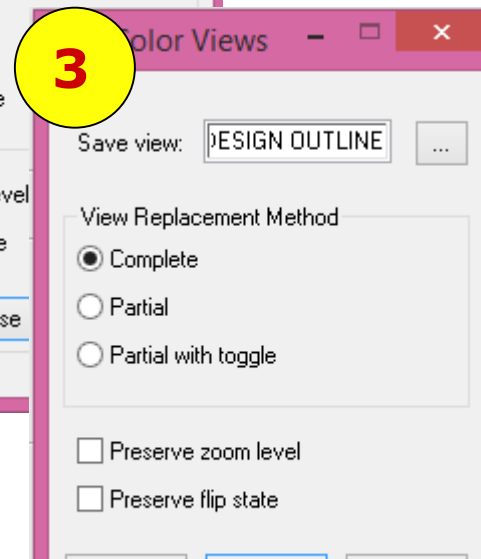
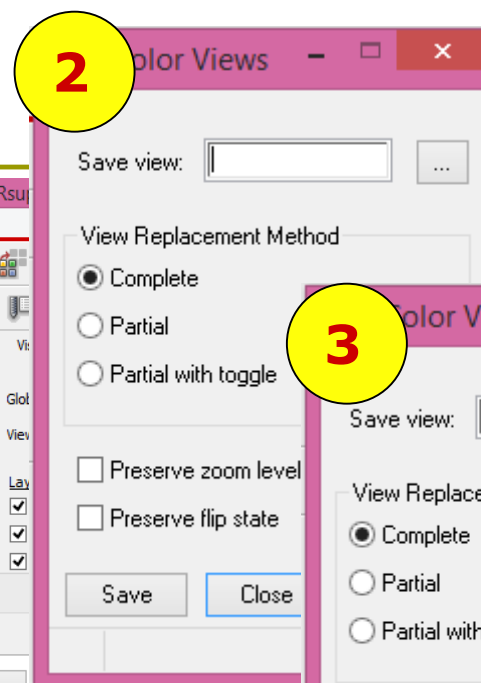
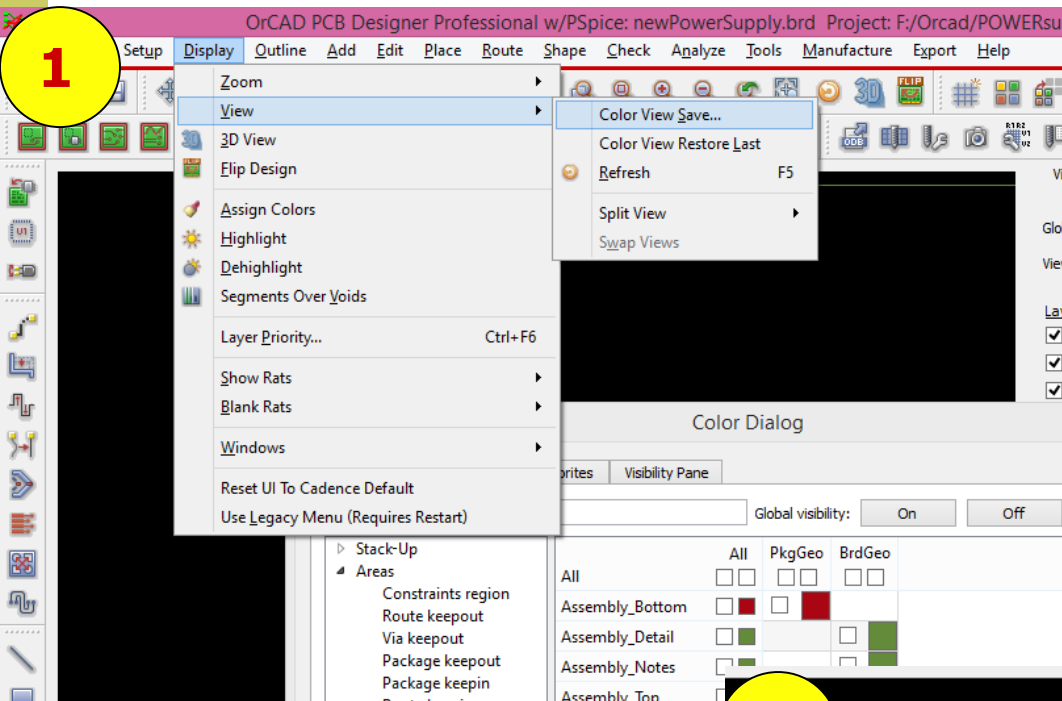
1

2

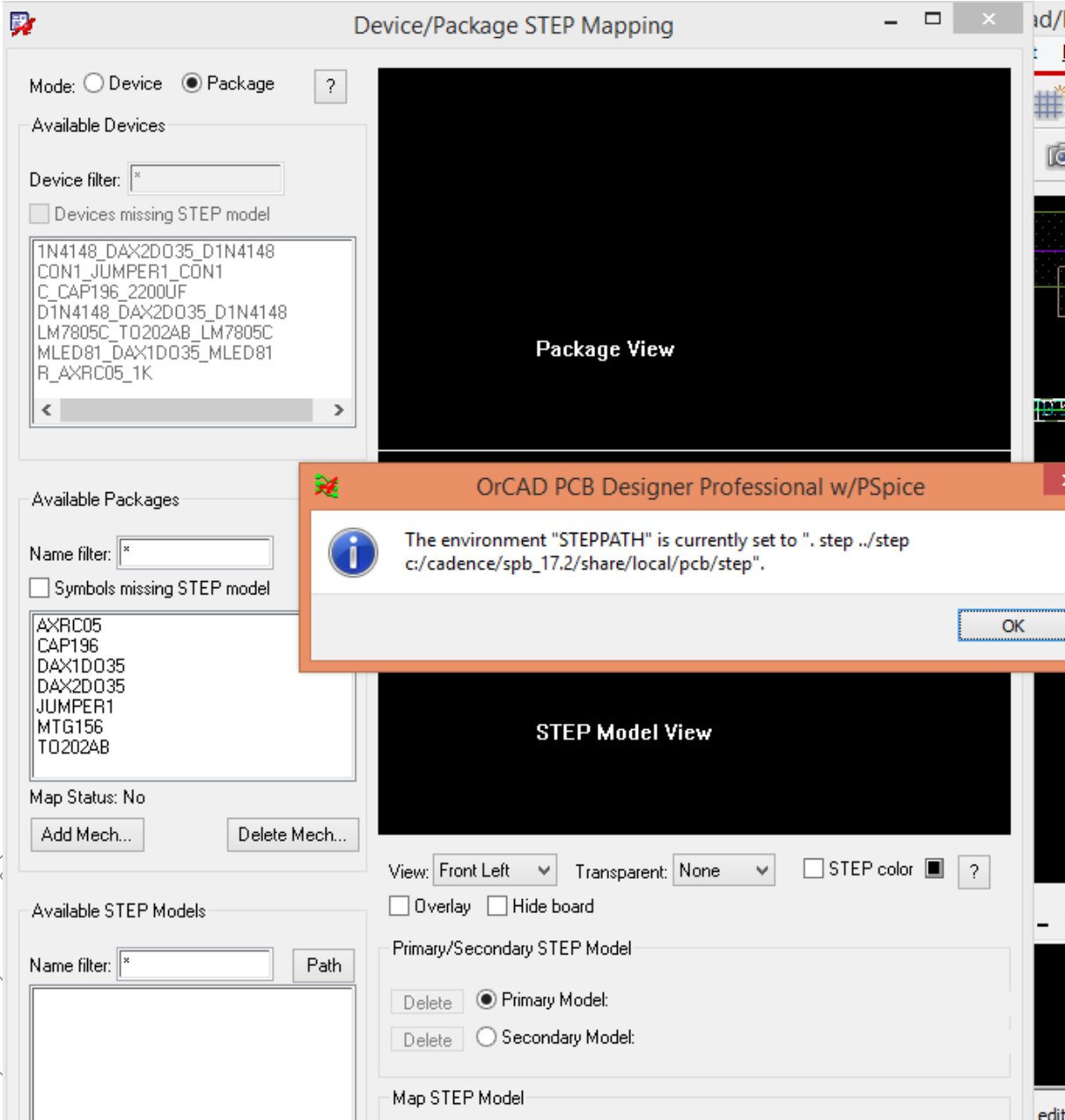
3



Creating Views



Setup > Step Mapping



Device/Package STEP Mapping

Mode: ☐ Device ☒ Package ?

Available Devices

Device filter: *

☐ Devices missing STEP model

1N4148_DAX2D035_D1N4148
CON1_JUMPER1_CON1
C_CAP196_2200UF
D1N4148_DAX2D035_D1N4148
LM7805C_T0202AB_LM7805C
MLED81_DAX1D035_MLED81
R_AXRC05_1K

Package View

Available Packages

Name filter: *

☐ Symbols missing STEP model

AXRC05
CAP196
DAX1D035
DAX2D035
JUMPER1
MTG156
T0202AB

Map Status: No

Add Mech... Delete Mech...

Available STEP Models

Name filter: * Path

STEP Model View

View: Front Left Transparent: None ☐ STEP color ☐ ?

☐ Overlay ☐ Hide board

Primary/Secondary STEP Model

Delete ☒ Primary Model
Delete ☐ Secondary Model

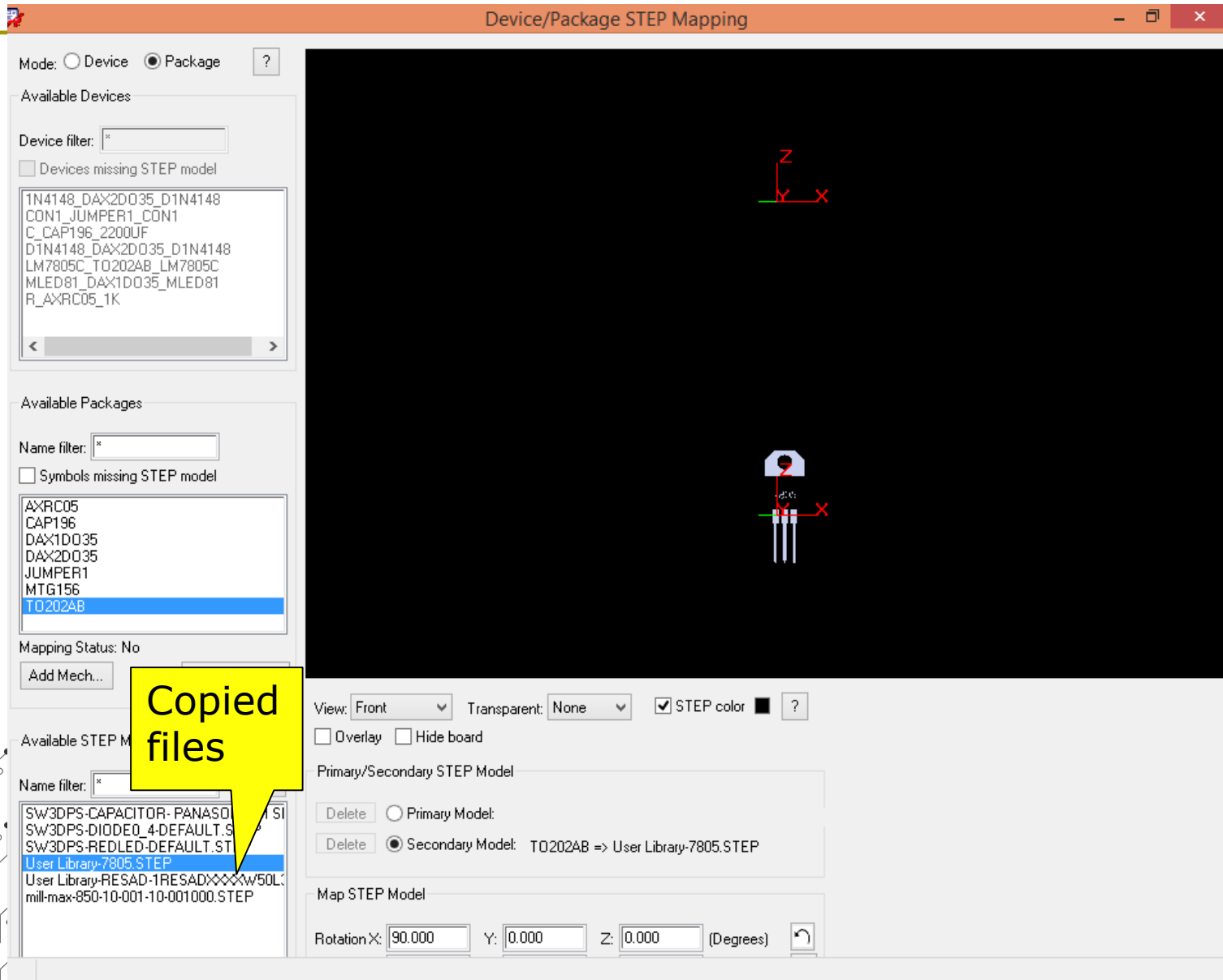
Map STEP Model

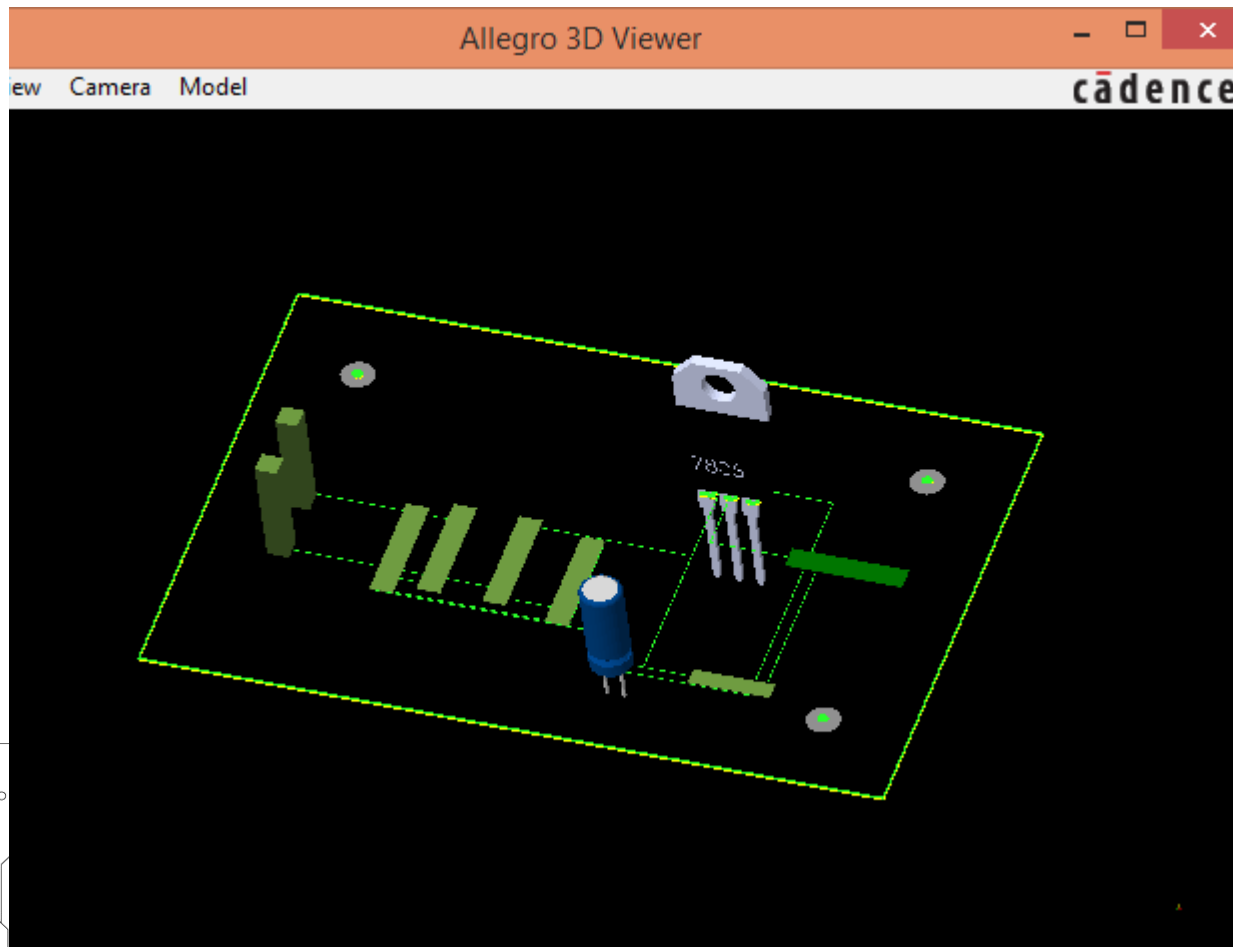
OrCAD PCB Designer Professional w/PSpice

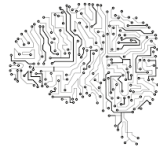
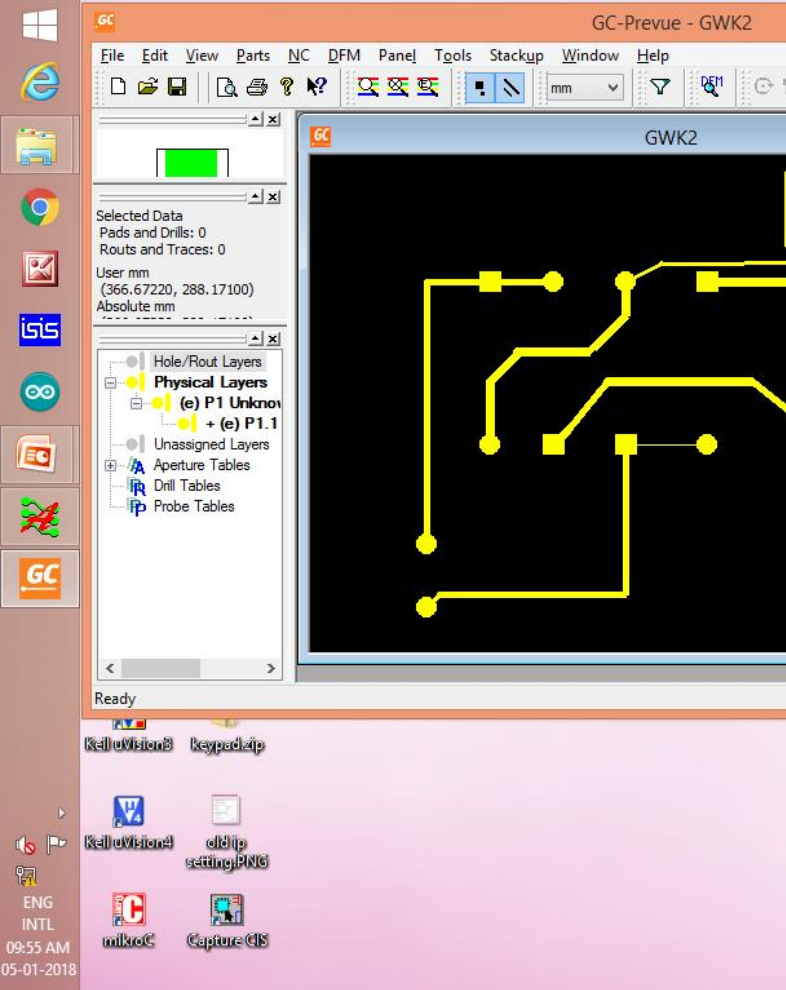
The environment "STEPPATH" is currently set to ". step ../step c:/cadence/spb_17.2/share/local/pcb/step".

OK

C:\Cadence\SPB_17.2\share\local\pcb\step







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