VLSI Design : Assignment-1

Spring 2021, IIIT Hyderabad (Instructor: Abhishek Srivastava)

Due date : 29 Jan, 2021 (23:55 hrs)

Instructions:

1. Submit your assignment as a single file in pdf format (Name_RollNo.pdf)

2. Use the given 180 nm technology file for the NGSPICE simulations

3. Answers should be complete and must be presented in a systematic way with explanation, plots, annotations and netlist

4. Maximum marks for each question is 10. Bonus marks (10) will be given for a good report

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1. Install NGSPICE. Run the given net-lists (in tutorial) and observe the results (**No need to submit this part**).

2. Plot I_D vs V_{GS} for $\frac{1.8\mu}{0.18\mu}$ NMOS transistor and estimate its V_T from the graph for the following cases :

    (a) V_{DS} = 50 mV and V_{GS} is swept from 0 to 1.8 V in a step of 0.1 V

    (b) V_{DS} = 1.8 V and V_{GS} is swept from 0 to 1.8 V in a step of 0.1 V

    (c) Do you observe any difference in V_T values in case (a) and (b) ? If yes, explain why.

3. From the simple MOS models discussed in class, find out the technology parameter μC_{ox} and V_T for NMOS and PMOS devices with the help of simulations for i) Body to source voltage (V_{BS}) of $0V$, ii) $V_{BS} = 900mV$ and ii) $V_{BS} = -900mV$. Do you observe any difference in V_T for the three cases? Explain.

4. Plot $I_D - V_{DS}$ for the two cases shown in figures 1(a) and (b). Explain why a W/2L transistor does not behave in exactly the same way as a series combination of two W/L transistors for small values of L.
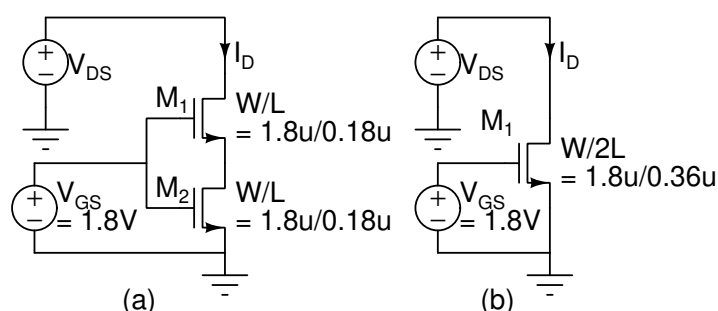

Figure 1

5. Consider the circuits shown in figures 2(a) and (b). Find the peak I_{ON} and average I_{OFF} for W= 1.8μm, W= 3.6μm, W= 18μm, W= 36μm. (Give plot snapshots and a table of I_{ON} and I_{OFF} for different W.) Do I_{ON} and I_{OFF} scale linearly with respect to W, comment.

6. Consider the schematic shown in figure 3. Switch 'SW' is closed at time t=0.

    (a) Replace the switch 'SW' by an NMOS (W/L = $\frac{1.8\mu}{0.18\mu}$) and plot v(out), when i) $v_c(0^-) = 0V$ and v(in) = 1.8V, ii) $v_c(0^-) = 1.8V$ and v(in) = 0V. Do you get exact same voltage at output as at input in steady state for both the cases. Comment for both the cases with reasons for difference (if any).
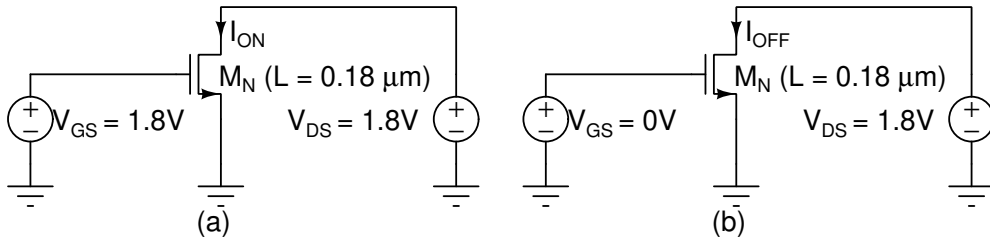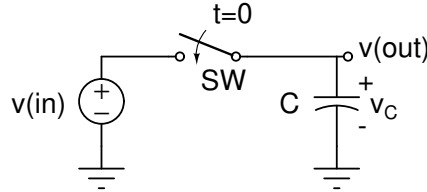
Figure 2

Figure 3

(b) Replace the switch 'SW' by an PMOS (W/L = $\frac{1.8\mu}{0.18\mu}$) and plot v(out), when i) $v_c(0^-) = 0V$ and v(in) = 1.8V, ii) $v_c(0^-) = 1.8V$ and v(in) = 0V. Do you get exact same voltage at output as at input in steady state for both the cases. Comment for both the cases with reasons for difference (if any).

(Hint : use .ic v(node-name)=value to set initial condition at a node before .control in your netlist)

7. Write a netlist for the circuit shown in figure 4. Remember to specify the AS, AD and PS, PD parameters for the transistors. Plot V_{out} with respect to time and calculate the propagation delay
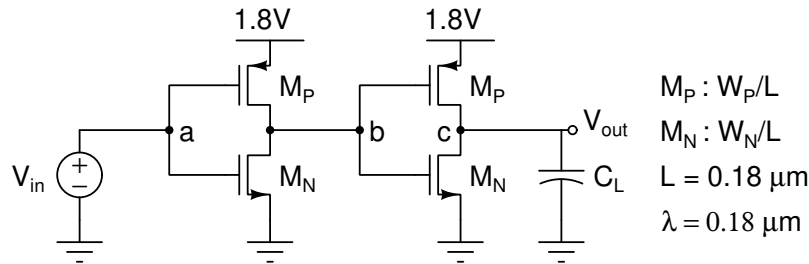

Figure 4

between input and output (t_{pd}) and tabulate them for the following cases:
Given: V_{in} (vin a 0 pulse 0 1.8 0ns 100ps 100ps 9.9ns 20ns)

(a) C_L =100 fF, $W_n = 1.8\mu$m $W_p = 2.5 \times W_n$

(b) C_L =500 fF $W_n = 1.8\mu$m $W_p = 2.5 \times W_n$

(c) C_L =500 fF $W_n = 9\mu$m $W_p = 2.5 \times W_n$.

(d) From the delay table, comment how the scaling up of transistor widths affects the propagation delays.

Note: Delay = (rise-time + fall-time)/2, where rise-time is defined as the delay between rising output and corresponding falling input when both are at their 50% values. Similarly fall-time is defined as the delay between falling output and corresponding rising input when both are at their 50% values.