VLSI design Assignment-1 report

U. S. S. Sasanka-2019102036

Question 2

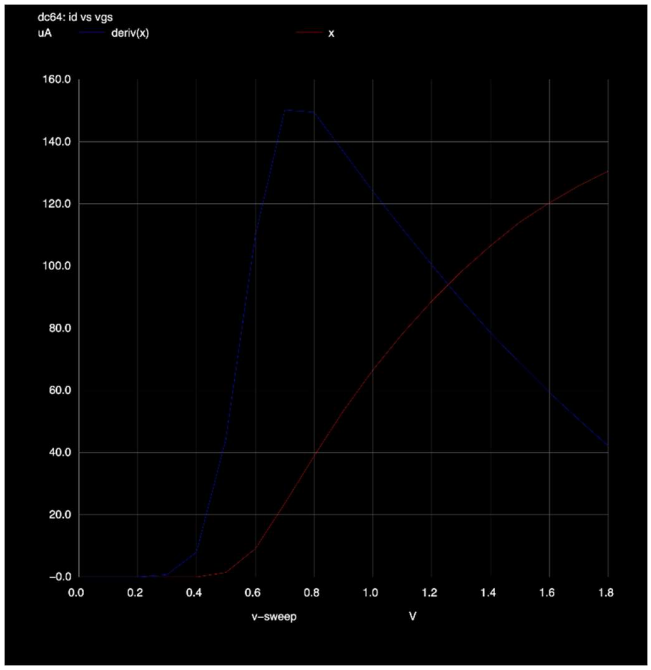
Code:

```
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.global gnd vdd

VGS     G       gnd 'SUPPLY'
VDS D   gnd 0.05V
VDS1 D1 gnd 1.8V

M1      D       G       gnd     gnd  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M2      D1       G       gnd     gnd  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}


.dc VGS 0 1.8 0.1


.control

run

let x = -VDS#branch
let y = -VDS1#branch
set curplottitle="id vs vgs"
let vectri=vecmax(deriv(x))
let vecsat=vecmax(deriv(sqrt(y)))
print vectri
print vecsat

plot x
set hcopypscolor = 1 *White background
plot y
*hardcopy question1.eps x y
plot deriv(x)
plot deriv(sqrt(y))
.endc
"question2.sp" 42L, 883C
```

We have included the necessary header and defined parameters. Then we define the points G, D, S and their potentials. Later we defined the two MOSFETS one which has drain voltage at 0.05V and the other with the drain voltage 1.8V. We then plotted the current vs VGS graphs and also included the derivatives which help to calculate the threshold voltage Vth.

Plots:

Figure1



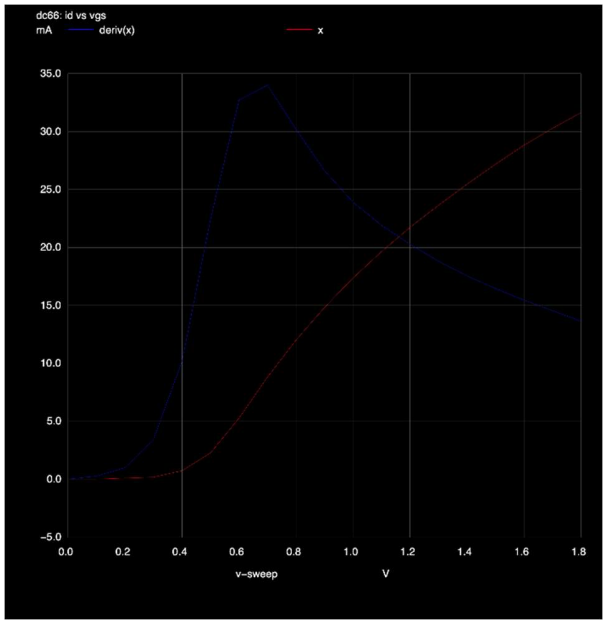


Figure 2

Explanation:

Figure 1:

VDS=0.05V; VGS=1.8V

Here, we have taken the value of VDS such that the MOSFET is in triode region(ie VDS<=VGS-Vth). The current plot(red) is as expected abides with the relation IDS=0.5*un*cox*W/L((2Vgs-Vth)Vds-Vds^2).

Figure 2:

VDS=1.8V; VGS=1.8V

Here, we have taken the value of VDS such that the MOSFET is in saturation region(VDS>=VGS-Vth). The current plot(red) is as expected abides with the relation IDS=0.5*un*cox*W/L(Vgs-Vth)^2.

Now, we need to find the Vth.

1) One simple way is by directly using the MOSFET cutoff property which indicates that Ids is non-zero only when Vgs>Vth. So by checking the graph values, we get that **Vth= 0.399306(for triode)** in figure 1 and **Vth= 0.376087 (for saturation)** in figure2.

However this method is **unreliable** because we neglect the **subthreshold region current** which is non-zero and hence we don't get the values as expected. We have to take values to the right where the value is non-zero.

The solution is to take the point where the **slope is maximum**, because the maximum change in sloped indicates the actual ideal point where the value of current changes from 0 to non-zero.

2) So the better method is to take the point where we have the maximum slope, **draw a tangent** and see where it intersects the Vgs axis to get Vth.

However even in this method, there are two cases, one for linear region and the other for the saturation region.

For linear region we directly take the point where the slope is maximum to ensure linear behavior whereas for the saturation region, we take a point on the square root of the slope graph to detect the change.

We calculate the respective points where the above criteria is satisfied and then calculate the line equation from which we can get the value of Vth which is the point where the lines cuts Vgs axis.

Calculations:

a) $V_{DS} = 0.05V$; $V_{GS} = 1.8V$

We notice from $\frac{dI_{DS}}{dV_{GS}}$ vs V_{GS} graph

that the maximum slope $= 150.1 \times 10^{-6}$

The corresponding point in $V_{GS} = 700 \times 10^{-6}$

$\therefore$ Point $(700, 150.1)\ \mu$

x_1 m_1

Now we find y_1 which is the point (x_1, y_1) in I_{DS} vs V_{GS} graph.

We got $y_1 = 24.1 \times 10^{-6}$

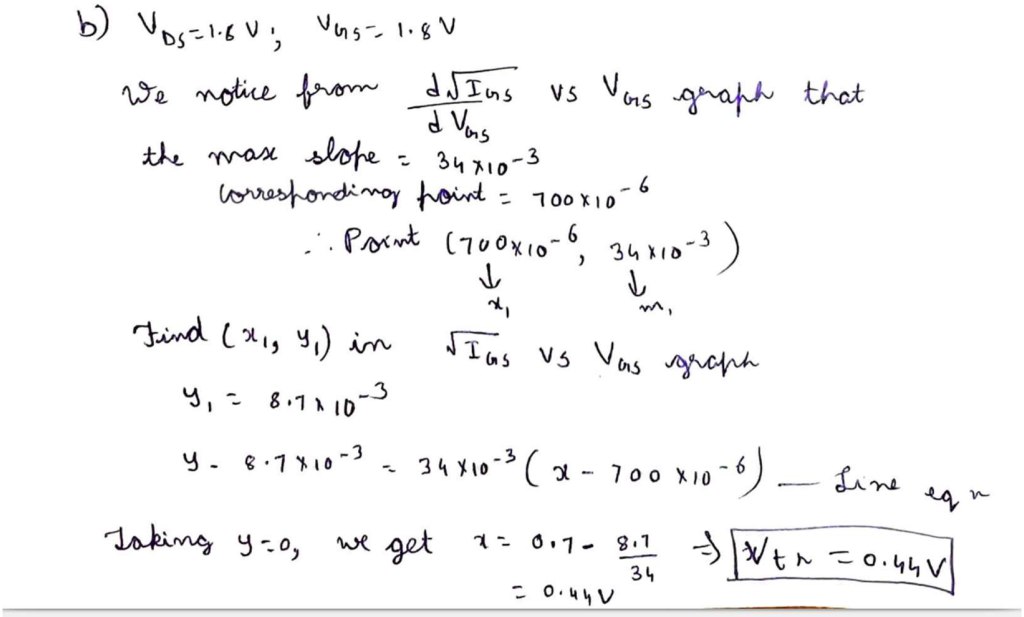
$y - 24.1 = 150.1\,(x - 700)$ ___ line equation

Taking $y = 0$, we get $x = 700 - \frac{24.1}{150.1} \times 10^{-6}\ V$

$= 0.7 - 0.16\ V$

$= 0.54V$

$V_{th} = 0.54V$



Result and inference:

We get Vth in triode region to be **Vth=0.54V** whereas we get the value of Vth in saturation region to be **Vth=0.44V**.

We clearly notice that the threshold voltage in the saturation region is lesser than that of in triode region. This is due to an effect called the **Drain induced barrier lowering.** When the MOSFET has high drain voltage, it aids in the forming of the inversion layer which effectively reduces the threshold voltage given by the formula Vth=Vth0-n*VDS where Vth0 is the value of threshold voltage when VDS=0 and n is a constant.

Question 3

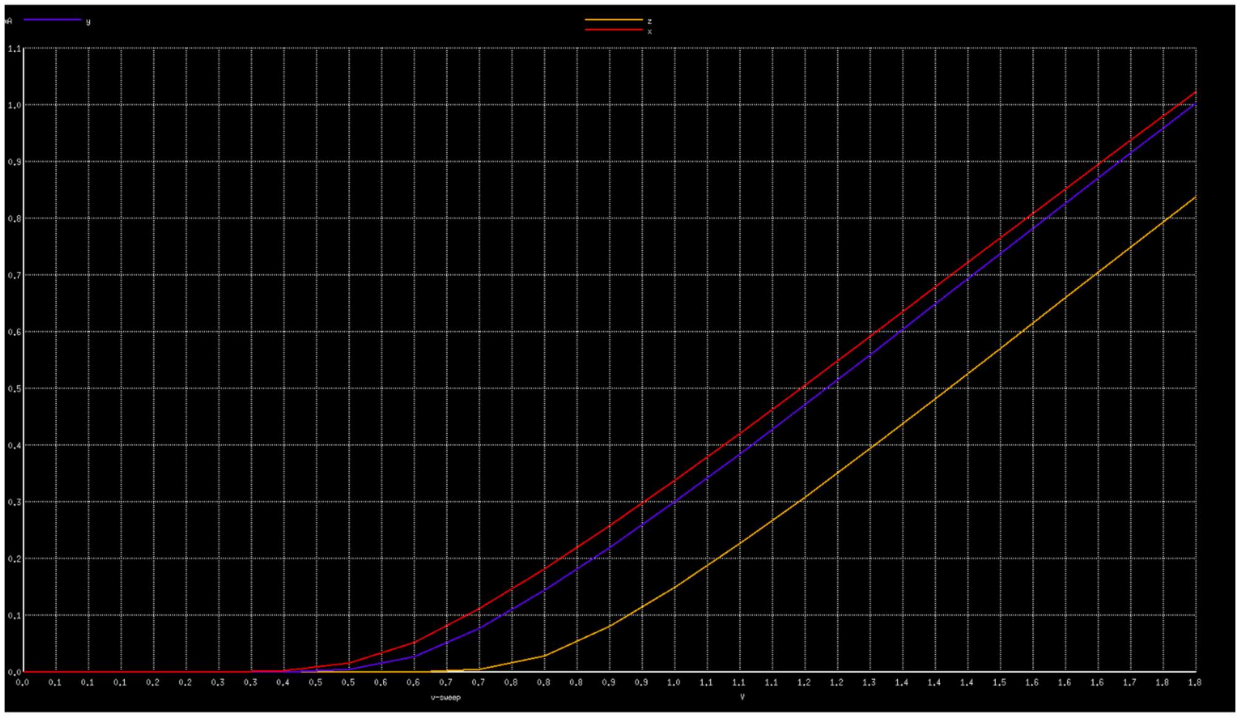
A)

Code:

```
Netlist to evaluate MOS I-V characterisitics

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param VGG=1.5
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.global gnd vdd

VGS     G       gnd 'SUPPLY'
VDS D   gnd 1.8V
VDS1 D1 gnd 1.8V
VDS2 D2 gnd 1.8V
VBS B  gnd -0.9V
VBS1 B1 gnd 0.9V

M1      D       G       gnd     B1  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M2      D1      G       gnd     gnd  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M3      D2      G       gnd     B  CMOSN   W={width_N}   L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}


.dc VGS 0 1.8 0.1


.control

run

let x = -VDS#branch
let y = -VDS1#branch
let z = -VDS2#branch

set curplottitle="id vs vgs"


plot x
plot y
plot z
```

Here, we take the same setup as previous question but only change is we take is the value of voltage of Body to be non-zero. We take VBS=0, 0.9, -0.9 V and then find the IDS vs VGS and then we find the Vth value as well. Note that we also require der(sqrt(IDS) vs VGS graphs as well.

Plots:



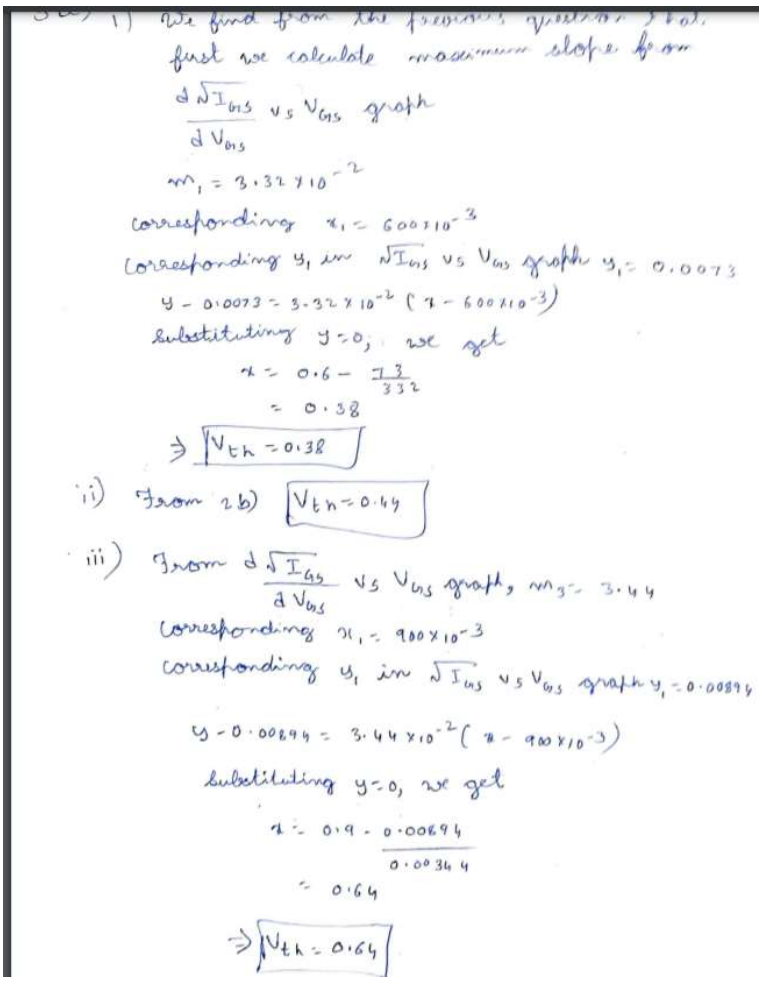
Explanation:

We have already seen the red graph in the previous question. We know that the shapes of the rest of the graph is also same but the threshold voltage either increases or decreases. This is explained by a phenomenon callled the **body effect.**

Let us take **VBS as positive**, then at the body, we notice that the holes in the p substrate drift towards the gate and thus cause the channel to form less slowly and thus **increases** the Vth.

When we take **VBS<0**, then we the holes drift towards the gate and form the channel easily and thus **decreases** Vth.

Calculations:



i) We find from the previous question that, first we calculate maximum slope from $\frac{d\sqrt{I_{DS}}}{dV_{DS}}$ vs V_{GS} graph

$m_1 = 3.32 \times 10^{-2}$

corresponding $x_1 = 600 \times 10^{-3}$

Corresponding y_1 in $\sqrt{I_{DS}}$ vs V_{GS} graph $y_1 = 0.0073$

$y - 0.0073 = 3.32 \times 10^{-2} (x - 600 \times 10^{-3})$

Substituting $y = 0$, we get

$x = 0.6 - \frac{73}{332}$

$= 0.38$

$\Rightarrow \boxed{V_{th} = 0.38}$

ii) From 2b) $\boxed{V_{th} = 0.44}$

iii) From $\frac{d\sqrt{I_{DS}}}{dV_{DS}}$ vs V_{GS} graph, $m_3 = 3.44$

corresponding $x_1 = 900 \times 10^{-3}$

corresponding y_1 in $\sqrt{I_{DS}}$ vs V_{GS} graph $y_1 = 0.00894$

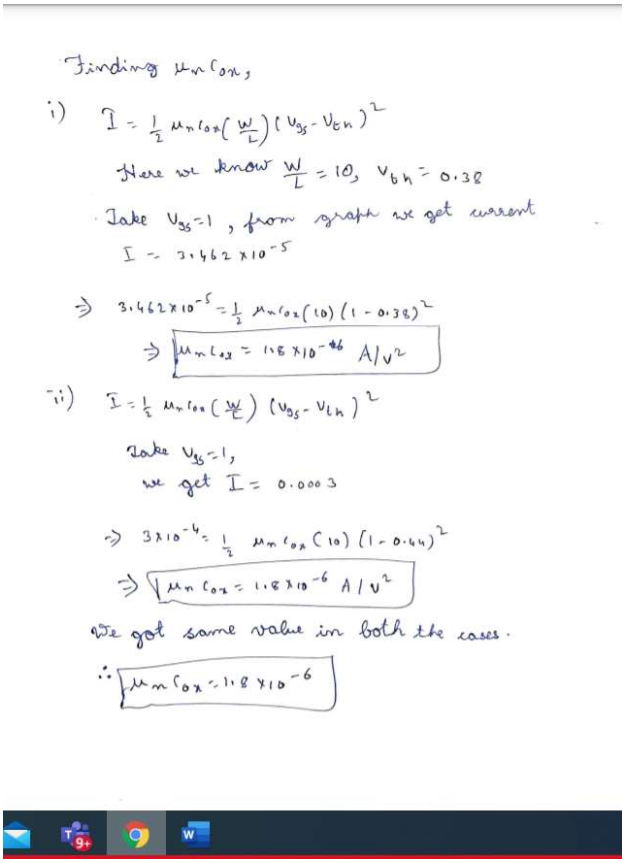
$y - 0.00894 = 3.44 \times 10^{-2} (x - 900 \times 10^{-3})$

Substituting $y = 0$, we get

$x = 0.9 - \frac{0.00894}{0.00344}$

$= 0.64$

$\Rightarrow \boxed{V_{th} = 0.64}$



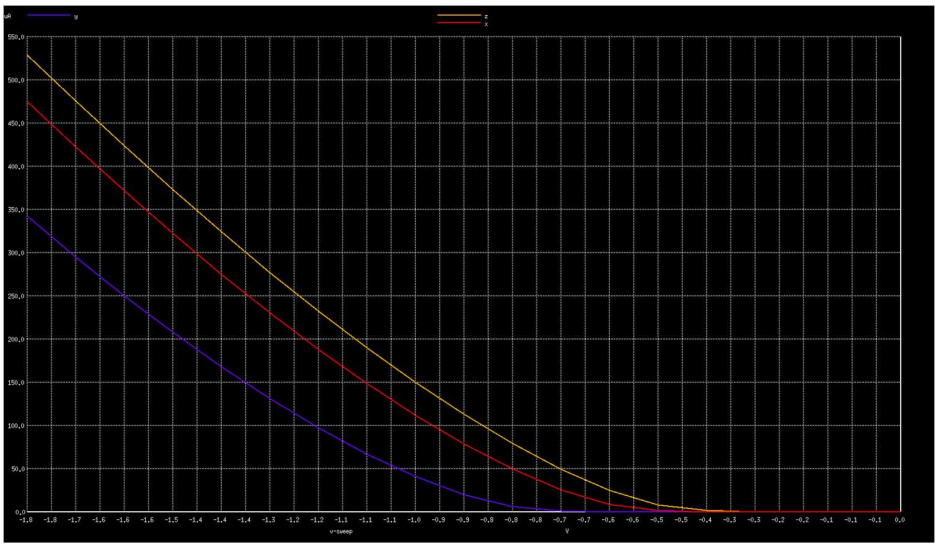
B)

Codes:

```
Netlist to evaluate MOS I-V characterisitics

.include TSMC_180nm.txt
.param SUPPLY=-1.8
.param VGG=1.5
.param LAMBDA=0.09u
.param width_P={20*LAMBDA}
.param width_N={20*LAMBDA}
.global gnd vdd


VGS     G       gnd 'SUPPLY'
VDS D   gnd -1.8V
VDS1 D1 gnd -1.8V
VDS2 D2 gnd -1.8V
VBS B  gnd -0.9V
VBS1 B1 gnd 0.9V

M1      gnd       G       D1     B1  CMOSP   W={width_P}   L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M2      gnd       G       D     gnd  CMOSP   W={width_P}   L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M3      gnd       G       D2     B  CMOSP   W={width_P}   L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}


.dc VGS 0 -1.8 -0.1


.control
```

```
run

let x = VDS#branch
let y = VDS1#branch
let z = VDS2#branch

let x1=vecmin(deriv(sqrt(x)))
let x2=vecmin(deriv(sqrt(y)))
let x3=vecmin(deriv(sqrt(z)))
print x1
print x2
print x3
set curplottitle="id vs vgs"

plot x deriv(sqrt(x))
plot y deriv(sqrt(y))
plot z deriv(sqrt(z))
plot x y z

set hcopypscolor = 1 *White background
*hardcopy question1.eps x y
.endc
                                                                    55,5          Bot
```

Plots:



The above plot is for the pmos. We notice the same thing we noticed with the nmos but just the values are flipped to the negative side of the voltage due to the characteristics of the pmos.

The method to find the Vth remains effectively the same.

The reason for this graph to look like this is the body effect.

Calculations:

The same procedure is followed to get the values of Vth for x, y, z as

Vthx=-0.36

Vthy=-0.45

Vthz=-0.67

From the similar method that we calculated the values of upcox which turns out to be **2.21*10^-4**

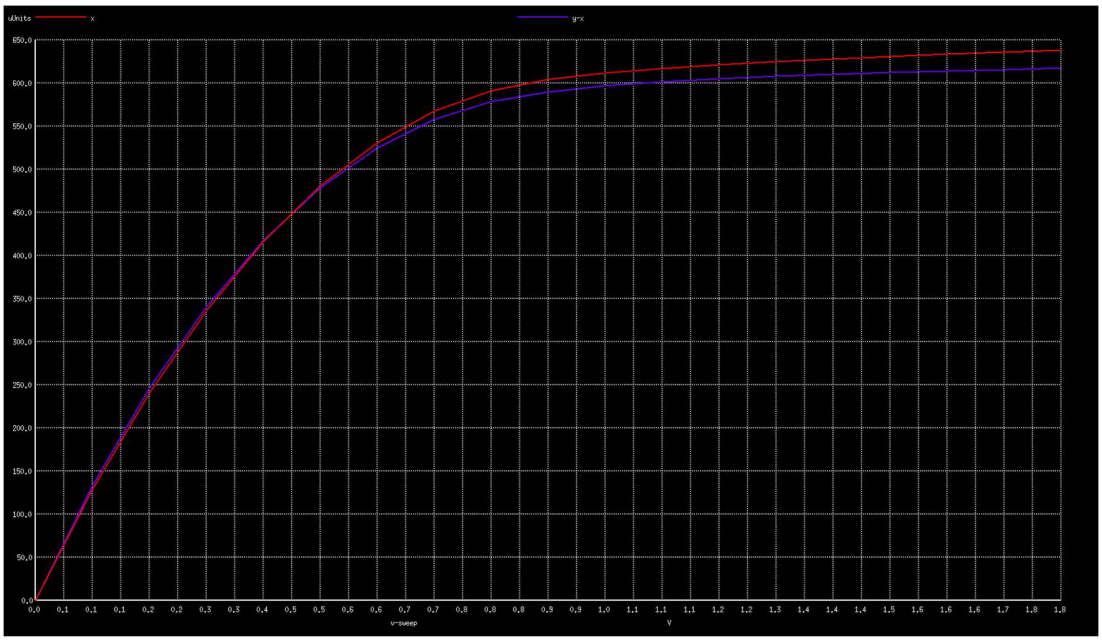
Question 4

Code:

```
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param VGG=1.5
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.global gnd vdd



VGS G gnd 'SUPPLY'
VDS D gnd 1.8
VSD1 S D1 0



M1 D G S gnd CMOSN W={width_N} L={2*LAMBDA}
+AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}



M2 D1 G gnd gnd CMOSN W={width_N} L={2*LAMBDA}
+AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}



M3 D G gnd gnd CMOSN W={width_N} L={2*2*LAMBDA}
+AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}


.dc VDS 0 1.8 0.1


.control

run

let x = VSD1#branch
let y = -VDS#branch
set curplottitle="id vs vds"
plot x y-x

.endc
~
"question4copy.sp" 45L, 793C
```

Here, we have taken two MOSFETs of each of W/L in series and one MOSFET of W/2L. We take a common point D and it gives VDS. We assume the current is x in the branch with the two MOSFETs, then we take the current in the other branch to be y-x where y is the total current of the VDS branch. We print the plots and observe.

Plots:



RED– Series MOSFETs

BLUE- Single MOSFET

Explanation:

Since in most cases we assume that the effective width/length between the series MOSFETs is W/2L expect that both the graphs are he same but they are not.

This is because the two devices are two different devices i.e. l**ong channel devices and short channel devices**. The two MOSFETs in series are of length L(short channel) and the other one is length 2L(Long channel).

We know that the long channel devices have lesser **second order effects** when compared to the short channel devices. The effects like mos capacitance and channel length modulation result in the increase in current for the short channel device.

In the **mos capacitance**, we have couple of capacitors in parallel and thus effectively increasing the total capacitance and hence increasing the current for MOSFETs in series.

In the **channel length**, we have two L length MOSFETs, since length is less for the series MOSFETs, we can expect that the current is higher in them due to the channel length modulation. This can also be explained like this let x be the pinchoff length. For the two MOSFETS the pinch of length will be L-x+L-x=2L-2x. For the single MOSFET however, we have 2L-x pinch off meaning that the combined one has higher current due to the inverse relatiosnship between current and channel width.

Question 5

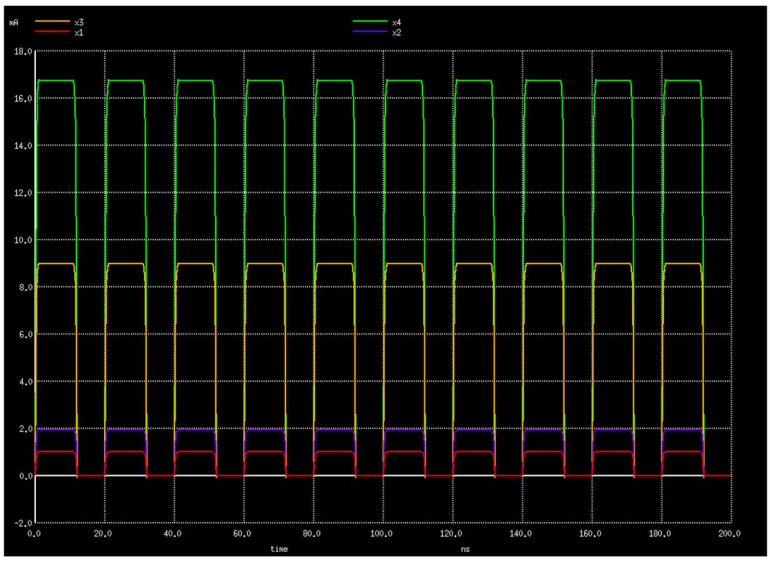
A)Codes:

```
Netlist to evaluate MOS I-V characterisitics

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param VGG=1.5
.param LAMBDA=0.09u
.param width_N1={20*LAMBDA}
.param width_N2={40*LAMBDA}
.param width_N3={200*LAMBDA}
.param width_N4={400*LAMBDA}

.global gnd vdd

VGS     G       gnd 'SUPPLY'
VDS1 D1   gnd pulse 0 1.8 0ns 1ns 1ns 10ns 20ns
VDS2 D2   gnd pulse 0 1.8 0ns 1ns 1ns 10ns 20ns
VDS3 D3   gnd pulse 0 1.8 0ns 1ns 1ns 10ns 20ns
VDS4 D4   gnd pulse 0 1.8 0ns 1ns 1ns 10ns 20ns



M1      D1      G       gnd     gnd  CMOSN   W={width_N1}   L={2*LAMBDA}
+ AS={5*width_N1*LAMBDA} PS={10*LAMBDA+2*width_N1} AD={5*width_N1*LAMBDA} PD={10*LAMBDA+2*width_N1}

M2      D2      G       gnd     gnd  CMOSN   W={width_N2}   L={2*LAMBDA}
+ AS={5*width_N2*LAMBDA} PS={10*LAMBDA+2*width_N2} AD={5*width_N2*LAMBDA} PD={10*LAMBDA+2*width_N2}

M3      D3      G       gnd     gnd  CMOSN   W={width_N3}   L={2*LAMBDA}
+ AS={5*width_N3*LAMBDA} PS={10*LAMBDA+2*width_N3} AD={5*width_N3*LAMBDA} PD={10*LAMBDA+2*width_N3}

M4      D4      G       gnd     gnd  CMOSN   W={width_N4}   L={2*LAMBDA}
+ AS={5*width_N4*LAMBDA} PS={10*LAMBDA+2*width_N4} AD={5*width_N4*LAMBDA} PD={10*LAMBDA+2*width_N4}

.tran 0.1n 200n


.control
```

```
run

plot v(D1)
let x1= -VDS1#branch
let x2= -VDS2#branch
let x3= -VDS3#branch
let x4= -VDS4#branch

let vec1=vecmax(x1)
let vec2=vecmax(x2)
let vec3=vecmax(x3)
let vec4=vecmax(x4)
print vec1
print vec2
print vec3
print vec4

set curplottitle="id vs vds"
plot x1 x2 x3 x4
set hcopypscolor = 1 *White background
.endc
```

Here, we have to calculate ION time of the nMOSFET. We take different values of W for the MOSFET and obtain the plots. To calculate the peak Ion, we take the input VDS=1.8, to be a pulse for 10ns. Then we have calculated the maximum value of current in the time interval 0 to 200ns. Note that we consider transient analysis here owing to the fact that we have an ac kind of input.

PLOTS:



The highest peak is for W=36 and lowest for W=1.8

Explanation:

For

W=1.8 IONpeak=1 mA

W=3.6 IONpeak=1.94mA

W=18 IONpeak=9.01mA

W=36 IONpeak=16.8mA

Clearly we notice that there is slight variation in the linear relation due to the fact that there are many second order effects that occur when we increase the width.

B)

```
Netlist to evaluate MOS I-V characterisitics

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param VGG=1.5
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.global gnd vdd

VGS     G       gnd 0V
VDS1 D1   gnd pulse 0 1.8 0ns 1ns 1ns 10ns 20ns
VDS2 D2   gnd pulse 0 1.8 0ns 1ns 1ns 10ns 20ns
VDS3 D3   gnd pulse 0 1.8 0ns 1ns 1ns 10ns 20ns
VDS4 D4   gnd pulse 0 1.8 0ns 1ns 1ns 10ns 20ns



M1      D1       G       gnd     gnd  CMOSN   W={width_N}    L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M2      D2       G       gnd     gnd  CMOSN   W={2*width_N}    L={2*LAMBDA}
+ AS={5*2*width_N*LAMBDA} PS={10*LAMBDA+2*2*width_N} AD={5*2*width_N*LAMBDA} PD={10*LAMBDA+2*2*width_N}

M3      D3       G       gnd     gnd  CMOSN   W={10*width_N}    L={2*LAMBDA}
+ AS={5*10*width_N*LAMBDA} PS={10*LAMBDA+2*10*width_N} AD={5*10*width_N*LAMBDA} PD={10*LAMBDA+2*10*width_N}

M4      D4       G       gnd     gnd  CMOSN   W={20*width_N}    L={2*LAMBDA}
+ AS={5*20*width_N*LAMBDA} PS={10*LAMBDA+2*20*width_N} AD={5*20*width_N*LAMBDA} PD={10*LAMBDA+2*20*width_N}

.tran 0.1n 2n

                                                                                1,4
```

```
.control

run

plot v(D1)
let x1= -VDS1#branch
let x2= -VDS2#branch
let x3= -VDS3#branch
let x4= -VDS4#branch


set curplottitle="id vs vds"
plot x1 x2 x3 x4
set hcopypscolor = 1 *White background
plot avg(x1) avg(x2) avg(x3) avg(x4)
.endc
```

We just take the VGS=0, So we expect current to not flow. But due to leakage current, we get IOFF whose plot is as follows.

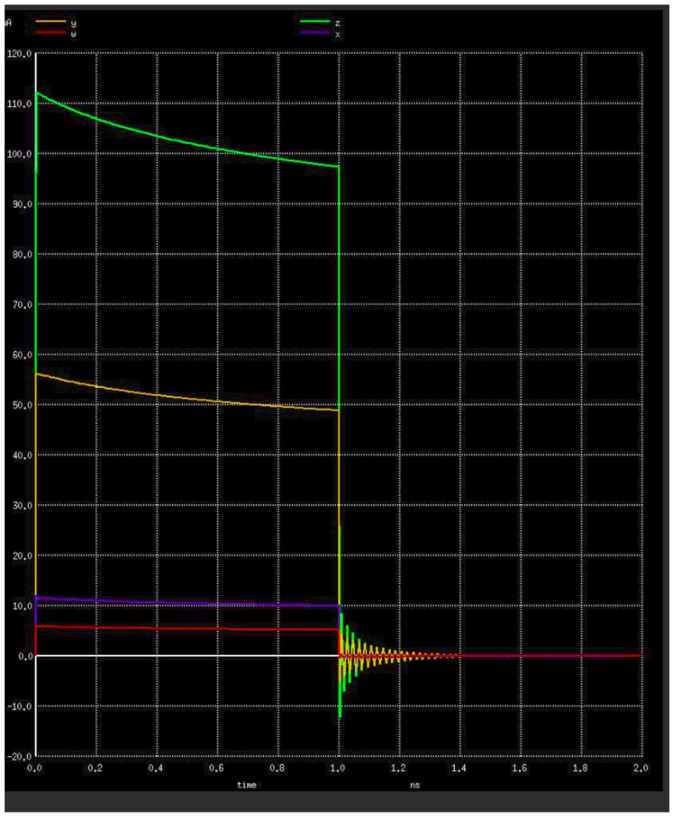


Figure depicts Ioff. W=36, 18, 3.6, 1.8 in decreasing value of peak

Now, we need to find the average current which is done by the average function in the above question

The plot for that is given as follows

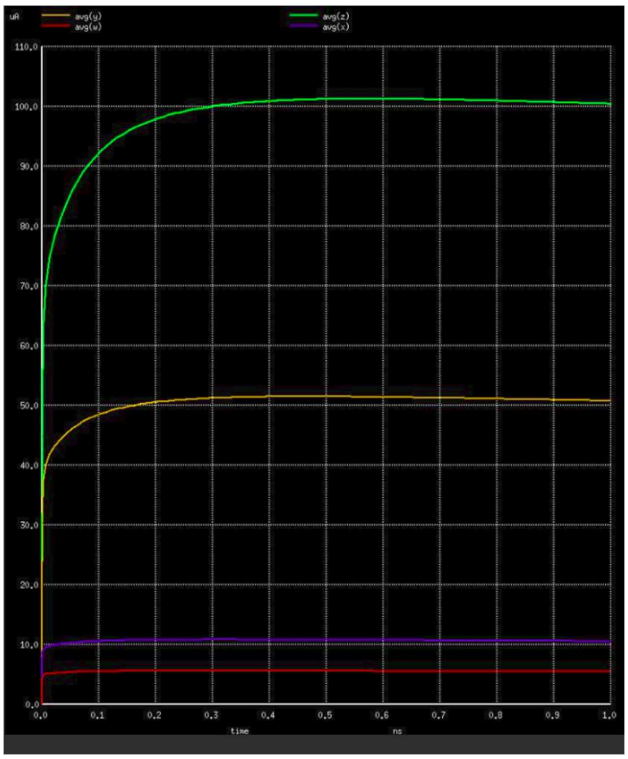


Figure depicts average IOFF values

We get the value for average IOFF as follows

W=1.8 IOFF=5.47uA

W=3.6 IOFF=10.5uA

W=18 IOFF=50.72uA

W=36 IOFF=100.4auA

This plot is linear unlike the previous case where we get a non linear plot.

Since the MOSFET is off, we do not get any effects that might alter the linearity.

Question 6

A)Codes:

```
Netlist to evaluate MOS I-V characterisitics

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param VGG=1.5
.param LAMBDA=0.09u
.param width_N={20*LAMBDA}
.global gnd vdd


Vin in gnd 1.8
*Vin in gnd 0 $This is used for part ii)
VGS G gnd 1.8

M1      in       G       out    gnd  CMOSN   W={width_N}   L={2*LAMBDA}
*+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

C1 out gnd 100f

.ic v(out)=0
*.ic v(out)=1.8 $This is used for part ii)

.tran 0.1n 20u
* .tran 0.1n 10n $This is used for part ii)
.control

run


plot v(out)
```

The above code is for nmos. We have two cases, I) We take a capacitor with no initial charge and a drain voltage

II) We take a fully charged capacitor with mosfet to 0 drain voltage.

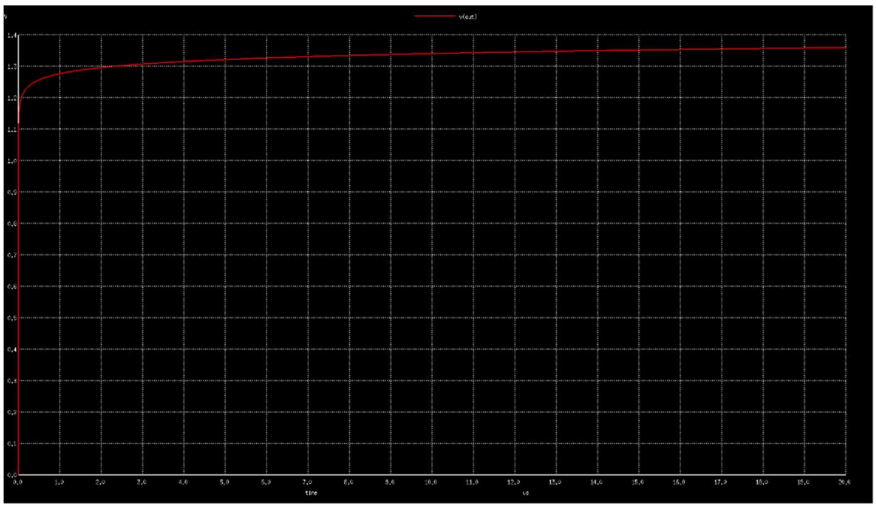


Figure depicts Vc=0 Vin=1.8 initially

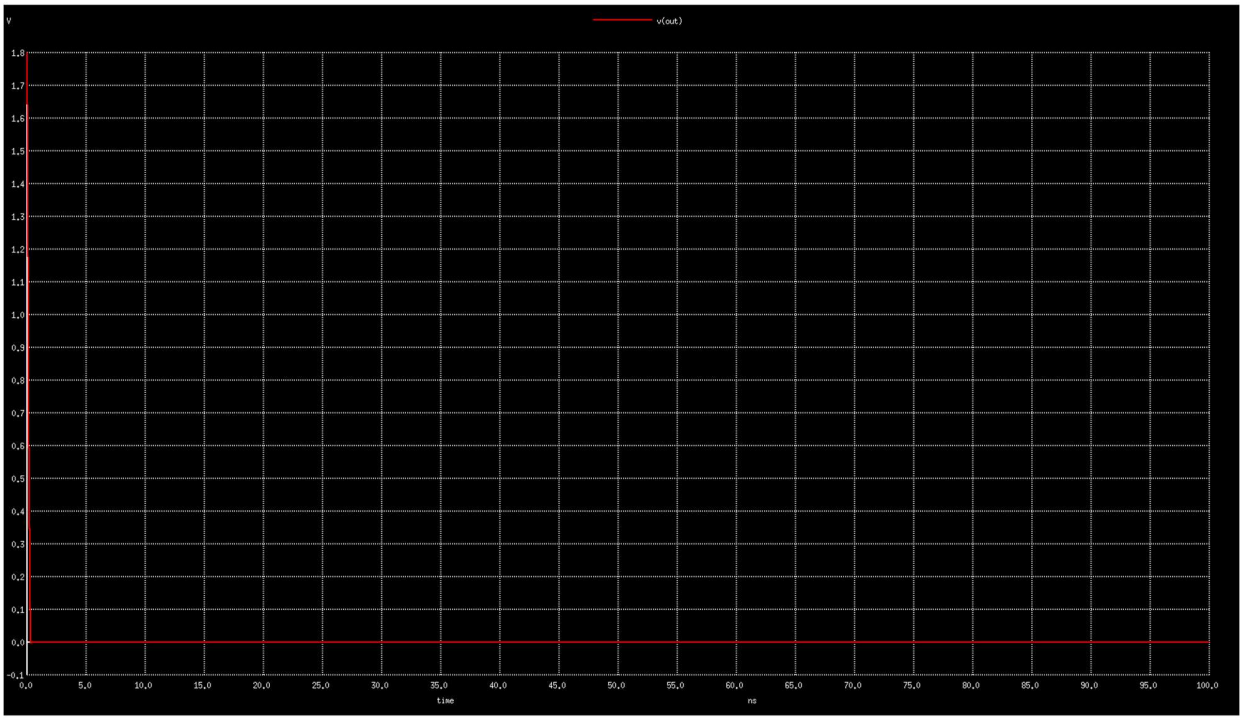


Figure depicts Vc=1.8 Vin=0 initially

For the first case, we have capacitor voltage to be initially 0 and the Vin as 1.8V. So current flows through the mosfet. The graph looks similar to a capacitor charging.

For the second case, we have capacitor voltage to be 1.8 and Vin as 0. Here the mosfet is off. Therefore we have the leakage current through which the discharging of capacitors take place.

We notice that the capacitor does not fully charge but it discharges immediately. So we can say that NMOS is a **pulldown setup**. So we can use nmos as a cmos inverter as well because as capacitor gets charged, source voltage increases pulling the mos from 0 state to 1 state.

```
Netlist to evaluate MOS I-V characterisitics

.include TSMC_180nm.txt
.param SUPPLY=1.8
.param VGG=1.5
.param LAMBDA=0.09u
.param width_N={20*LAMBDA} $PMOS
.global gnd vdd

VGS G gnd 0
VDS S gnd 1.8 $ VIN
VSC D C 0
C1 C gnd 0.1p  $ VOUT
 .ic v(d) = 0
M1 D G S S CMOSP W={width_N} L={2*LAMBDA} AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

*.dc VGS 0 1.8 0.1
.tran 0.1 100n
.control
*set hcopypscolor = 1 *White background for saving plots
*set color0=white
*set color1=black

run

let x = C
let y = VSC#branch
set curplottitle="id vs vgs"
plot x

.endc
```

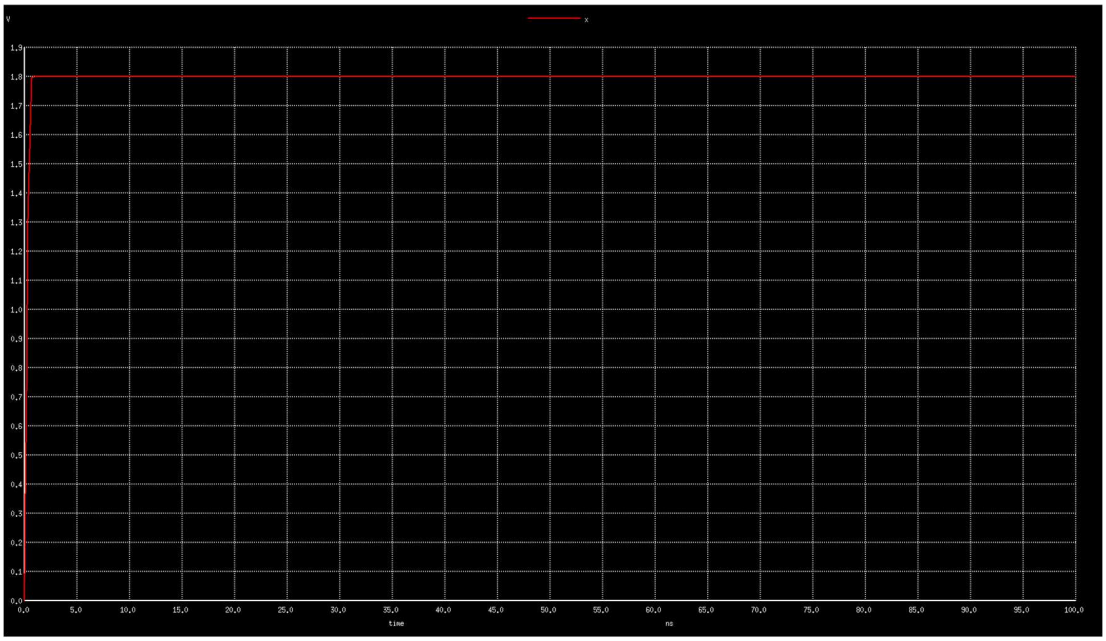


Figure depicts Vc=0 Vin=1.8 initially

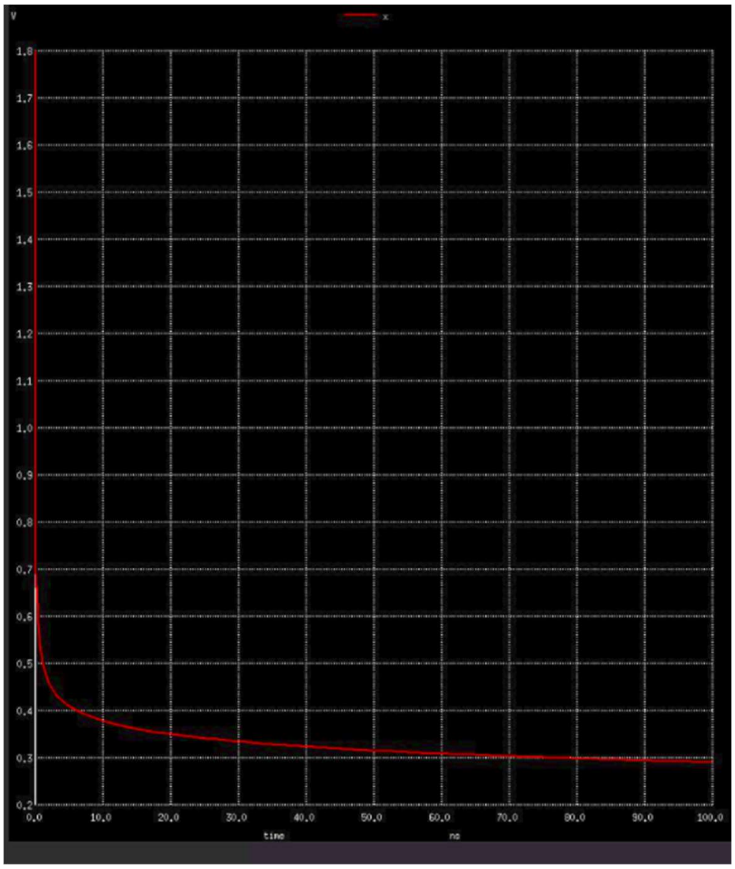


Figure depicts Vc=0 Vin=1.8 initially

The exact reverse happens with the case of pmos. The capacitor cannot discharge completely but can charge instantly. This means that we can use pmos as **a pull up setup**. This is the reason why we can see that pmos is used in cmos inverter. When the capacitor is fully charged, source voltage increases resulting in changing MOSFET from 1 to 0.

Question 7

Code:

```
.param LAMBDA=0.09u
.param width_N=10*LAMBDA
.param width_P=2.5*width_N
.global gnd vdd

Vdd vdd gnd 'SUPPLY'
Vdd1 vdd1 gnd 'SUPPLY'
vin a gnd pulse 0 1.8 0ns 100ps 100ps 9.9ns 20ns

M1 b a gnd gnd CMOSN W={width_N} L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M2 b a vdd vdd CMOSP W={width_P} L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M3 c b gnd gnd CMOSN W={width_N} L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M4 c b vdd1 vdd1 CMOSP W={width_P} L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

Cout c gnd 100f

.tran 0.1n 200n
```

```
.measure tran trise
+TRIG v(c) VAL='SUPPLY/2' RISE=1
+TARG v(a) VAL='SUPPLY/2' FALL=1
.measure tran tfall
+TRIG v(a) VAL='SUPPLY/2' RISE=1
+TARG v(c) VAL='SUPPLY/2' FALL=1
.measure tran tpd param ='(trise+tfall)/2' goal=0

.control
run

set curplottitle="id vs vds"
plot v(a) v(c)
set hcopypscolor = 1 *White background
.endc
~
~
~
~
-- INSERT --                                                    35,50
```

We can change this code directly for the three parts by changing width_N and the value of capacitance. We have ‘measure’ function which we are cleverly using to calculate the values of the rise time and fall time of the pulse so that we can finally calculate the propagation delay.

Plots:

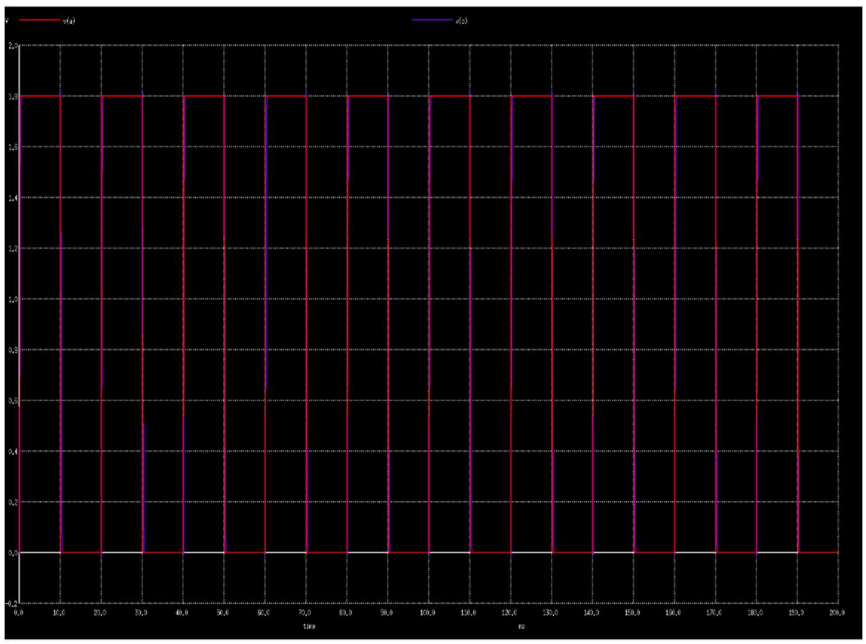


Figure depicts 1.8 u, 100f

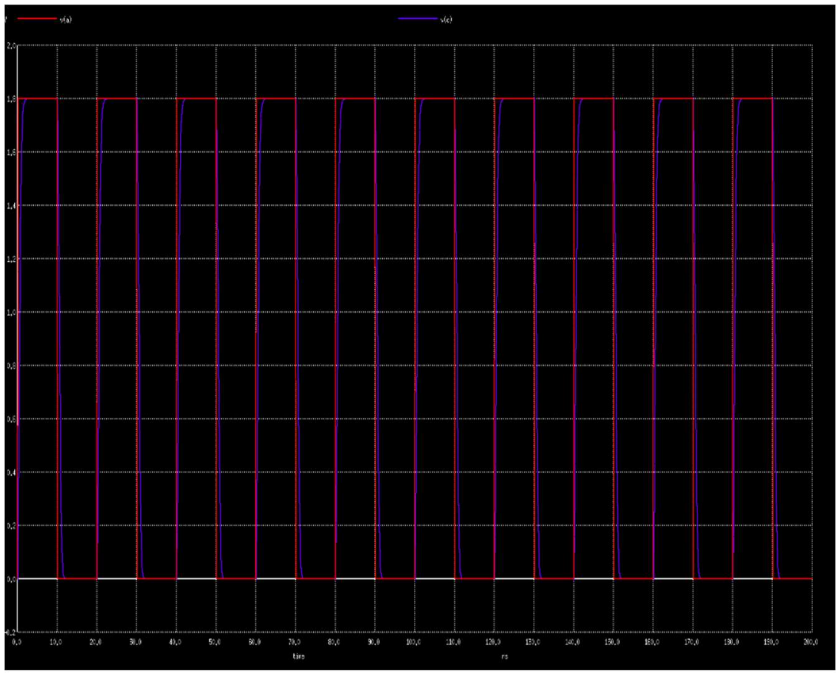


Figure depicts 1.8u, 500f

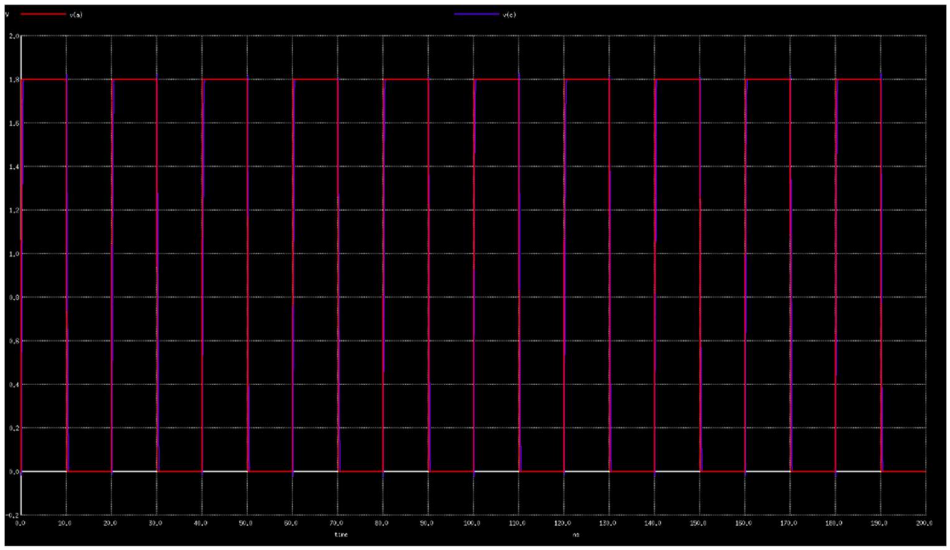


Figure depicts 9u, 500f

Explanation:

Before we actually start defining the entities, let us understand what a few important terms are.

Delay: (Rise time +Fall time)/2

Rise time: It maybe defined as the delay between the rising output and the falling input corresponding to the output

Fall time: It maybe defined as the delay between the falling output and the rising input corresponding to the input

Propagation delay: It maybe defined as the time between the given command and the implemented command.

	Trise	Tfall	Delay
Case 1(1.8, 100f)	9.843 ns	10.169 ns	10.006 ns
Case 2(1.8, 500f)	9.519 ns	10.537 ns	10.028 ns
Case 3(9, 500f)	9.832 ns	10.181 ns	10.006 ns

We know about the capacitances which are of two types basically

One is mos capacitance and the other is the load capacitance. These when changed ensure that the delays are changed. Mos capacitance of the mosfet depends on the area and thus depends directly on W.

Both the relations are directly proportional

Case 1: We have 1.8 and 100f for which we get certain rise time and fall time

Case 2: Here, we increased the capacitance and kept the width same. Due to the increase in capacitance, the load capacitance increases 5 times increasing the delay.

Case 3: Here, the capacitance is 5 times that of the original case and so expect that the delay to increase, however, due to the increase in W, the area increases, decreasing the capacitance of the mosfet and thus the delay comes back to original case.