VLSI Design

Assignment-2 Report

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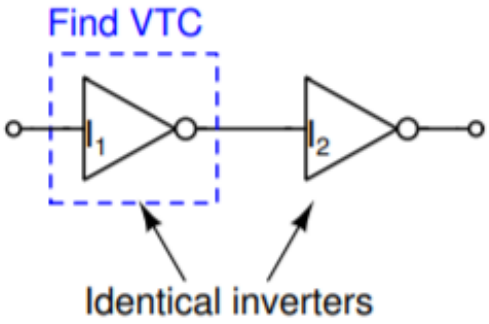
All the netlists, layouts and plots can be viewed by clicking this link

https://iiitaphyd-my.sharepoint.com/:f:/g/personal/sri_surya_students_iiit_ac_in/EmLnsiJXMBVAizC1lx3EffYBMuQoRo1L_qfeaLzK6IwIiQ?e=IFxa3i

Problem-3

Consider a CMOS inverter with size W , which has the following parameters : L = 0.18µm, Wn = W = 1.8µm and Wp = 2.5 × W.

Circuit:



We need to find the voltage tranfer characteristics (VTC) of the first inverter when it is connected in series with an identical second inverter.

First, we are expected to implement the circuit and plot VTC from which we can obtain the 'Noise margins'

Then we need to plot the layout in MAGIC for which we extract the NGSpice code and obtain the VTC and compare the two cases.

Theory:

We know that when we sweep the input voltage(Gate voltage) of the inverter from 0V to 1.8V, the MOSFETs pass through many stages.

Input	PMOS	NMOS	Output
$0<V_{in}<V_{tn}$	Linear	Cutoff	V_{DD}
$V_{tn}<V_{in}<V_i$	Linear	Saturation	Gradual Decrease
$V_i\{=(V_{DD}+V_{tn}-\|V_{tp}\|)/2\}$	Saturation	Saturation	Rapid decrease
$V_i<V_{in}<V_{DD}-\|V_{tp}\|$	Saturation	Linear	Gradual Decrease
$V_{DD}-\|V_{tp}\|<V_{in}<V_{DD}$	Cutoff	Linear	0

NOISE Margin:

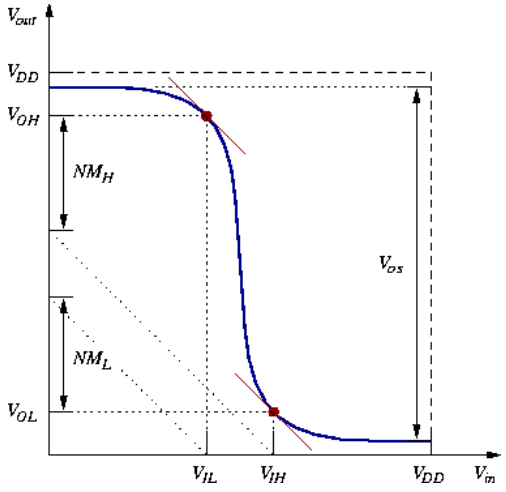
We can safely say that a state is low or high depending on the values on certain parameters.

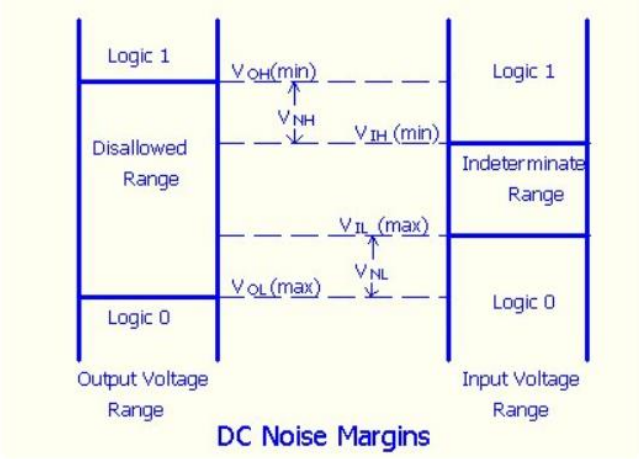
V_{IL}- Maximum input that can as be considered as 'low'

V_{OH}-Minimum output that can be considered as 'high'

V_{IH}- Minimum input that can be considered as 'high'

V_{OL}- Maximum input that can be considered as 'low'





(V_{IL}, V_{OH}) and (V_{IH}, V_{OL}) are the two critical points which are the points where dVout/dVin=-1

If the logic state of the input is intermediate(neither high not low), it leads to errors as we can't predict the exact logic state of the output.

We define the noise margins to be

$NM_H=V_{OH}-V_{IH}$

$NM_L=V_{IL}-V_{OL}$

Netlist (Pre-layout):

```
Third question
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param width_N=20*LAMBDA
.param width_P=2.5*width_N
.global gnd vdd

Vdd vdd gnd 'SUPPLY'
Vdd1 vdd1 gnd 'SUPPLY'
vGS a gnd 'SUPPLY'

M1 b a gnd gnd CMOSN W={width_N} L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M2 b a vdd vdd CMOSP W={width_P} L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}

M3 c b gnd gnd CMOSN W={width_N} L={2*LAMBDA}
+ AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M4 c b vdd vdd CMOSP W={width_P} L={2*LAMBDA}
+ AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}


.dc VGS 0 1.8 0.01

.control
run

set curplottitle="SuryaSasanka_2019102036"
plot v(a) v(b)
let volt=v(b)
plot deriv(volt)
set hcopypscolor = 1 *White background
hardcopy q3preplot.eps v(a) v(b)
.endc
```

The netlist is self explanatory where we implement the two CMOS inverters. The circuit is implemented. The input of the first inverter is 'a' and its output is 'b'(This acts as input for second inverter). We plot V(b) and V(a).Then we have also taken derivative of the V(b) with respect to V(a) and plotted it.

Plot (Pre-layout)

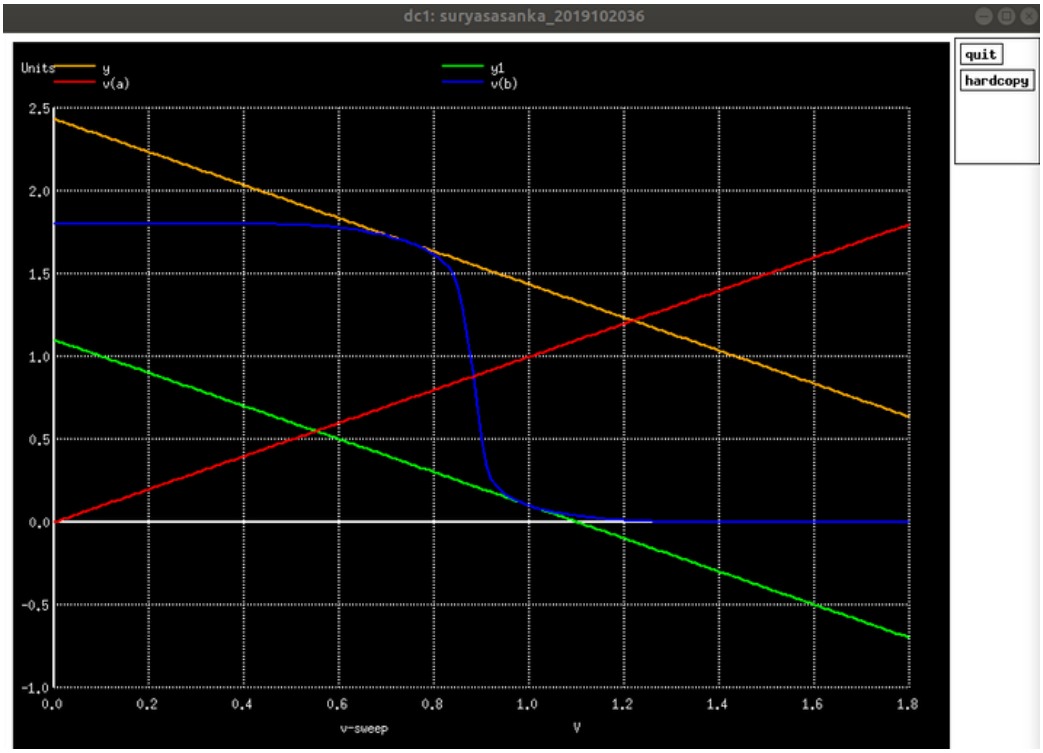


Figure 1

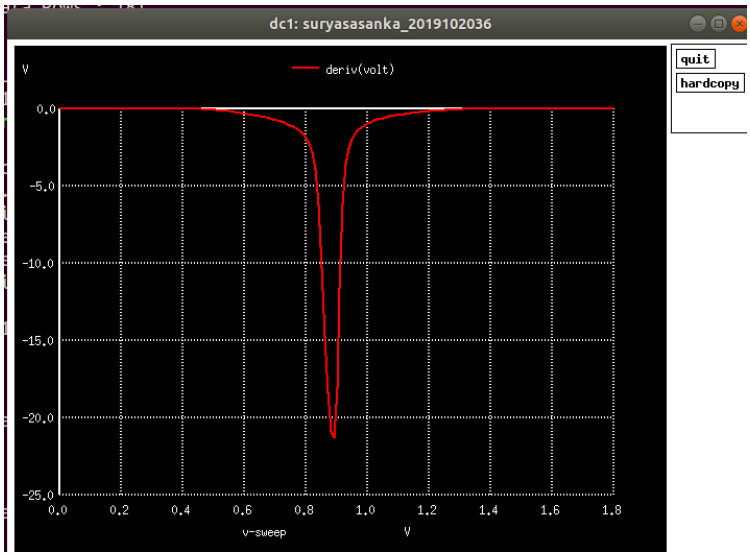


Figure2

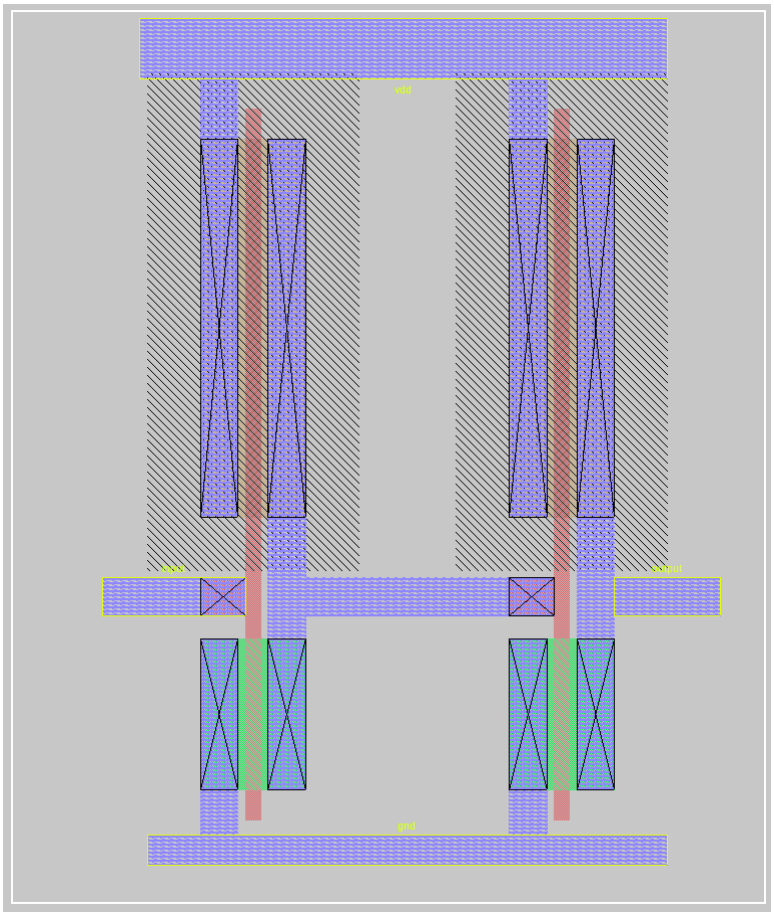
Figure-1 represents the pre-layout VTC of the first inverter

- blue line -voltage transfer characteristics(V_{out})
- red line - input voltage (V_{in})
- parallel lines -The tangents with slope -1
- points of intersection of tangents and V_{out} - (V_{IL}, V_{OH}) and (V_{IH}, V_{OL}).

Figure-2 represents the dV_{out}/dV_{in}

The VTC plot is in accordance with the theory mentioned earlier. Note that the tangents are not intuitive. The derivative plot is observed, the x coordinate corresponding to the slopes -1 are noted. Then (x1, y1) and (x2, y2) are obtained from which the tangent equations are added into the netlist.

Magic layout



Parameters:

- Length of the MOSFET- (2 * lambda). Can be found from width of polysilicon
- Width of P-MOSFET - (50 * lambda). Can be found from pdiffusion layer (14X50 lambda)
- Width of N-MOSFET - (20 * lambda). Can be found from ndiffusion layer (14X20 lambda)

In the above figure, we have two identical inverters. They have common Vdd(at the top) and common ground(at the bottom). We have pmos at the top and nmos at the bottom in both the inverters. The input is at the middle left which is the gate voltage of the first cmos inverter. The voltage that we are interested is the voltage of the middle joint connecting inverter 1 and 2.

Netlist(Post-layout):

```
* SPICE3 file created from q3.ext - technology: scmos

.include TSMC_180nm.txt
.param SUPPLY=1.8
.global gnd vdd
.option scale=0.09u

Vdd vdd gnd 'SUPPLY'
VGS a gnd 'SUPPLY'

M1 b a gnd Gnd CMOSN w=20 l=2
+  ad=120 pd=52 as=240 ps=104
M2 b a vdd vdd CMOSP w=50 l=2
+  ad=300 pd=112 as=600 ps=224
M3 c b gnd Gnd CMOSN w=20 l=2
+  ad=120 pd=52 as=0 ps=0
M4 c b vdd vdd CMOSP w=50 l=2
+  ad=300 pd=112 as=0 ps=0

C0 vdd vdd 0.12fF
C1 a b 0.07fF
C2 b vdd 0.52fF
C3 vdd b 0.08fF
C4 c vdd 0.08fF
C5 a vdd 0.08fF
C6 vdd vdd 0.12fF
```

```
C7 c b 0.07fF
C8 c vdd 0.52fF
C9 gnd b 0.31fF
C10 gnd a 0.07fF
C11 c gnd 0.24fF
C12 vdd b 0.08fF
C13 gnd Gnd 0.52fF
C14 c Gnd 0.11fF
C15 vdd Gnd 0.04fF
C16 b Gnd 0.31fF
C17 vdd Gnd 1.86fF
C18 a Gnd 0.20fF
C19 vdd Gnd 1.86fF

.dc VGS 0 1.8 0.01

.control
run

set curplottitle="SuryaSasanka_2019102036"
plot v(a) v(b)
let volt=v(b)
plot deriv(volt)
set hcopypscolor = 1 *White background
hardcopy q3postplot.eps v(a) v(b)
.endc
```

We notice a number of parasitic capacitances in the extracted netlist in addition to the inverter circuit. We make appropriate changes to this extracted netlist and then again plot the VTC of the first inverter.

Plot (Post-layout)

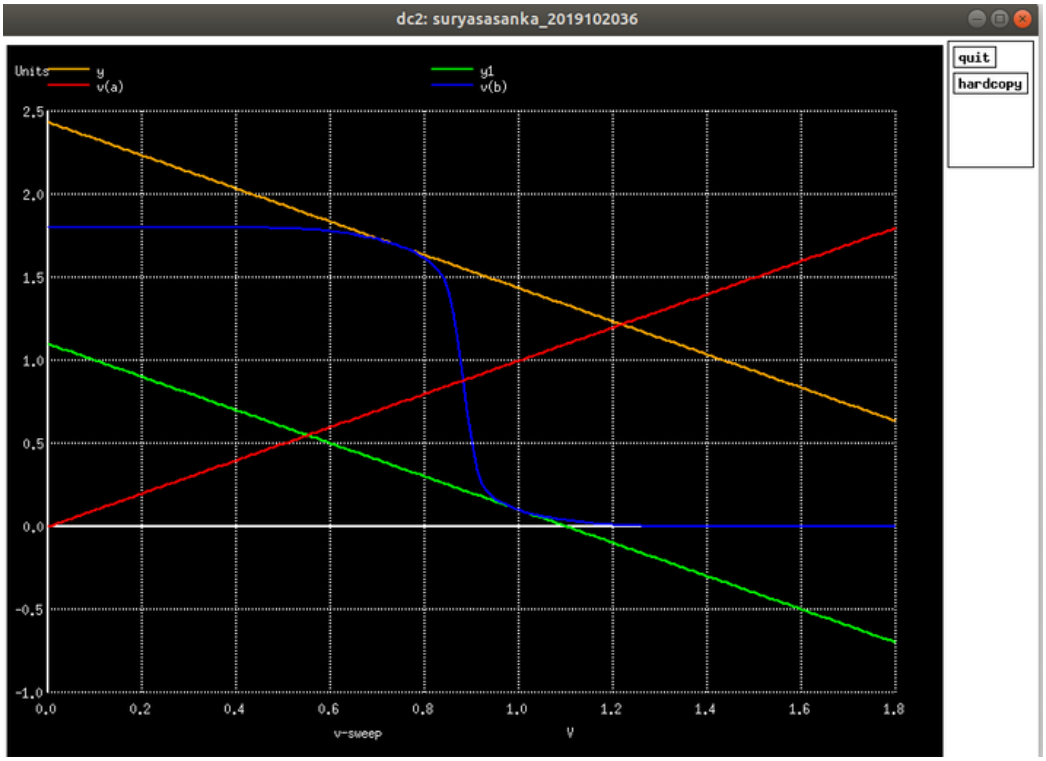


Figure3

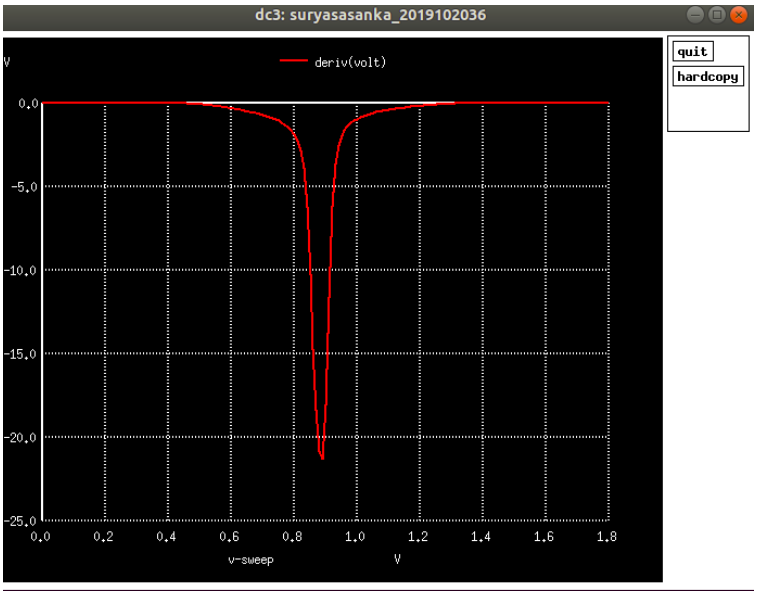


Figure4

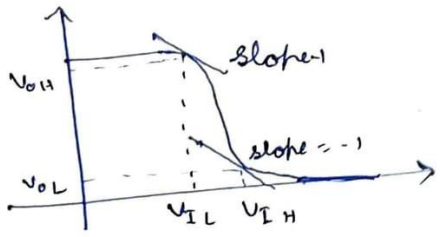
Figure-3 represents the post-layout VTC of the first inverter

- blue line -voltage transfer characteristics(V_{out})
- red line - input voltage (V_{in})
- parallel lines -The tangents with slope -1
- points of intersection of tangents and V_{out} - (V_{IL}, V_{OH}) and (V_{IH}, V_{OL}).

Figure-4 represents the dV_{out}/dV_{in}

The post-layout VTC plot has the expected shape. Though the pre-layout plot and post-layout plot appear the same to the naked eye, there is a small difference (of the order 10^-3 V) in the plots when we zoom them. The observed values support our claims.

b) calculation of NM_H, NM_L



We know that $NM_H = V_{OH} - V_{IH}$

$NM_L = V_{IL} - V_{OL}$

i) (V_{IL}, V_{OH})

Here nmos is in saturation
pmos is in linear
Equating the currents

$$\frac{k_n}{2}(v_i - v_{tn})^2 = k_p(V_{DD} - v_i - |v_{tp}|)(V_{DD} - v_o) - \frac{k_p}{2}(V_{DD} - v_o)^2$$

We can make $k_n = k_p$ $\left(\mu_n C_{ox}\left(\frac{W}{L}\right)_n = \mu_p C_{ox}\left(\frac{W}{L}\right)_p\right)$
by appropriately changing $\left(\frac{W}{L}\right)_n$ and $\left(\frac{W}{L}\right)_p$.

$$\Rightarrow \frac{1}{2}(V_i - V_{tn})^2 = (V_{DD} - V_i - |V_{tp}|)\left[(V_{DD} - V_o) - \frac{1}{2}(V_{DD} - V_o)^2\right]$$

take $V_{DD} - V_o = x$

$$x^2 - 2x(V_{DD} - V_i - |V_{tp}|) + (V_i - V_{tn})^2 = 0$$

$$x = 2(V_{DD} - V_i - |V_{tp}|) \pm \sqrt{4(V_{DD} - V_i - |V_{tp}|)^2 - 4(V_i - V_{tn})^2}$$

$$= (V_{DD} - V_i - |V_{tp}|) \pm \sqrt{(V_{DD} - V_i - |V_{tp}|)^2 - (V_i - V_{tn})^2}$$

$$\Rightarrow V_o = (V_i + |V_{tp}|) + \sqrt{(V_{DD} - V_{tn} - |V_{tp}|)(V_{DD} - 2V_i + V_{tn} - |V_{tp}|)}$$

$$\frac{\partial V_o}{\partial V_i} = -1 \qquad \text{— (1)}$$

$$\Rightarrow -1 = 1 + \frac{\sqrt{V_{DD} - V_{tn} - |V_{tp}|} \times -2}{2\sqrt{V_{DD} - 2V_i + V_{tn} - |V_{tp}|}}$$

$$\Rightarrow 4 = \frac{V_{DD} - V_{tn} - |V_{tp}|}{V_{DD} - 2V_i + V_{tn} - |V_{tp}|}$$

$$\Rightarrow \boxed{V_i = \frac{3V_{DD} + 5V_{tn} - 3|V_{tp}|}{8}} \quad (V_{IL})$$

Now substituting this in (1).

$$v_o = \frac{3V_{DD} + 5V_{tn} - 3|V_{tp}|}{8} + |V_{tp}|$$

$$+ \sqrt{(V_{DD} - V_{tn} - |V_{tp}|)\left(V_{DD} + V_{tn} - |V_{tp}| - \left(\frac{6V_{DD} + 10V_{tn} - 6|V_{tp}|}{8}\right)\right)}$$

$$= \frac{3V_{DD} + 5V_{tn} + 5|V_{tp}|}{8} + \sqrt{(V_{DD} - V_{tn} - |V_{tp}|)\left(\frac{V_{DD} - 0V_{tn} - |V_{tp}|}{4}\right)}$$

$$= \frac{3V_{DD} + 5V_{tn} + 5|V_{tp}|}{8} + \frac{V_{DD} - V_{tn} - |V_{tp}|}{2}$$

$$\boxed{v_o = \frac{7V_{DD} + V_{tn} + |V_{tp}|}{8} \quad (V_{OH})}$$

ii) (V_{IH}, V_{OL})

Here nmos is in linear
pmos is in saturation.

Equating currents

$$k_n\left((V_i - V_{th})V_o - \frac{V_o^2}{2}\right) = \frac{k_p}{2}\left(V_{DD} - V_i - |V_{tp}|\right)^2$$

Here also take $k_n = k_p$

$$\frac{V_o^2}{2} - (V_i - V_{tn})V_o + \frac{1}{2}(V_{DD} - V_i - |V_{tp}|)^2 = 0$$

$$\Rightarrow V_o = \frac{2(V_i - V_{tn}) \pm \sqrt{4(V_i - V_{tn})^2 - 4(V_{DD} - V_i - |V_{tp}|)^2}}{2}$$

Taking the required solution, which satisfies the initial condition

$$V_o = -(V_i - V_{tn}) - \sqrt{(V_{DD} - V_{tn} - |V_{tp}|)(2V_i - V_{DD} - V_{tn} + |V_{tp}|)} \quad \text{---(2)}$$

$$\frac{\partial V_o}{\partial V_i} = -1$$

$$\Rightarrow -1 = -1 - \frac{\sqrt{V_{DD} - V_{tn} - |V_{tp}|}}{\sqrt{2V_i - V_{DD} - V_{tn} + |V_{tp}|}}$$

$$\Rightarrow 4 = \frac{V_{DD} - V_{tn} - |V_{tp}|}{2V_i - V_{DD} - V_{tn} + |V_{tp}|}$$

$$\Rightarrow \boxed{V_{IH} = \frac{5V_{DD} + 3V_{tn} - 5|V_{tp}|}{8}}$$

Substitute this in (2)

$$V_o = \frac{5V_{DD} - 5V_{tn} - 5|V_{tp}|}{8} - \sqrt{(V_{DD} - V_{tn} - |V_{tp}|)\left(\frac{10V_{DD} + 6V_{tn} - 10|V_{tp}|}{8} - V_{DD} - V_{tn} + |V_{tp}|\right)}$$

$$\Rightarrow V_o = \frac{5V_{DD} - 5V_{tn} - 5|V_{tp}|}{8} - \sqrt{\left(V_{DD} - V_{tn} - |V_{tp}|\right)\left(\frac{V_{DD} - V_{tn} - |V_{tp}|}{4}\right)}$$

$$= \frac{5V_{DD} - 5V_{tn} - 5|V_{tp}|}{8} - \left(\frac{V_{DD} - V_{tn} - |V_{tp}|}{2}\right)$$

$$V_o \; (V_{OL}) = \frac{V_{DD} - V_{tn} - |V_{tp}|}{8}$$

Now,

$$NM_H = V_{OH} - V_{IH} = \frac{V_{DD} - V_{tn} + 3|V_{tp}|}{4}$$

$$NM_L = V_{IL} - V_{OL} = \frac{V_{DD} + 3V_{tn} - |V_{tp}|}{4}$$

c) $(V_{IH}, V_{IL}, V_{OH}, V_{OL})$

From Pre layout VTC graphs values are

(0.9947, 0.7423, 1.694, 0.1072)

$NM_H = 1.694 - 0.9947$

$\Rightarrow \boxed{NM_H = 0.6993V}$

$NM_L = 0.7423 - 0.1072$

$\Rightarrow \boxed{NM_L = 0.6351\ V}$

Theoritical values:

$V_{DD} = 1.8$; $V_{tn} = 0.54$; $V_{tp} = -0.45$

From the calculated formulas above, we get

$V_{IH} = 1.04625$

$V_{IL} = 0.84375$

$V_{OH} = 1.69875$

$V_{OL} = 0.10125$

$\Rightarrow (1.04625, 0.84375, 1.69875, 0.10125)$

$NM_H = 1.69875 - 1.04625$

$\Rightarrow \boxed{NM_H = 0.6525\ V}$

$NM_L = 0.84375 - 0.10125$

$\Rightarrow \boxed{NM_L = 0.7425V}$

Post layout values:

$(0.9915, 0.7486, 1.6896, 0.1037)$

$NM_H = 1.6896 - 0.9915$

$\Rightarrow \boxed{NM_H = 0.6981V}$

$NM_L = 0.7486 - 0.1037$

$\Rightarrow \boxed{NM_L = 0.6449V}$

	V_{IH}	V_{IL}	V_{OH}	V_{OL}	N_{MH}	N_{ML}
Theoretical	1.04625	0.84375	1.69875	0.10125	0.6525	0.7425
Pre-layout	0.9947	0.7423	1.694	0.1072	0.6993	0.6351
Post-layout	0.9915	0.7486	1.6896	0.1037	0.6981	0.6449

Difference between pre-layout values and theoretical values

We notice that there is a maximum difference of 0.04V in the theory values and pre-layout values. While calculating the theory values, we have taken Kn=Kp. => $u_nc_{ox}(W/L)_n = u_pc_{ox}(W/L)_p$ and $(W/L)_p = 2.5*(W/L)_n$

=> $u_nc_{ox} = 2.5 * u_pc_{ox}$

This is not true in the case of simulation because for that in simulation, we observed in the last assignment we got approximately $u_nc_{ox} \sim 2.7 * u_pc_{ox}$.

=> Kn is slightly greater than Kp

So due to that we get a difference in the pre-layout and theoretical values.

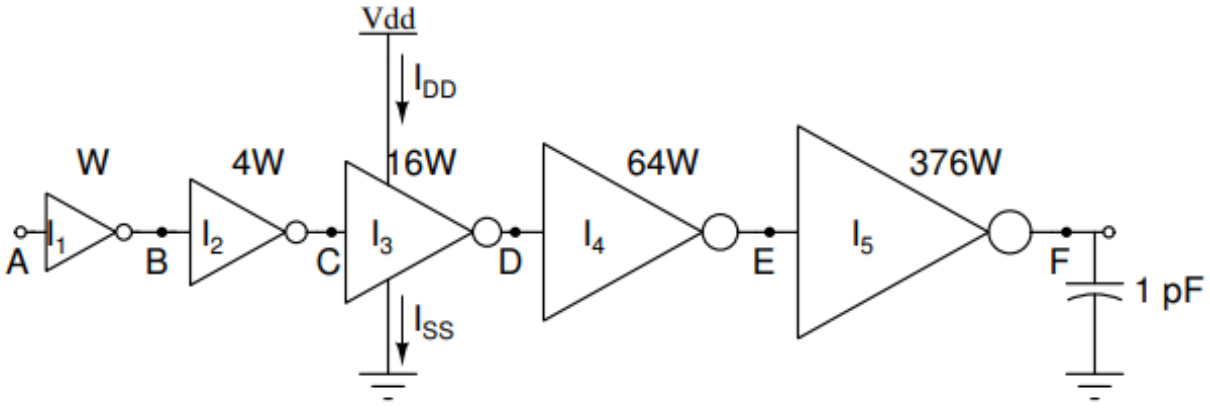
Difference between pre-layout values and post-layout values

We have noticed a maximum difference of 0.009 V in pre-layout and post-layout values. This is due to parasitic capacitances that we have ignored in the pre-layout netlist. After we have extracted the netlist from the magic layout we have noticed 20 parasitic capacitances. These capacitances can be of many types which are Capacitance of the wire(This is because wire is designed as metal), Self-capacitance(This is because of parasitic capacitance between gate-body, drain-body etc). But these values are very small and in the order of femto Farad(10^-15) and do not affect the value hugely. Incase we use more complex circuits, these capacitances add up and cause huge deviations.

Problem-4

We need to characterize the delay of a FO4 inverter with the following parameters : L = 0.18µm, Wn = W = 1.8µm and Wp = 2.5 × W. The W for the different inverters is changed. Input to the first node is Vin vin A 0 pwl (0 0V 0.5ns 1.8V 1.1ns 1.8V 1.5ns 0V 10ns 0V) .

Circuit:



- We need to derive the T_{rise} and T_{fall} expression manually and calculate Kp*Trise/C, Kn*Tfall/C
- We need to write the netlist for the 5 inverters and add a capacitor in the end. Then we need to calculate the Trise and Tfall at nodes C and D.
- We need to calculate the propagation delays, Tpd at inverter I3 and I4.
- Finally we need to plot the Idd and Iss.

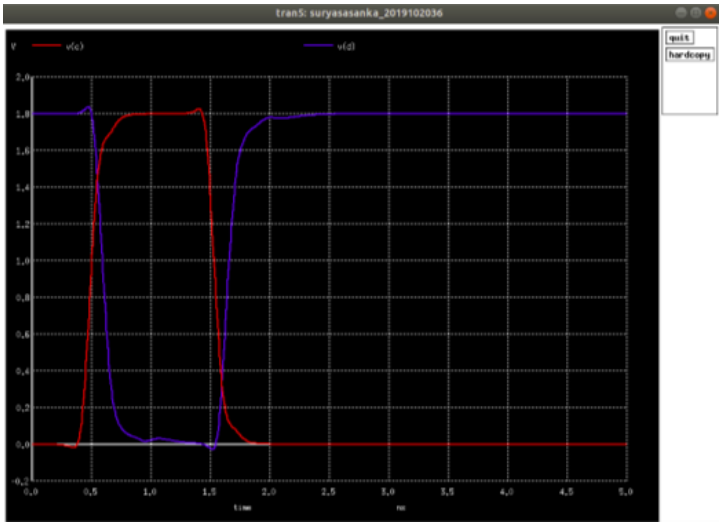
Netlist:

```
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param width_N1=20*LAMBDA
.param width_P1=2.5*width_N1
.param width_N2=4*width_N1
.param width_P2=2.5*width_N2
.param width_N3=16*width_N1
.param width_P3=2.5*width_N3
.param width_N4=64*width_N1
.param width_P4=2.5*width_N4
.param width_N5=376*width_N1
.param width_P5=2.5*width_N5

.global gnd vdd

Vdd vdd gnd 'SUPPLY'
VDS D1 gnd 1.8
VDS1 gnd S1 0
VGS in gnd pwl (0 0V 0.5ns 1.8V 1.1ns 1.8V 1.5ns 0V 10ns 0V)

M1 b in gnd gnd CMOSN W={width_N1} L={2*LAMBDA}
+ AS={5*width_N1*LAMBDA} PS={10*LAMBDA+2*width_N1} AD={5*width_N1*LAMBDA} PD={10*LAMBDA+2*width_N1}

M2 b in vdd vdd CMOSP W={width_P1} L={2*LAMBDA}
+ AS={5*width_P1*LAMBDA} PS={10*LAMBDA+2*width_P1} AD={5*width_P1*LAMBDA} PD={10*LAMBDA+2*width_P1}

M3 c b gnd gnd CMOSN W={width_N2} L={2*LAMBDA}
+ AS={5*width_N2*LAMBDA} PS={10*LAMBDA+2*width_N2} AD={5*width_N2*LAMBDA} PD={10*LAMBDA+2*width_N2}

M4 c b vdd vdd CMOSP W={width_P2} L={2*LAMBDA}
+ AS={5*width_P2*LAMBDA} PS={10*LAMBDA+2*width_P2} AD={5*width_P2*LAMBDA} PD={10*LAMBDA+2*width_P2}
                                                                                15,0-1        2%
```

```
M5 d c gnd gnd CMOSN W={width_N3} L={2*LAMBDA}
+ AS={5*width_N3*LAMBDA} PS={10*LAMBDA+2*width_N3} AD={5*width_N3*LAMBDA} PD={10*LAMBDA+2*width_N3}

M6 d c vdd vdd CMOSP W={width_P3} L={2*LAMBDA}
+ AS={5*width_P3*LAMBDA} PS={10*LAMBDA+2*width_P3} AD={5*width_P3*LAMBDA} PD={10*LAMBDA+2*width_P3}

M7 e d gnd gnd CMOSN W={width_N4} L={2*LAMBDA}
+ AS={5*width_N4*LAMBDA} PS={10*LAMBDA+2*width_N4} AD={5*width_N4*LAMBDA} PD={10*LAMBDA+2*width_N4}

M8 e d vdd vdd CMOSP W={width_P4} L={2*LAMBDA}
+ AS={5*width_P4*LAMBDA} PS={10*LAMBDA+2*width_P4} AD={5*width_P4*LAMBDA} PD={10*LAMBDA+2*width_P4}

M9 f e gnd gnd CMOSN W={width_N5} L={2*LAMBDA}
+ AS={5*width_N5*LAMBDA} PS={10*LAMBDA+2*width_N5} AD={5*width_N5*LAMBDA} PD={10*LAMBDA+2*width_N5}

M10 f e vdd vdd CMOSP W={width_P5} L={2*LAMBDA}
+ AS={5*width_P5*LAMBDA} PS={10*LAMBDA+2*width_P5} AD={5*width_P5*LAMBDA} PD={10*LAMBDA+2*width_P5}

Cout f gnd 1pf

.tran 10p 5n

.control
run

set curplottitle="suryasasanka_2019102036"
plot v(c) v(d)
set hcopypscolor = 1 *White background
hardcopy q4aplot.eps v(c) v(d)
.endc
                                                                                58,0-1
```

In the above netlist, we implemented the 5 inverter along with the capacitor. We have given the input to the first inverter as the piece wise linear waveform. We have defined the widths of the inverters as mentioned in the question. Then we have plotted the voltages at C and D points in the circuit (i.e V(c) and V(d))

Plot:



Blue line- Voltage at node C

Red line- Voltage at node D

We notice that the plot is as expected because it is of an inverter. When the input voltage inverter I3(V(C)) is low, the output voltage of I3 (V(D)) is high and vice versa.

Theory(To calculate T_{rise} and T_{fall}):

Rise time (T_{rise}) – It is defined as the time taken for the positive edge of the input to rise from minimum value to maximum value.

Fall time(T_{fall}) – It is defined as the time taken for the negative edge of the input to fall from the maximum value to minimum value.

We need to know about these dynamic characteristics of the inverter for good operation as operating it in this region makes it difficult to predict the logic state and also gives non-zero power in that region.

Sometimes, the value of the capacitance maybe large, so the complete charging and discharging might take a lot of time. To avoid this problem we take the rise time as time taken for the voltage to rise from 10% to 90% of the supply voltage whereas the fall time is the time taken for the voltage to fall from 90% to 10% of the supply voltage.

Netlist (To calculate T_{rise} and T_{fall}):

```
.measure tran tpdr_c
+ TRIG v(c) VAL='SUPPLY/10' RISE=1
+ TARG v(c) VAL='9*SUPPLY/10' RISE=1

.measure tran tpdf_c
+ TRIG v(c) VAL='9*SUPPLY/10' FALL=1
+ TARG v(c) VAL='SUPPLY/10' FALL=1

.measure tran tpdr_d
+ TRIG v(d) VAL='SUPPLY/10' RISE=1
+ TARG v(d) VAL='9*SUPPLY/10' RISE=1

.measure tran tpdf_d
+ TRIG v(d) VAL='9*SUPPLY/10' FALL=1
+ TARG v(d) VAL='SUPPLY/10' FALL=1
```

We have cleverly used the '.measure' function to calculate the Trise and Tfall of the nodes C and D.

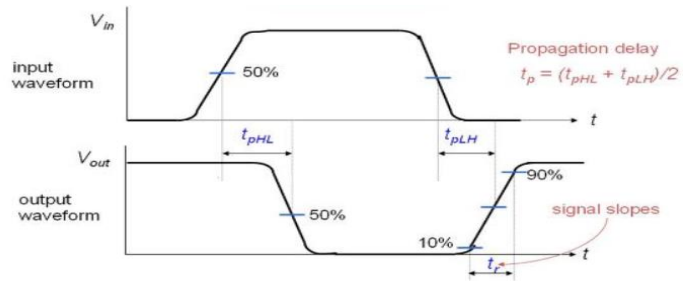
To calculate the rise time, we have calculated the time at which the input voltage is at 10% of the supply using TRIG, then calculated the time when the input voltage is 90% of the supply using TARG. Then T_{rise}=TRIG-TARG. Using similar approach we calculate T_{fall}. The same procedure is used for nodes C and D.

Theory(To calculate T_{pd}):

Propagation delay- It is defined as the delay in time taken for the output to switch after changing the input. Mathematically, it is defined as the average of the high-low propagation delay and low-high propagation delay.

Tpdr(High-low pd): It is the time elapsed between the output reaching 50% from 0 after the input reaches 50% from Vdd.

Tpdf(Low-high pd): It is the time elapsed between the output reaching 50% from Vdd after the input reaches 50% from 0.



Netlist (To calculate T_{pd}):

```
.measure tran Tpdr3
+ TRIG v(c) VAL='SUPPLY/2' FALL=1
+ TARG v(d) VAL='SUPPLY/2' RISE=1

.measure tran Tpdf3
+ TRIG v(c) VAL='SUPPLY/2' RISE=1
+ TARG v(d) VAL='SUPPLY/2' FALL=1

.measure tran tpd3 param='(Tpdr3+Tpdf3)/2' goal=0

.measure tran Tpdr4
+ TRIG v(d) VAL='SUPPLY/2' FALL=1
+ TARG v(e) VAL='SUPPLY/2' RISE=1

.measure tran Tpdf4
+ TRIG v(d) VAL='SUPPLY/2' RISE=1
+ TARG v(e) VAL='SUPPLY/2' FALL=1

.measure tran tpd4 param='(Tpdr4+Tpdf4)/2' goal=0
```

We use the '.measure' function to calculate the time.

The TRIG is used to start the time count when input is SUPPLY/2 (and is falling) and TARG is to end the time count when output is SUPPLY/2(and is rising) to calculate the Tpdr.

The TRIG is used to start the time count when input is SUPPLY/2 (and is rising) and TARG is to end the time count when output is SUPPLY/2(and is falling) to calculate the Tpdf.

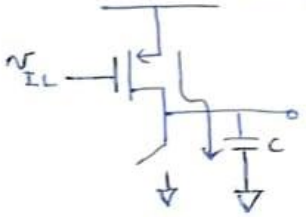
Results(in terminal):

```
  Measurements for Transient Analysis

tr_c                =  1.647124e-10 targ=  5.882254e-10 trig=  4.235131e-10
tf_c                =  1.563435e-10 targ=  1.625228e-09 trig=  1.468884e-09
tr_d                =  1.801530e-10 targ=  1.756253e-09 trig=  1.576100e-09
tf_d                =  1.640233e-10 targ=  6.935144e-10 trig=  5.294911e-10
tpdr3               =  1.092863e-10 targ=  1.644951e-09 trig=  1.535665e-09
tpdf3               =  1.068900e-10 targ=  5.979614e-10 trig=  4.910714e-10
tpd3                =  1.08088e-10
tpdr4               =  1.845303e-10 targ=  7.824916e-10 trig=  5.979614e-10
tpdf4               =  1.649269e-10 targ=  1.809878e-09 trig=  1.644951e-09
tpd4                =  1.74729e-10
```

Derivations:

Assume that only one transistor is on at a particular time

i) PMOS On. NMOS Off.



T_{rise} is the time taken by capacitor to charge from 0 to V_{OH}

$$I_{dsp} = \frac{C\, dv_o}{dt}$$

Note that P-MOS is in ~~linear~~ saturation region initially and changes to linear at $V_{IL} + |V_{tp}|$

$$\Rightarrow dt = \frac{C\, dv_o}{I_{dsp}}$$

$$\Rightarrow \frac{1}{C}\int_0^{T_{rise}} dt = \int_0^{V_{OH}} \frac{dv_o}{I_{dsp}}$$

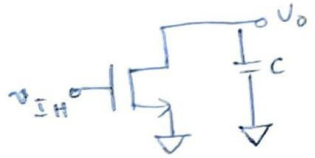
$$\Rightarrow \frac{T_{rise}}{C} = \int_0^{V_{IL}+|V_{TP}|} \frac{dv_o}{I_{dp\,sat}} + \int_{V_{IL}+|V_{TP}|}^{V_{OH}} \frac{dv_o}{I_{dp\,linear}}$$

$$= \int_0^{V_{IL}+|V_{TP}|} \frac{dv_o}{\frac{K_p}{2}(V_{DD}-V_i-|V_{TP}|)^2} + \int_{V_{IL}+|V_{TP}|}^{V_{OH}} \frac{dv_o}{K_p\left((V_{DD}-V_i-|V_{tp}|)(V_{DD}-v_o) - \frac{(V_{DD}-V_o)^2}{2}\right)}$$

$$\Rightarrow \boxed{\frac{K_p T_{rise}}{C} = \frac{2(V_{IL}+|V_{TP}|)}{(V_{DD}-V_{IL}-|V_{TP}|)^2} + \frac{1}{(V_{DD}-V_{IL}-|V_{TP}|)} \ln\left(\frac{V_{DD}+V_{OH}-2V_{IL}-2|V_{TP}|}{V_{DD}-V_{OH}}\right)}$$

Calculating, we get $\boxed{\frac{K_p T_{rise}}{C} = 13.21}$

ii) NMOS on PMOS off



T_{fall} – Time taken for the capacitor to discharge from V_{DD} to V_{OL}

$$I_{dsn} = -C\frac{dv_o}{dt}$$

Initially NMOS is in saturation. After $V_o = V_{IH} - V_{tn}$, it moves into linear region.

$$\frac{1}{C}\int_0^{T_{fall}} dt = -\int_{V_{DD}}^{V_{OL}} \frac{dv_o}{I_{dsn}}$$

$$\Rightarrow \frac{T_{fall}}{C} = -\int_{V_{DD}}^{V_{IH}-V_{tn}} \frac{dv_o}{I_{dn\,sat}} - \int_{V_{IH}-V_{tn}}^{V_{OL}} \frac{dv_o}{I_{dn\,linear}}$$

$$= \int_{V_{IH}-V_{tn}}^{V_{DD}} \frac{dv_o}{\frac{k_n}{2}(V_{IH}-V_{tn})^2} + \int_{V_{OL}}^{V_{IH}-V_{tn}} \frac{dv_o}{k_n\left((v_i-V_{tn})v_o - \frac{v_o^2}{2}\right)}$$

$$\Rightarrow \boxed{\frac{k_n T_{fall}}{C} = \frac{2(V_{DD}-V_{IH}+V_{tn})}{(V_{IH}-V_{tn})^2} + \frac{1}{k_n(V_{IH}-V_{tn})}\ln\left(\frac{2(V_{IH}-V_{tn})-V_{OL}}{V_{OL}}\right)}$$

Substituting the values of the parameters, we get

$$\boxed{\frac{k_n T_{fall}}{C} = 13.11}$$

$$\Rightarrow \boxed{\frac{k_p T_{rise}}{C} = \frac{k_n T_{fall}}{C}}$$ Theoritically

Results and comments:

	C	D
T_{rise}	0.164 ns	0.180 ns
T_{fall}	0.156 ns	0.164ns

	I3	I4
T_{pdr}	0.1092ns	0.1845ns
T_{pdf}	0.1068ns	0.1649ns
T_{pd}	0.108ns	0.1747ns

Firstly, T_{rise} is greater than T_{fall} . This is because in my ngspice transistors, as mentioned in question3, Kn is slightly greater than Kp.

The **T_{rise} and T_{fall} values at node D >node C**. So they are not same.

Also, the **Tpd of I4> I3.**

We can easily justify why this is happening. Beyond a point, when we increase the W of a transistor, the size of the transistor becomes bigger. This means that the parasitic capacitances inside the transistor increases as W increases. I3 has lesser individual capacitance compared to that of I4. Also the load capacitance for I3 is lesser than that of I4(Because I3 has capacitance as I4+I5+CL whereas I4 has load capacitance I5+CL). This means that for I4, we have more charging/discharging time when compared with I3. This results in slower operation time i.e. more Tpd for I4 when compared with I3. We also know that the value of Trise and Tfall are closely related and are directly proportional to the Tpd and increase when Tpd increases. So based on the argument of capacitances mentioned above, we can say that the Trise and Tfall values at D are more when compared to the values at C.

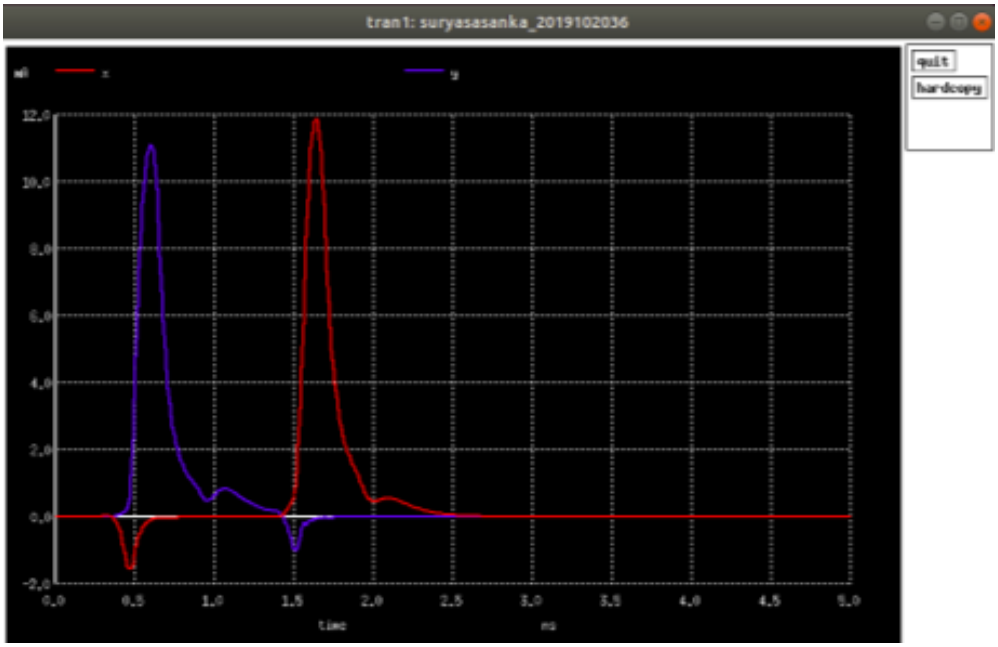
Netlist (To calculate I_{DD} and I_{SS}):

```
Vdd vdd gnd 'SUPPLY'
VDS D1 gnd 1.8
VDS1 gnd S1 0
VGS in gnd pwl (0 0V 0.5ns 1.8V 1.1ns 1.8V 1.5ns 0V 10ns 0V)

M1 b in gnd gnd CMOSN W={width_N1} L={2*LAMBDA}
+ AS={5*width_N1*LAMBDA} PS={10*LAMBDA+2*width_N1} AD={5*width_N1*LAMBDA} PD={10*LAMBDA+2*width_N1}

M2 b in vdd vdd CMOSP W={width_P1} L={2*LAMBDA}
+ AS={5*width_P1*LAMBDA} PS={10*LAMBDA+2*width_P1} AD={5*width_P1*LAMBDA} PD={10*LAMBDA+2*width_P1}

M3 c b gnd gnd CMOSN W={width_N2} L={2*LAMBDA}
+ AS={5*width_N2*LAMBDA} PS={10*LAMBDA+2*width_N2} AD={5*width_N2*LAMBDA} PD={10*LAMBDA+2*width_N2}

M4 c b vdd vdd CMOSP W={width_P2} L={2*LAMBDA}
+ AS={5*width_P2*LAMBDA} PS={10*LAMBDA+2*width_P2} AD={5*width_P2*LAMBDA} PD={10*LAMBDA+2*width_P2}

M5 d c S1 gnd CMOSN W={width_N3} L={2*LAMBDA}
+ AS={5*width_N3*LAMBDA} PS={10*LAMBDA+2*width_N3} AD={5*width_N3*LAMBDA} PD={10*LAMBDA+2*width_N3}

M6 d c D1 vdd CMOSP W={width_P3} L={2*LAMBDA}
+ AS={5*width_P3*LAMBDA} PS={10*LAMBDA+2*width_P3} AD={5*width_P3*LAMBDA} PD={10*LAMBDA+2*width_P3}

M7 e d gnd gnd CMOSN W={width_N4} L={2*LAMBDA}
+ AS={5*width_N4*LAMBDA} PS={10*LAMBDA+2*width_N4} AD={5*width_N4*LAMBDA} PD={10*LAMBDA+2*width_N4}
```

```
.control
run

let x= (-VDS#branch)
let y= (-VDS1#branch)

set curplottitle="suryasasanka_2019102036"
plot v(c) v(d)
plot x y
set hcopypscolor = 1 *White background
hardcopy q4dplot.eps x y
.endc
"question4.sp" 106L, 3033C
```

We make the highlighted change in the initial netlist and add few lines to print the values of I_{DD} and I_{SS} .

Plot (I_{DD} and I_{SS})



Red line- I_{DD}

Blue line- I_{SS}

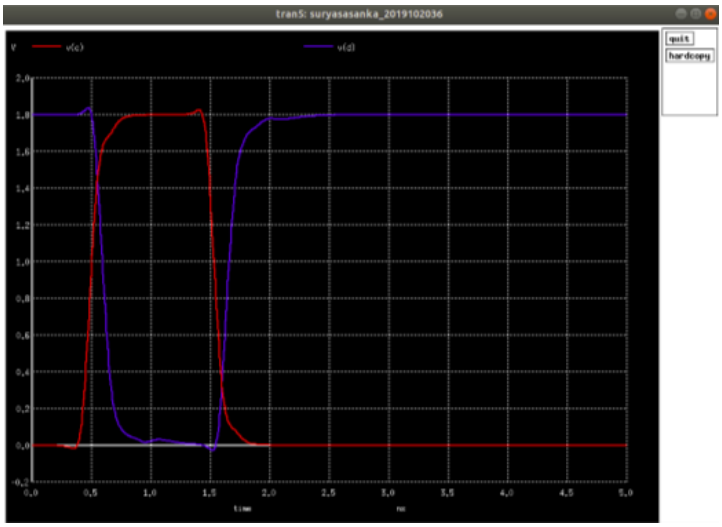


Figure-5(Repeated for the sake of clarity)

Red line- Input voltage

Blue line- Ouput voltage

We know that CMOS inverter is used to make static logic gates. However, we have a dynamic region as well in the inverter.

When operate the inverter at HIGH or LOW, we find that one of the MOSFET is in the cutoff region. This means that one of the inverter is in OFF state. So no current flows through it. So both I_{DD} and I_{SS} equal to 0 in that case. During the transition states/dynamic region, we find that the current is non-zero.

Initially at t=0, the input gate voltage to I3 is 0. The pmos is ON and nmos is OFF. When the gate voltage transitions from 0 to 1, we notice a small negative value of gate voltage as shown in figure-5 just before changing to 1, so we notice that small current flows from drain(V0) to Vdd which is I_{DD}.

As the value of input starts increasing, the output starts decreasing from 1 to 0 with a delay. During that period, both the mosfets are on. Then the pmos becomes off. In between this process, the capacitor which is at the V0 discharges from 1 to 0 through the nmosfet causing a spike in the current I_{SS}.

When the input at 1 is just about to transition to 0, we notice that the value becomes slightly more than Vdd. Here, we have a small value of current(I_{SS}) flowing from the source of nmos to the capacitor and charging it.

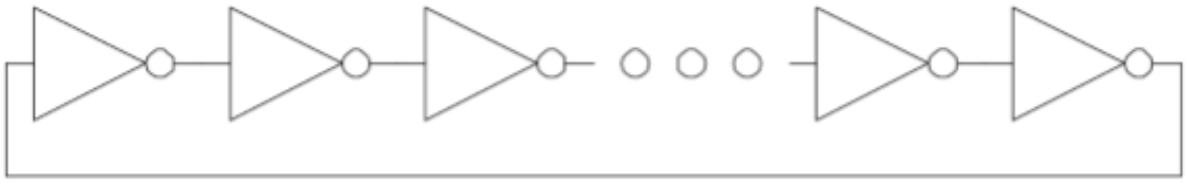
As the value of input starts decreasing, the value of output starts increasing from 0 to 1 with a delay, During that period, both the mosfets are on. Then the nmos becomes off. In between the process, we find that since the capacitor is at 0 volts and the source of the capacitor is at Vdd, current flows immediately from the pmos into the capacitor charging it. This current spike is the I_{DD} shown in the figure.

Clearly, we notice that the huge positive current spikes are the currents corresponding to the charging and discharging of the capacitor through the mosfets.

Problem 5:

Design a 31 stage ring oscillator (RO) using L = 2λ, Wn = 10λ and Wp = 25λ, where λ = 0.09µm.

Circuit:



We can place 31 CMOS inverters as shown above but this is not the optimal circuit. Here, we get a lot of capacitance because the gaps(metal wires) between the inverters are not equally spaced. So the ideal circuit would be to place 16 inverters in the top row and 15 inverters in the bottom row and join them with almost equal spacing wires to reduce the capacitance.

Theory:

Frequency of oscillation(fRO)- It is 1/Time period.

Time period- It can be defined as the time elapsed between two rising edges at a particular node.

Time delay(T_D)- It is the propagation delay i.e. the average of Tpdr and Tpdf as mentioned in question 4.

In one time period at a particular node, we have the input from 0 to 1 and then back to 0 from 1. This means that if we look at one particular input/output node of an inverter, we can find that the voltage needs to change from 0 to 1 which has propagation delay T_D and then again from 1 to 0 which has propagation delay T_D. So the total would be $2*T_D$. We have 31 such nodes. So the total time period would be $62*T_D$. So the frequency of oscillation would be $fRO=1/62*T_D$.

Netlist(prelayout):

```
Fifth question
.include TSMC_180nm.txt
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param width_N=20*LAMBDA
.param width_P=2.5*width_N
.global gnd vdd

VDS vdd gnd 'SUPPLY'

.subckt inv y x vdd gnd
.param width_N=20*LAMBDA
.param width_P=2.5*width_N

M1 y x gnd gnd CMOSN W={width_N} L={2*LAMBDA}
+AS={5*width_N*LAMBDA} PS={10*LAMBDA+2*width_N} AD={5*width_N*LAMBDA} PD={10*LAMBDA+2*width_N}

M2 y x vdd vdd CMOSP W={width_P} L={2*LAMBDA}
+AS={5*width_P*LAMBDA} PS={10*LAMBDA+2*width_P} AD={5*width_P*LAMBDA} PD={10*LAMBDA+2*width_P}
.ends inv

x1 inp2 inp1 vdd gnd inv
x2 inp3 inp2 vdd gnd inv
x3 inp4 inp3 vdd gnd inv
x4 inp5 inp4 vdd gnd inv
x5 inp6 inp5 vdd gnd inv
x6 inp7 inp6 vdd gnd inv
x7 inp8 inp7 vdd gnd inv
x8 inp9 inp8 vdd gnd inv
x9 inp10 inp9 vdd gnd inv
x10 inp11 inp10 vdd gnd inv
x11 inp12 inp11 vdd gnd inv
x12 inp13 inp12 vdd gnd inv
x13 inp14 inp13 vdd gnd inv
x14 inp15 inp14 vdd gnd inv
x15 inp16 inp15 vdd gnd inv
x16 inp17 inp16 vdd gnd inv
x17 inp18 inp17 vdd gnd inv
x18 inp19 inp18 vdd gnd inv
x19 inp20 inp19 vdd gnd inv
x20 inp21 inp20 vdd gnd inv
x21 inp22 inp21 vdd gnd inv
x22 inp23 inp22 vdd gnd inv
x23 inp24 inp23 vdd gnd inv
```

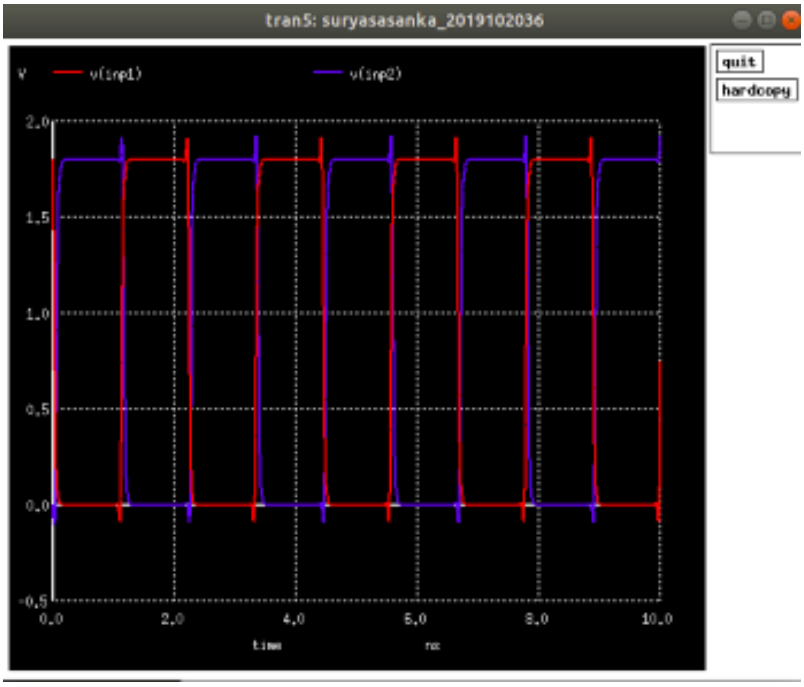
```
x24 inp25 inp24 vdd gnd inv
x25 inp26 inp25 vdd gnd inv
x26 inp27 inp26 vdd gnd inv
x27 inp28 inp27 vdd gnd inv
x28 inp29 inp28 vdd gnd inv
x29 inp30 inp29 vdd gnd inv
x30 inp31 inp30 vdd gnd inv
x31 inp1 inp31 vdd gnd inv
```

In the netlist, we have used the subckt function and called it inv where we have defined a single CMOS inverter. We repeatedly call the inv to place the 31 inverters. We also plot two consecutive node voltages to check that the 31-stage oscillator works properly.

```
.tran 0.01n 50n
.ic v(inp1)=1.8
.measure tran tfreq
+ TRIG v(inp1) VAL='SUPPLY/2' RISE=1
+ TARG v(inp1) VAL='SUPPLY/2' RISE=2

.measure tran tpdr
+ TRIG v(inp1) VAL='SUPPLY/2' RISE=1
+ TARG v(inp2) VAL='SUPPLY/2' FALL=1

.measure tran tpdf
+ TRIG v(inp1) VAL='SUPPLY/2' FALL=1
+ TARG v(inp2) VAL='SUPPLY/2' RISE=1

.measure tran tpd param='(tpdr+tpdf)/2' goal=0
```

This part of the netlist helps us to calculate the value of the time period and the propagation delay. We again use the '.measure' function. For the time period, we start the TRIG in the first rising edge when the voltage is supply/2 at the node inp1 and use the TARG when we again get the value of voltage to be supply/2 in the second rising edge which gives us the Tfreq. The calculation of propagation delay is similar to that of the question4.

Results and plots(pre-layout):



We have plotted two consecutive nodes just to check that our 31 stage ro is working.

```
  Measurements for Transient Analysis

tfreq                =  2.219297e-09 targ=  3.346007e-09 trig=  1.126709e-09
tpdr                 =  3.638918e-11 targ=  1.163098e-09 trig=  1.126709e-09
tpdf                 =  3.459494e-11 targ=  5.262380e-11 trig=  1.802886e-11
tpd                  =  3.54921e-11
```

Time period=2.219 ns

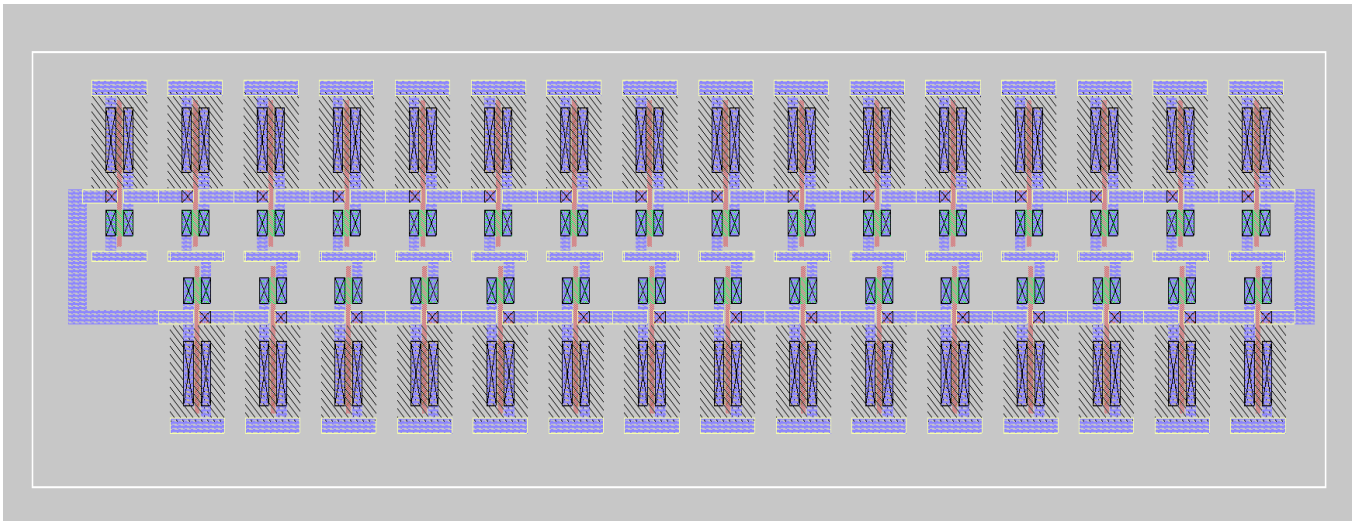
T_D=3.549*10^-2 ns

fRO=1/timeperiod=1/(2.219n)

1/62*T_D=1/(2.2003n).

So in the pre-layout setup, fRO=1/62*T_D

Magic layout



Parameters:

- Length of the MOSFET- (2 * lambda). Can be found from width of polysilicon
- Width of P-MOSFET - (25 * lambda). Can be found from pdiffusion layer (14X25 lambda)
- Width of N-MOSFET - (10 * lambda). Can be found from ndiffusion layer (14X10 lambda)

- Drawing this layout is not very complicated. We just need to draw the layout of one inverter. Then we use the getcell command to get the inverter.
- Using the array<16><1> command, we get the 16 inverters in the top row where one output is connected.

- Then we again use the getcell command to get another inverter in the second row. We use the ‘f’ command to flip the circuit.
- Then we use the upside down command to see that the ground of the top row inverter and the ground which came to the top of the bottom row inverter are joined.
- Now we simply connect the top and the bottom rows by using metal to complete the circuit.

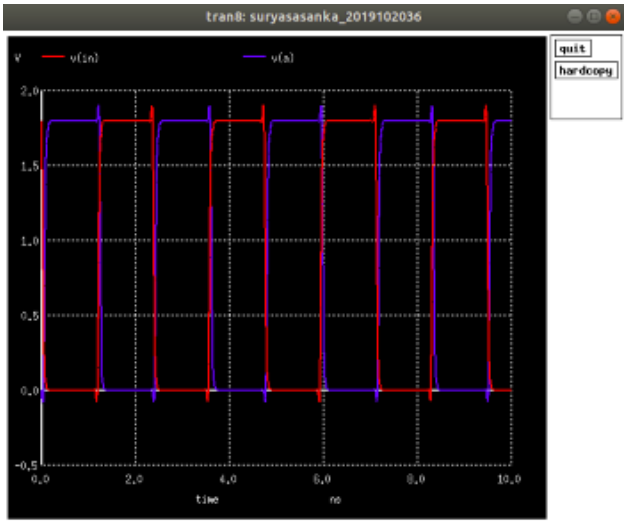
Netlist(Post-layout)

The extracted netlist contains 371 parasitic capacitances. We also have the original 62 mosfets. So the total extracted netlist when changed is more than 500 lines. So we are not attaching the netlist. Click on the link below to view the post-layout modified code for the ringoscillator.

https://iiitaphyd-my.sharepoint.com/:u:/g/personal/sri_surya_students_iiit_ac_in/EXVKInNHv5tGkI10DMu7LhIB8DKu2103jHWvgAhycYCKMA?e=GPfcft

We have to carefully modify the code and be very careful about spacing and replacing the names of the capacitances because debugging an error becomes almost impossible due to the length of the netlist.

Results and plots(pre-layout):



We have plotted two consecutive nodes just to check that our 31 stage ro is working.

```
  Measurements for Transient Analysis

tfreq                =  2.368975e-09 targ=  3.573057e-09 trig=  1.204082e-09
tpdr                 =  3.883127e-11 targ=  1.242913e-09 trig=  1.204082e-09
tpdf                 =  3.778675e-11 targ=  5.807174e-11 trig=  2.028499e-11
tpd                  =  3.83090e-11
```

Time period=2.368 ns

T_D=3.8309*10^-2 ns

fRO=1/timeperiod=1/(2.368n)

1/62*T_D=1/(2.3751 n).

So in the pre-layout setup, fRO=1/62*T_D

Pre-layout and post-layout

	Time period	T_D	fRO	1/62* T_D
Pre-layout	2.219 ns	3.549*10^-2 ns	450.653 MHz	454.48MHz
Post-layout	2.368 ns	3.8309*10^-2 ns	422.29 MHZ	421.03MHz

We have noticed that the propagation delay and time period are more in the case of post-layout when compared to pre-layout. This is because in the extracted post-layout netlist, we have 371 parasitic capacitances which were not included by us in the pre-layout simulation. Since the value of capacitances is high, the time taken to charge the capacitances increases and thus it increases the value of the time delay and the time period as well.

We can conclude from the obtained values that we have implemented the circuit very optimally because we got the time delay and time period deviation from the pre-layout values to be very less(~7.5%).