Portland State
UNIVERSITY

ECE 586 COMPUTER ARCHITECTURE FINAL PROJECT REPORT
SPRING 2024

MIPS
LITE PIPELINE SIMULATOR

Team 6
Yashaswi Katne
VVSS Lohith
Veekshith Venkatesha Murthy
Rakesh Reddy Kunduru

ROLE AND RESPONSIBILITIES

We worked on this project (Simulation of 5 stage pipeline MIPS Lite architecture) and completed it successfully. We split our work equally and worked together throughout the whole project.

Yashaswi Katne: Completion of pipeline simulator component of the simulator and calculating stall conditions.

V.V.S.S Lohith: Functional simulator which simulates the MIPS-lite ISA and captures the impact of instruction execution on machine state. Functional simulators testing and modelling in execution stage.

Veekshith Venkatesha Murthy: Writing all Instructions, Test by providing trace and by making necessary
modifications, test it again.

Rakesh Kunduru: Decode stall and write in various modes, check all necessary simulation results and project report.