Verification Plan Document(Team3_AsyncFIFO_S24_ECE593)

GitHub Link(Private): [sashakatne/Team3_AsyncFIFO_S24_ECE593 (github.com)]

Module Under Test: fifo2

Parameters:

- Data Size (DSIZE) = 8
- Address Size (ASIZE) = 4

Testbench Signals:

- wdata: Data to be written
- winc: Write enable
- wclk: Write clock
- wrst_n: Write reset
- rinc: Read enable
- rclk: Read clock
- rrst_n: Read reset
- rdata: Data read from the FIFO
- wfull: Write FIFO full indicator
- rempty: Read FIFO empty indicator

Clock Periods:

- Write Clock Period (CLK_PERIOD_WR) = 12.5 ns
- Read Clock Period (CLK_PERIOD_RD) = 20 ns

Test Sequence:

1. Initialize all signals.
2. Reset the write and read processes.
3. Write 120 items into the FIFO.
4. Wait for some cycles.
5. Read 120 items from the FIFO.
6. Finish simulation.

Verification Environment:

- Testbench instantiates the fifo2 module.
- Clocks wclk and rclk are generated with their respective periods.
- Test sequence writes and reads data to/from the FIFO.
- Monitor displays key signals.

Initial Verification Plan Summary:

1. Write Operation:
    - Write 120 items to the FIFO.
    - Check for write FIFO full condition.
2. Read Operation:
    - Read 120 items from the FIFO.
    - Check for read FIFO empty condition.
3. Clocks:
    - Verify write and read clock periods.
4. Reset:
    - Verify FIFO reset functionality.
5. Data Integrity:
    - Verify data integrity between write and read operations.

Division of Tasks among Team Members:

This division of tasks between team members is tentative only. In reality everyone gets involved in the project in some way or the other. The responsibilities are likely to change as the project progresses and tasks are given.

Milestone-1:

1a. **Anurag Ranga** : Complete design specifications document with calculations for DUT.

1b.**Maheshwar Kamalapuram**: Verification Plan document in place with initial information. Task division and schedule included.

1c.**Yashaswi Katne:** Implementation of design and successful compilation.

1d.**Naveen Kumar Reddy . T**: Develop a simple conventional testbench to check basic functionality.

Milestone-2:

2a.**Yashaswi Katne**: Develop Class-Based testbench. All interfaces completed and tested.

2b.**Naveen Kumar Reddy . T**: Complete transactions, Generator, Drivers, and other components.

2c.**Maheshwar Kamalapuram**: Verify at least 20-50 randomized bursts of data.

2d.**Anurag Ranga**: Update Verification Plan with more detailed updates.

Milestone-3:

3a.**Anurag**: Finalize any changes in RTL for any updates needed.

3b. **Yashaswi Katne and Anurag**: Complete the class-based verification. All components must be defined and working (Transaction, Generator, Driver, Monitors, Scoreboard, and Coverage).

3c.**Maheshwar Kamalapuram**: Include both code-coverage and functional coverage reports.

3d. **Naveen Kumar Reddy T:** Update Verification Plan with more detailed test cases if any more are added.

Milestone-4:

4a.**Anurag**: Develop UVM testbench, starting with UVM TB architecture.

4b.**Yashasvi Katne**: Add a section for UVM verification Plan and add details on UVM architecture, UVM hierarchy, UVM components (sequence, sequencer, driver, monitor, scoreboard, interfaces with DUT, number of agents planned, etc.).

4c.**Naveen Kumar Reddy T and Maheshwar** : Utilize UVM_MESSAGING, UVM_LOGGING mechanisms to create and log the reports and data.

Milestone-5 (Final Deliverables + Presentations):

5a.**Yashasvi Katne**: Complete the UVM architecture, UVM environment, and UVM testbench.

5b.**Naveen Kumar Reddy T**: Complete all test cases and reflect them in the coverage reports.

5c.**Maheshwar Kamalapuram**: Create scenarios of bug injection and verify. Show your work.

5d.**Anurag Ranga**: Finalize the documents, paper, and presentations. Update Design Specification document, Verification Plan documents with all the updated and latest data.

 # Specification B

FIFO Operating Conditions:

Transmitter clk1 frequency = 80 MHz

Receiver clk2 frequency = 50 MHz

With duty-cycle of 50%.

Max reads Burst size = 120

Num. of idle cycle between successive writes = 0

Num. of idle cycles between successive reads = 0

There are no idle cycles in both reading and writing which means that, all the items in the burst will be written and read in consecutive clock cycles

Time required to write one data item = 1 x (1/80MHz) = 12.5ns

Time required to write all the data in the burst = 120 x 12.5ns = 1500ns

Time required to read one data item = 1 x (1/50MHz) = 20ns

So, for every 20 ns, the Receiver is going to read one data item in the burst. In a period of 1500ns, 120 data items can be written

The no. of data items can be read in a period of 1500 ns = 1500/20 = 75

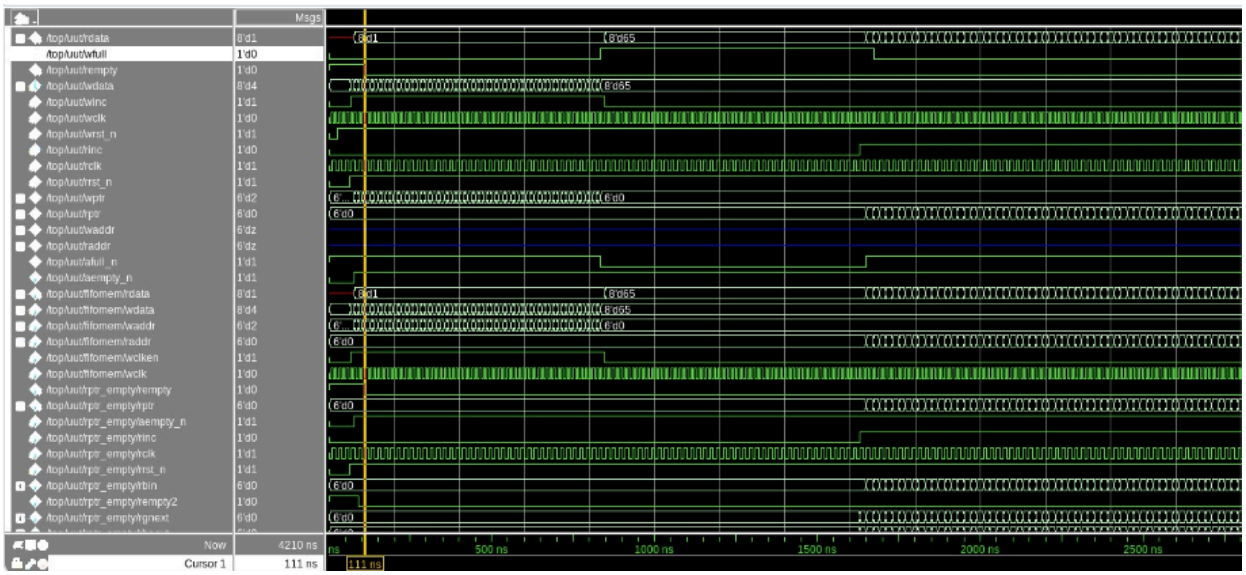
The remaining no. of bytes to be stored in the FIFO = 120 - 75 = 45

So, the FIFO which has to be in this scenario must be capable of storing 45 data items

So, the minimum depth of the FIFO should be 45.

Waveforms:

FIFO Read from Memory



FIFO Write to Memory.