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1. I. Cache lines $= \frac{cache\ size}{block\ size} = \frac{512*2^{10}}{4*4} = 2^{15}$

II. 16 = 2^4

Associative mapping cache - format of memory address

28bits	4bits

III. Cache lines = 2^15

Direct mapping cache - format of memory address

13bits	15bits	4bits

IV. If the cache is 8-way set associative, sets of cache = 2^15 / 8 = 2^12 sets

V. sets of cache = 2^12

8-way set associative mapping cache - format of memory address

16bits	12 bits	4 bits

VI. 0x B1AC95F9 = 0b 10110001101011001001010111111001

Tag 1011000110101100	Set 100101011111	Word 1001

Set number = 1001010111112

2.

X =(A*B-C) + (A/C)

I. Stack based

PUSH A
PUSH B
MUL
PUSH C
SUB
PUSH A
PUSH C
DIV
ADD
POP X

II. Accumulator based

```
LOAD A
DIV C
STORE P
LOAD A
MUL B
SUB C
ADD P
STORE X
```

III. Memory-memory based

3 operands

```
DIV N, A, C
MUL L, A, B
SUB M, L, C
ADD X, M, N
```

2 operands

```
MOV P, A
DIV P, C
MOV R, A
MUL R, B
SUB R, C
ADD R, P
```

IV. Register-Register based

```
LOAD R1, A
LOAD R2, B
LOAD R3, C
DIV R4, R1, R3
MUL R5, R1, R2
SUB R5, R5, R3
ADD R4, R5, R4
STORE X, R4
```

3.

-6 = (00110) => 11010_2 = **M**

9 = 01001_2 = **Q**

-6 * 9 =>

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A	Q	Q_{-1}	M	Cycle
00000	01001	0	11010	Initial state
00110	01001	0	11010	First cycle
00011	00100	1	11010	
11101	00100	1	11010	Second cycle
11110	10010	0	11010	
11111	01001	0	11010	Third cycle
00101	01001	0	11010	Forth cycle
00010	10100	1	11010	
11100	10100	1	11010	Fifth cycle
11110	01010	0	11010	

Final answer = 1111001010 => reverse 2's compliment => -54

4.

MAR ← [PC]

MBR ← $[Memory]_{MARaddress}$; PC ← [PC] + 1 (increment the PC for next cycle at the same time)

CIR ← [MBR]

[CIR] decoded then executed

5.