

**Birla Institute of Technology & Science, Pilani**  
**Work Integrated Learning Programmes Division**  
**Second Semester 2019-2020**  
**M.Tech (Data Science and Engineering)**  
**Mid-Semester Exam (EC-2 Makeup)**

Course No. : DSEIDZG516  
Course Title : Computer Organization and Software Systems  
Nature of Exam : Open Book  
Weightage : 30%  
Duration : 90 minutes  
Date of Exam : 05/07/2020 (FN), 10:00 am to 11:30 am

|                  |     |
|------------------|-----|
| No. of Pages     | = 3 |
| No. of Questions | = 4 |

Note to Students:

1. **All parts of a question should be answered consecutively. Each answer should start from a fresh page.**
2. **Assumptions** made if any, should be stated clearly at the beginning of your answer.
3. For all problems **relevant steps** are to be shown.

**Q1: Answer the following questions.**

**[7 MARKS]**

A. Games can be played in any device ranging from Xbox to mobiles. However, games must be conceptualized, designed and developed in computers with high end configurations. Desktops are powerful, but they do not give flexibility to game development companies. Game development companies are slowly shifting towards laptops as it encourages collaboration and agility. It also gives perfect work-life balance to their employees as they can continue their work from home with help of laptops. Due to this, there is a huge demand for laptops and their performance metrics. CPU manufacturing companies buy these performance metrics from “Mybenchmark” which is a benchmarking organization. “Mybenchmark” uses standard programs to assess the performance of CPUs.

Two new processors meant to be used in gaming laptops is designed with frequencies of 2 GHz and 1 GHz. These processors execute one instruction at a time. The table below gives instruction counts for the benchmark program - as well as number of cycles each instruction take, for the different classes of instructions.

| Instruction Type`       | Purpose  | Processor 1 (2 GHz) |        | Processor 2 (1 GHz) |        |
|-------------------------|--|---------------------|--------|---------------------|--------|
|                         |  | Instruction Count   | Cycles | Instruction count   | Cycles |
| Load & Store            | Memory access instructions take higher number of cycles ; added to benchmark programs to simulate industry scenarios | 3000                | 5      | 2000                | 2      |
| Arithmetic Instructions | Floating point and integer arithmetic instructions are predominantly used in business transactions and programs      | 4000                | 3      | 6000                | 1      |
| All others              | These are instructions such as program control transfer  | 3000                | 4      | 2000                | 1      |

Benchmark comparisons looks at few critical parameters such as CPI, MIPS and cycle time. Calculate the following parameters for both processors:

- i. What is the CPI for Processor1 and Processor2? [2]
- ii. What is the processor speed for Processor1 and Processor2 in millions of instructions per second (MIPS)? [2]
- iii. Which is the fastest processor among Processor1 and Processor2? Justify your answer. [1]

- B. A disk track holds 60 Kbytes and its sector size is 2048 bytes. If it takes 2 ms to transfer a sector, what is the disk's rotational speed in rpm? [2]

**Q2 . Answer the following questions.**

**[8 MARKS]**

- A. A company named CacheFul is designing a machine with a byte addressable main memory. The size of the main memory is  $2^{18}$  Bytes and block size is 16 Bytes. The machine employs a direct mapping cache consisting of 32 lines. This machine is specifically configured to run a classification algorithm.
- When the algorithm is run it is noted that a memory access to main memory on a cache "miss" takes 30 ns and memory access to the cache on a cache "hit" takes 3 ns. If 80% of the processor's memory requests result in a cache "hit", how much time does it take to access memory on average? [1.5]
  - Recommended average memory access time for the algorithm to perform optimally is not more than 5 ns, what option as a **developer**, do you have to keep it near to 5ns? [1.5]
- B. Scientists at Indian Science Research Institute, wanted to check whether implementing cache replacement using two existing cache memory replacement algorithm LFU and FIFO would help reducing miss rate. The proposed new algorithm would work in two phases. The first 6 clocks (0-5) follow LFU and next 6 clocks (6-11) follow FIFO. The main memory block sequence is
- 0, 4, 0, 2, 1, 5, 0, 1, 2, 5, 0, 2**
- What is the Hit Ratio for the proposed new replacement algorithm? Justify your answer by filling in the following table. In LFU, in case of tie between cache lines for replacement, select the line which has been there for longer time in the cache. [4]

|          | LFU |   |   |   |   |   | FIFO |   |   |   |    |    |
|----------|-----|---|---|---|---|---|------|---|---|---|----|----|
| Time     | 0   | 1 | 2 | 3 | 4 | 5 | 6    | 7 | 8 | 9 | 10 | 11 |
| Block #  | 0   | 4 | 0 | 2 | 1 | 5 | 0    | 1 | 2 | 5 | 0  | 2  |
| L0       |     |   |   |   |   |   |      |   |   |   |    |    |
| L1       |     |   |   |   |   |   |      |   |   |   |    |    |
| L2       |     |   |   |   |   |   |      |   |   |   |    |    |
| L3       |     |   |   |   |   |   |      |   |   |   |    |    |
| Hit/Miss |     |   |   |   |   |   |      |   |   |   |    |    |

- A hit ratio of 7/12 and 6/12 is achieved if LFU and FIFO replacement algorithms respectively are used. Scientists at Indian Science Research Institute would want you recommend appropriate replacement algorithm out of three schemes (LFU, FIFO and Proposed new scheme specified in part (i) ) with proper justification. [1]

**Q3. Answer the following Questions.**

**[8 Marks]**

- A. Consider a reservation table for an instruction pipeline with four stages: where IF- Instruction Fetch, ID - Instruction decode and operand fetch, EX- Execute and WR - write operand.

|    | 0 | 1 | 2 | 3 |
|----|---|---|---|---|
| IF | X |   |   |   |
| ID |   | X |   |   |
| EX |   |   | X |   |
| WR |   |   |   | X |

- Draw time space diagram showing 3 instruction execution (I1, I2 and I3). [1]
  - Calculate speed up and efficiency for 100 instruction execution. [2]
- B. Consider a reservation Table for a pipeline with 5 stages and inter-stage buffers. It takes 8 clock cycles to execute a task. Draw the pipeline structure and identify the category to which this pipeline belongs to. [2]

