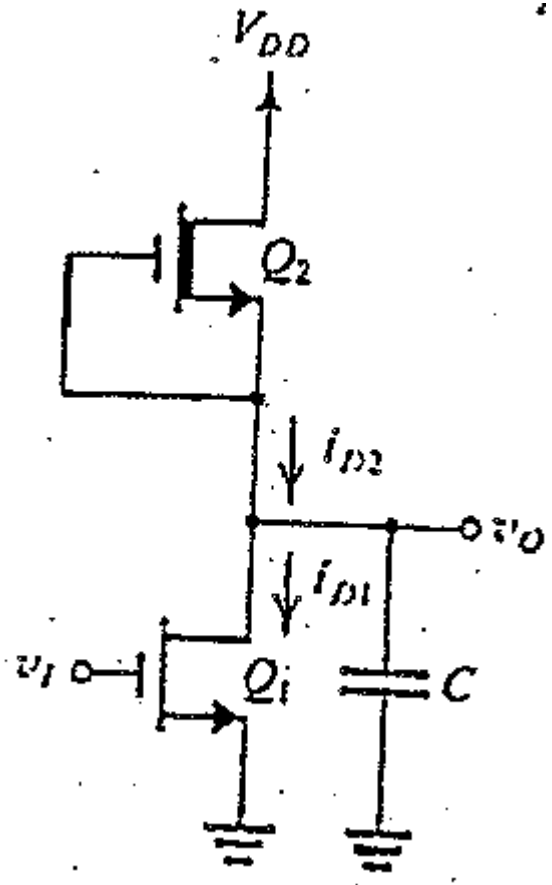
Circuiti digitali in tecnologia CMOS

Invertitore NMOS

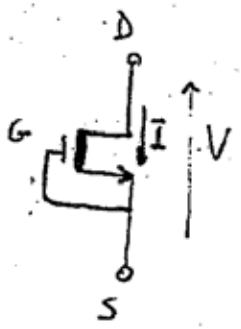


$v_I = v_{GS1}$

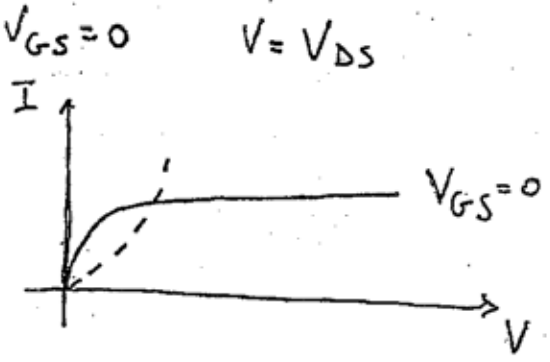
$v_O = v_{DS1} = V_{DD} - v_{DS2}$

Invertitore NMOS

carico attivo



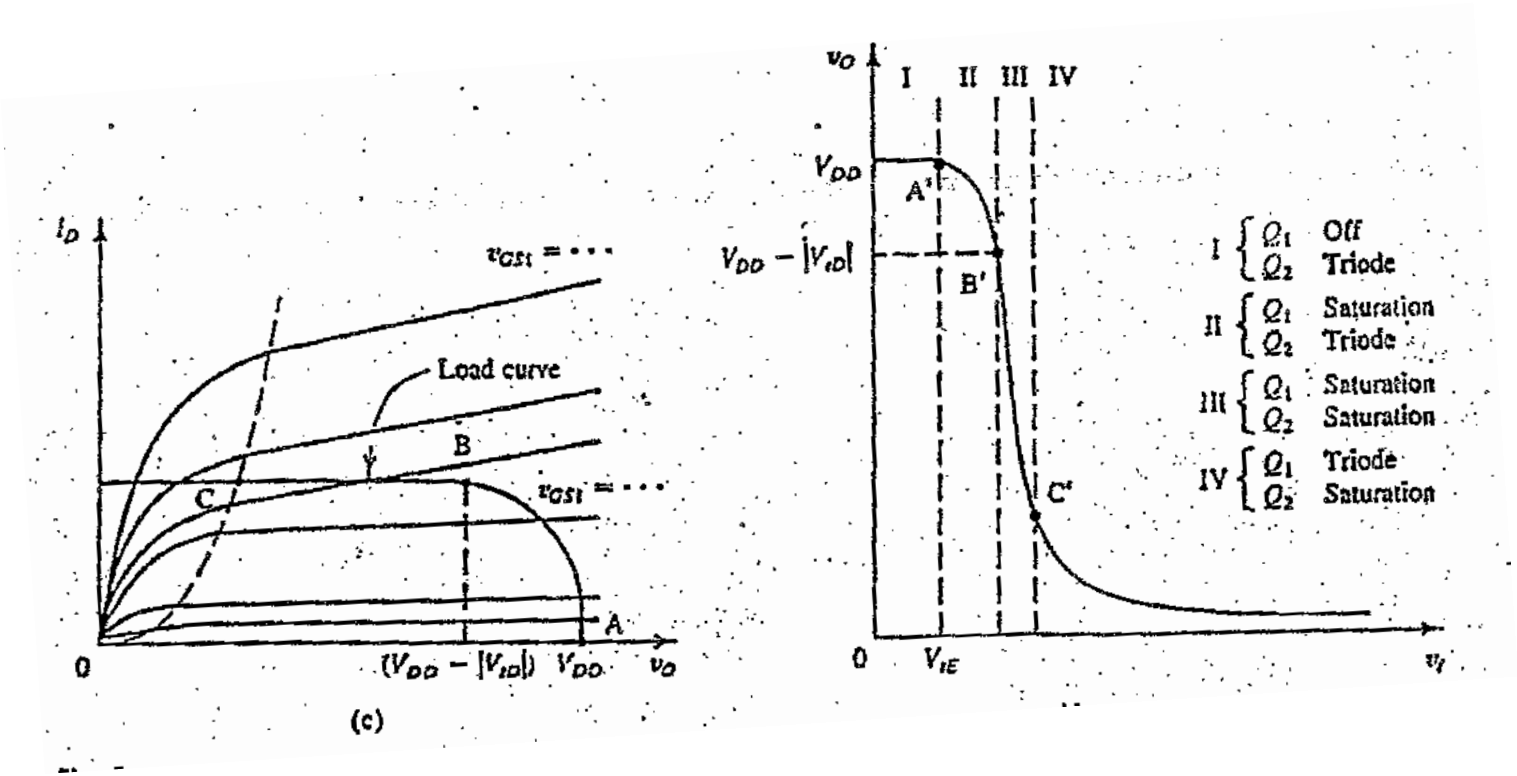
$V_t < 0$



- $V_{DS} < V_{GS} - V_t$ $\quad I = K\left[2(V_{GS} - V_t)V_{DS} - V_{DS}^2\right] = K\left[-2V_t V_{DS} - V_{DS}^2\right.$
  (0)

- $V_{DS} > V_{GS} - V_t$ $\quad I = K(V_{GS} - V_t)^2 \Rightarrow I = K V_t^2$
  (1)

Invertitore NMOS



Invertitore NMOS (margini di rumore)

Margini di rumore

- V_{OH} $\quad V_{OH} = V_{DD}$
- V_{OL} $\quad Q_1$ triodo $\quad Q_2$ pinch-off

$$i_{D1} = i_{D2}$$

$$K_1\left[2(v_{GS1} - V_{t0})v_{DS1} - v_{DS1}^2\right] = K_2(v_{GS2} - V_{t0})^2$$

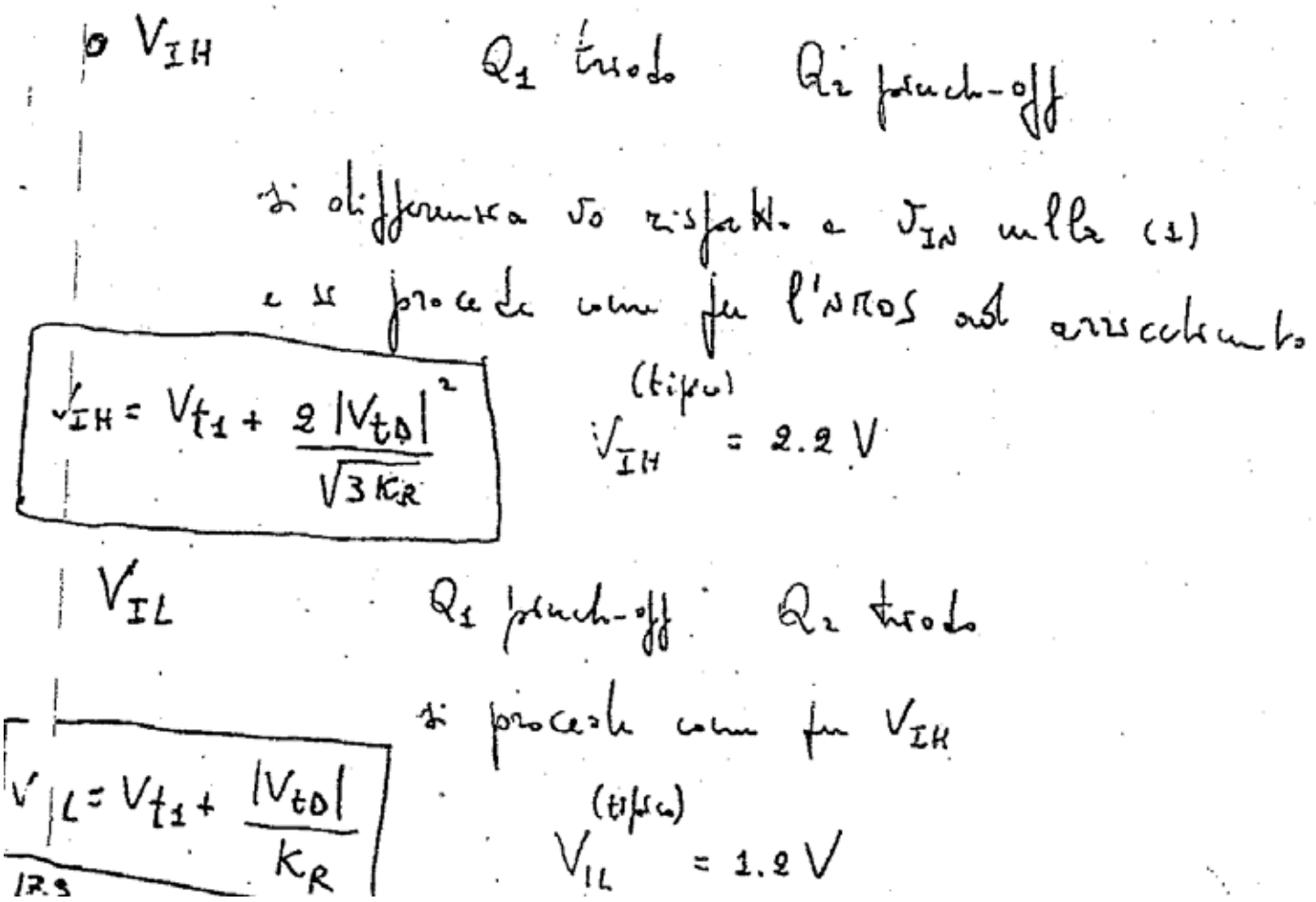
$$K_1\left[2(v_{IN} - V_{t0})v_O - v_O^2\right] = K_2|V_{t0}|^2 \qquad (1)$$

se $v_{IN} = V_{OH} \Rightarrow v_O = V_{OL}$

$$V_{OL} \simeq \frac{|V_{t0}|^2}{2K_R(V_{DD} - V_{t0})}$$

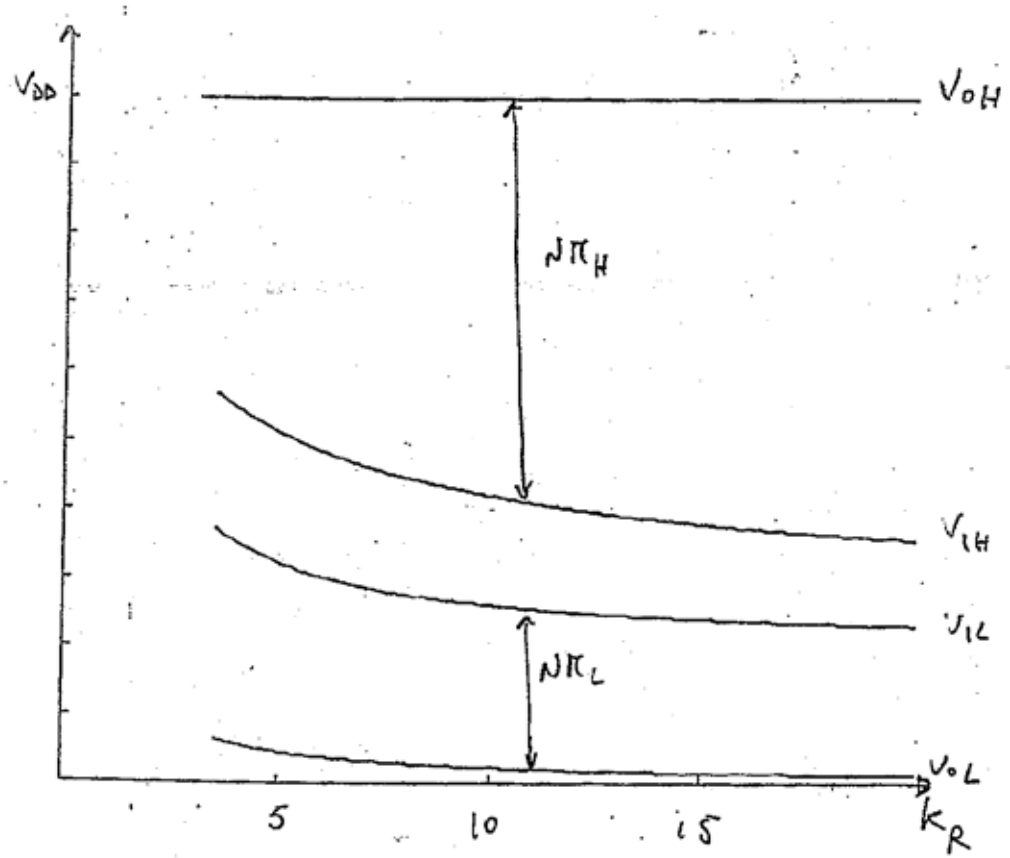
$$V_{OL}^{(tipico)} \simeq 0.1\ V$$

Invertitore NMOS (margini di rumore)

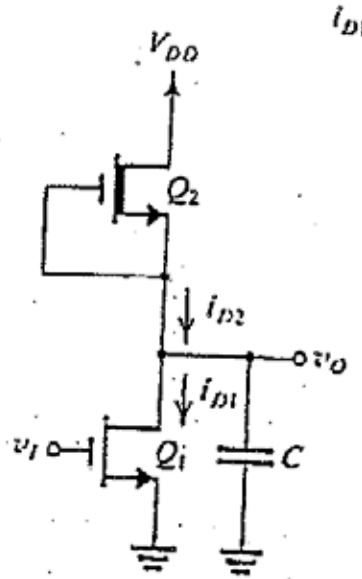


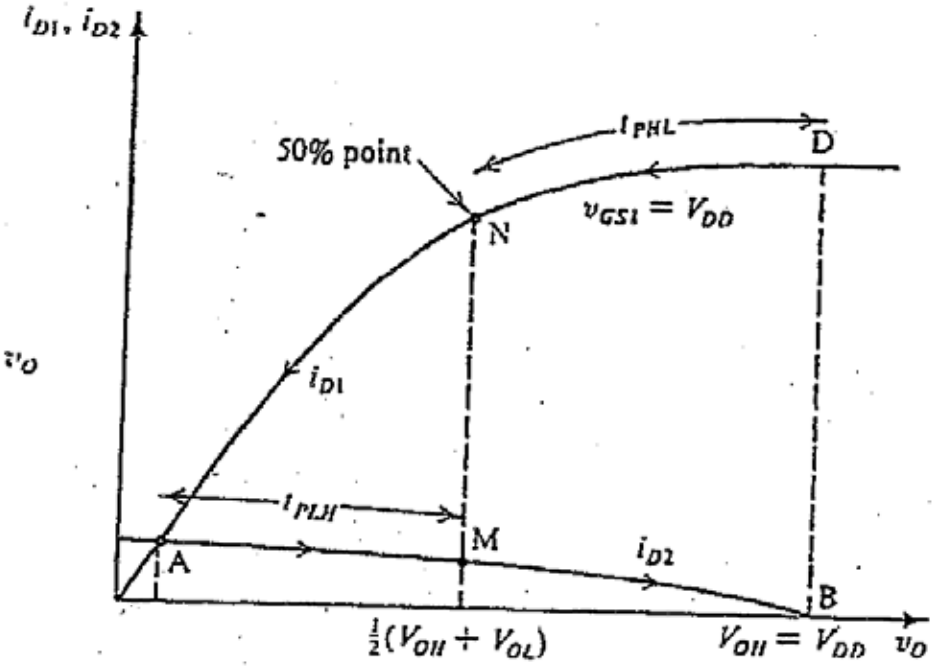
Invertitore NMOS (margini di rumore)

$$K_R = K_1 / K_2 = (W_1 / L_2) / (W_2 / L_2)$$



Invertitore NMOS (dissipazione di potenza)





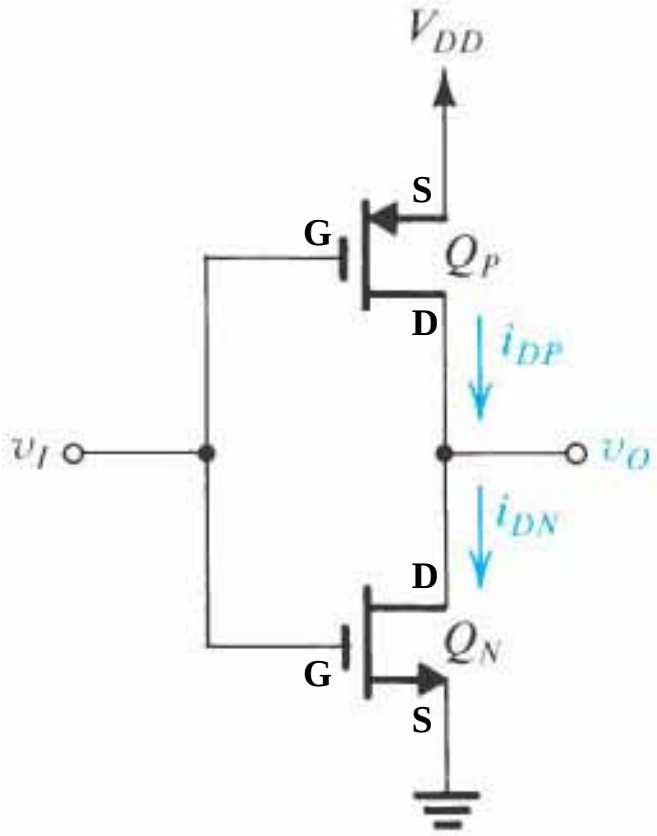
$$P_S^{(1)} \simeq 0$$

$$P_S^{(2)} = V_{DD} \cdot I_D^{(A)} = V_{DD} \cdot K_2 \left(V_{GS_2} - |V_{tD}|\right)^2$$

$$\bar{P}_S = \frac{1}{2}\left(P_S^{(1)} + P_S^{(2)}\right) = \frac{1}{2} K_2 |V_{tD}|^2 \cdot V_{DD}$$

$$P_{din} = f C V_{cc}^2$$

Invertitore CMOS



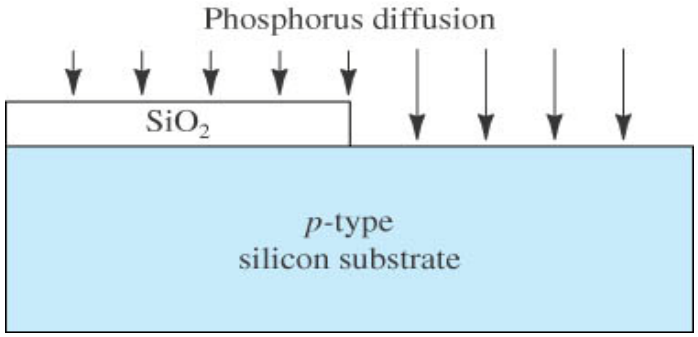
$v_I = v_{GSN}$

$v_O = v_{DSN} = V_{DD} - v_{SDP}$

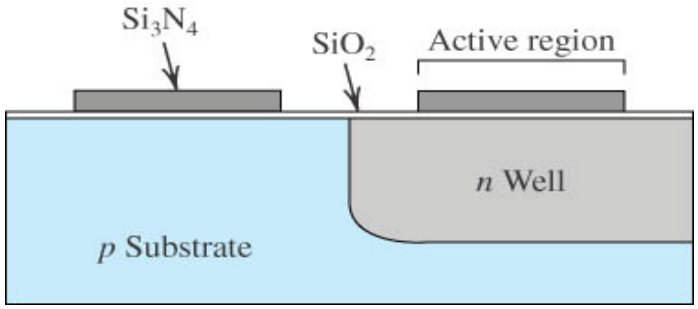
$v_{SGP} = V_{DD} - v_I$

Processo tecnologico CMOS (1/2)

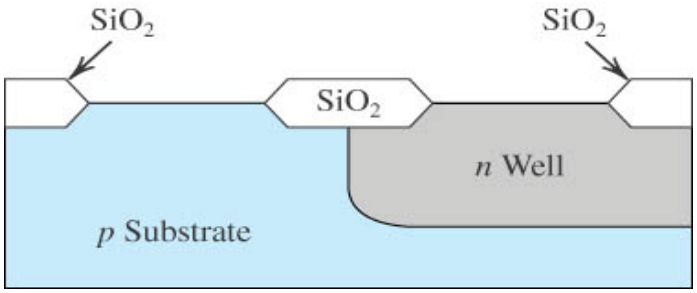
(a) Define *n*-well diffusion (mask #1)



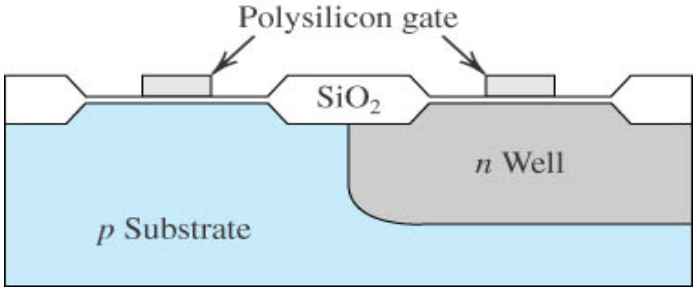
(b) Define active regions (mask #2)



(c) LOCOS oxidation

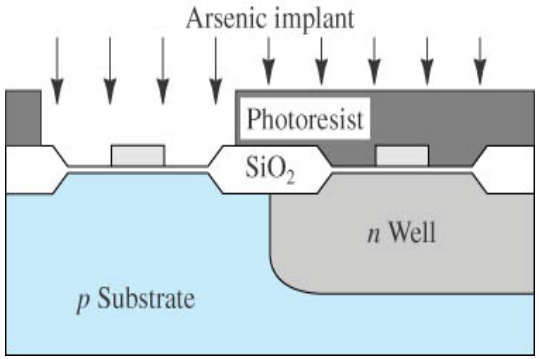


(d) Polysilicon gate (mask #3)

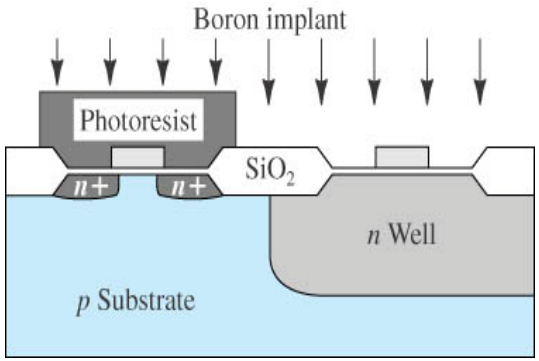


Processo tecnologico CMOS (2/2)

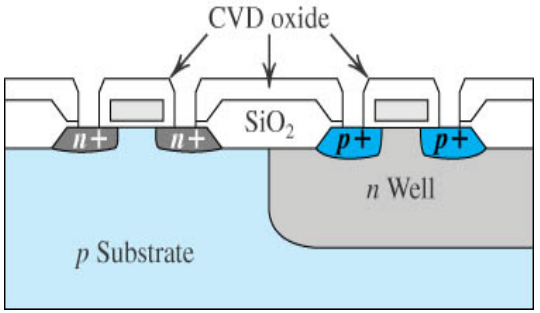
(e) *n*+ diffusion (mask #4)



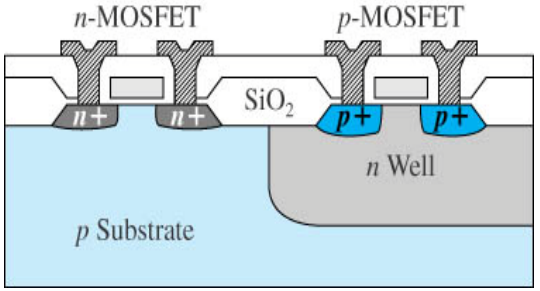
(f) *p*+ diffusion (mask #5)



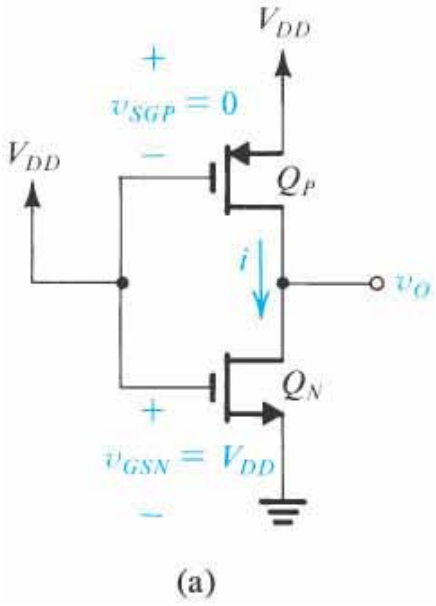
(g) Contact holes (mask #6)



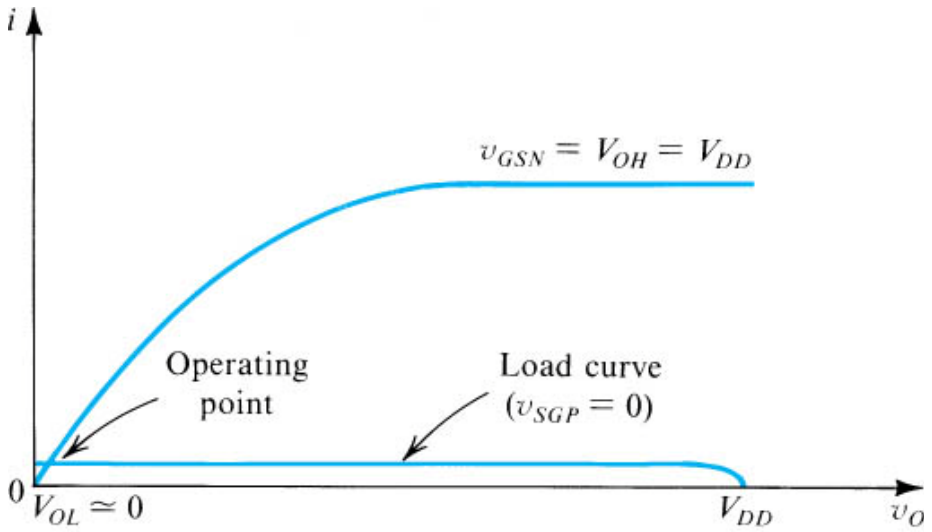
(h) Metallization (mask #7)



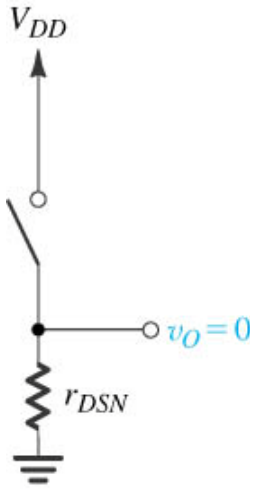
Funzionamento dell'invertitore CMOS (1/2)



(a)



(b)



(c)

$v_I = V_{DD}$ → ingresso alto

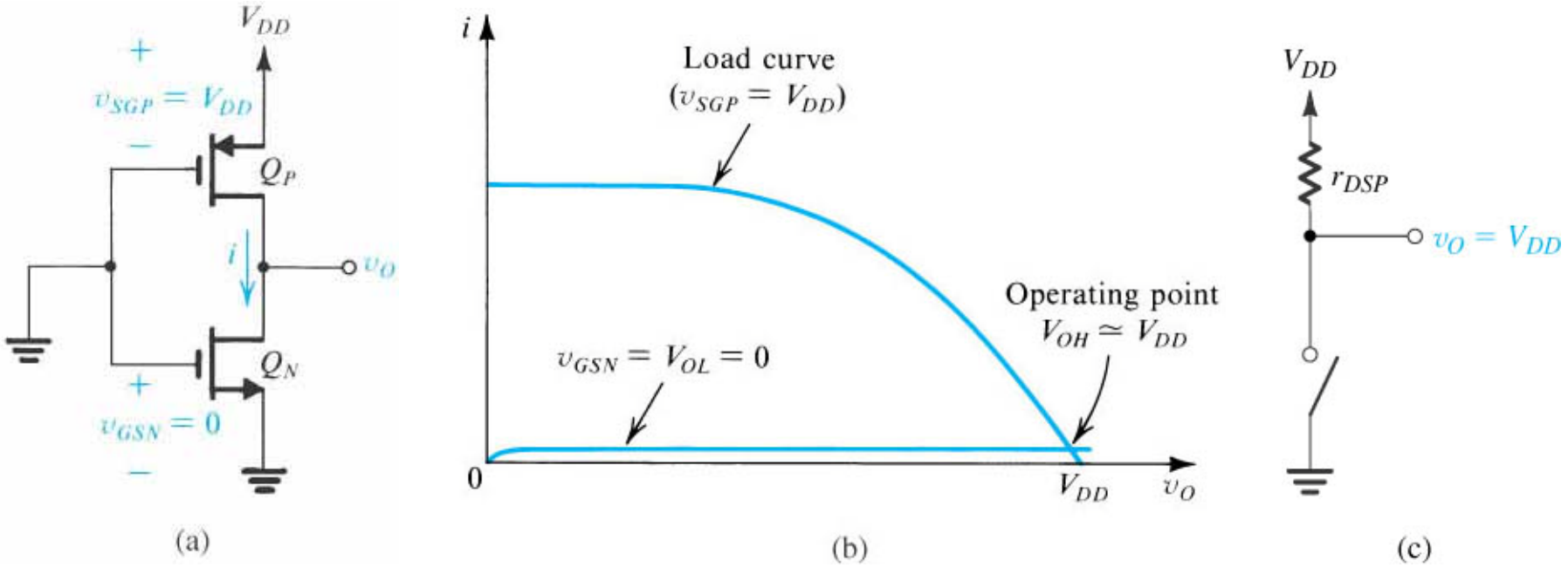
$v_{GSN} = V_{DD}$ → Q_N conduce

$v_{SGP} = 0$ → Q_P interdetto

$i_{DP} = i_{DN}$ @0 → corrente nulla

V_{OL} @0 → uscita bassa

Funzionamento dell'invertitore a CMOS (2/2)



$v_I = 0$ → ingresso basso

$v_{GSN} = 0$ → Q_N interdetto

$v_{SGP} = V_{DD}$ → Q_P conduce

$i_{DP} = i_{DN}$ @0 → corrente nulla

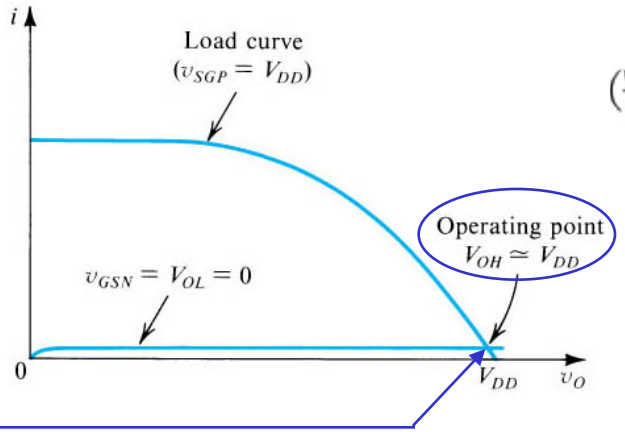
V_{OH} @V_{DD} → uscita alta

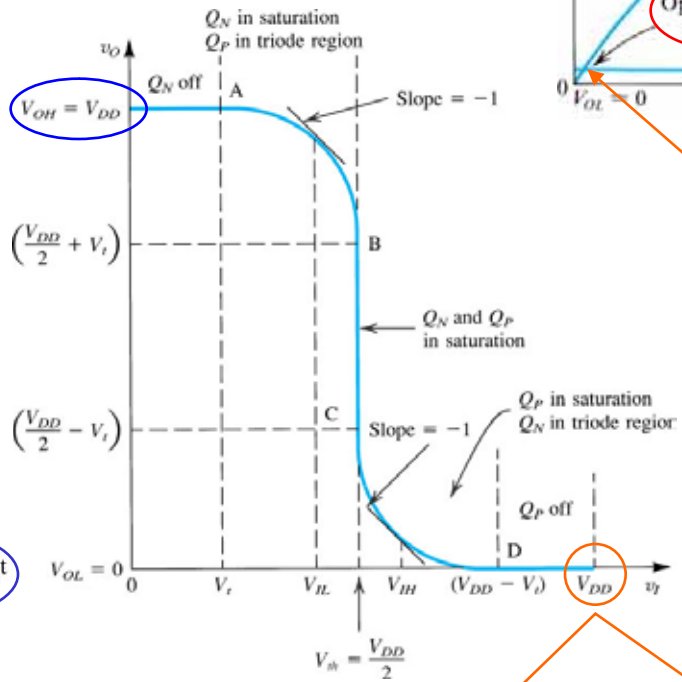
Caratteristica di trasferimento di tensione dell'invertitore a CMOS (1/2)

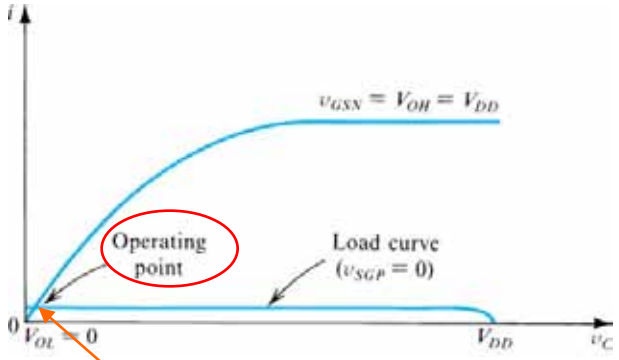
$$\begin{cases} v_I = v_{GSN} = V_{OL} = 0 \\ v_{SGP} = V_{DD} - v_I = V_{DD} \end{cases}$$

Q_N interdetto, Q_P in triodo

$$i = i_{DP} = i_{DN} = 0$$
$$v_O = v_{DSN} = V_{DD} = V_{OH}$$





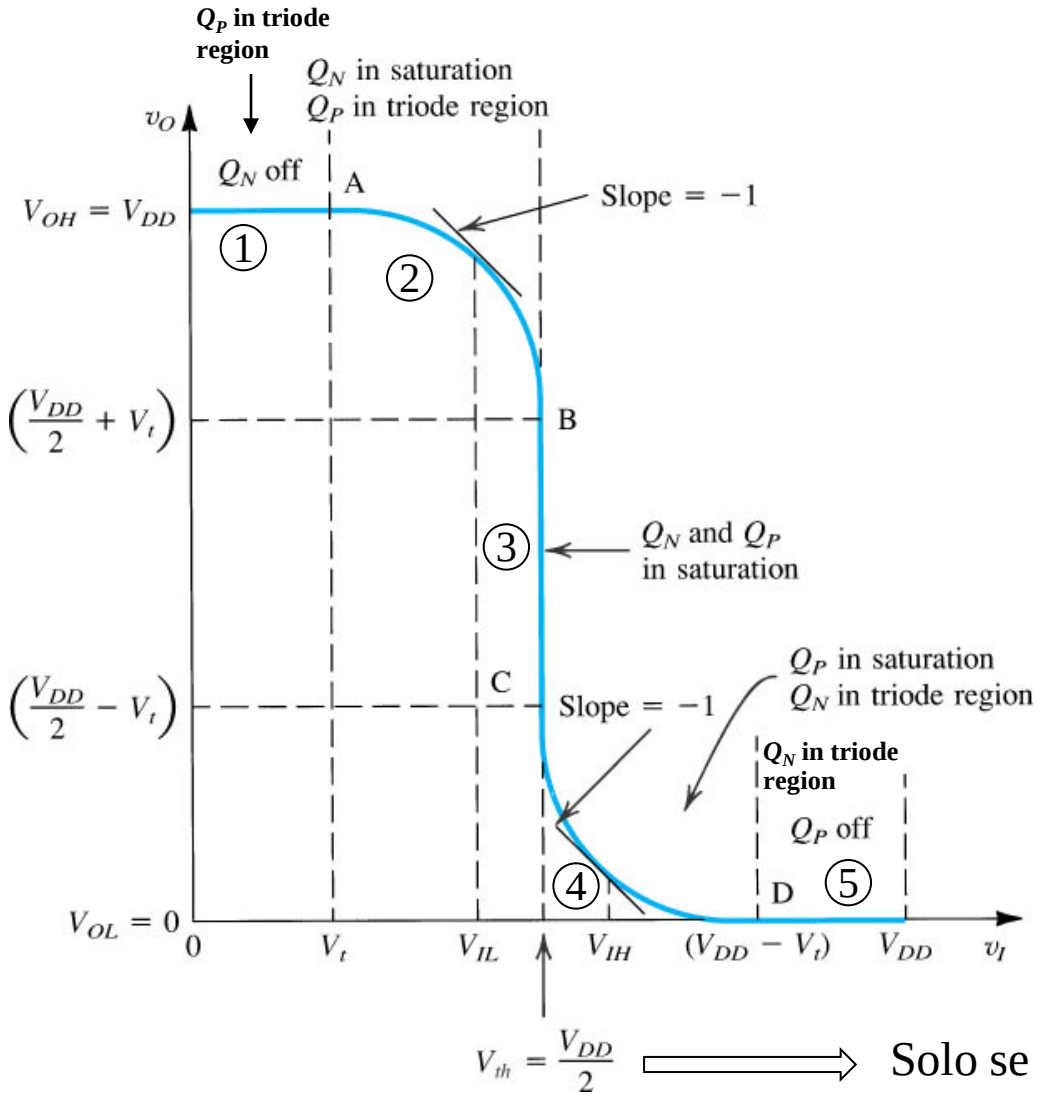


$$\begin{cases} v_I = v_{GSN} = V_{OH} = V_{DD} \\ v_{SGP} = V_{DD} - v_I = 0 \end{cases}$$

Q_N in triodo, Q_P interdetto

$$i = i_{DP} = i_{DN} = 0$$
$$v_O = v_{DSN} = 0 = V_{OL}$$

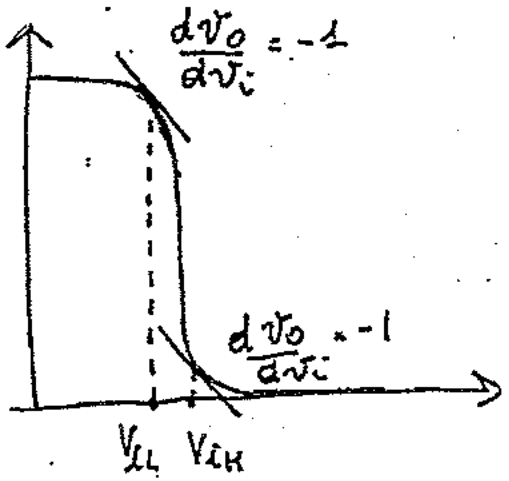
Caratteristica di trasferimento di tensione dell'invertitore a CMOS (2/2)

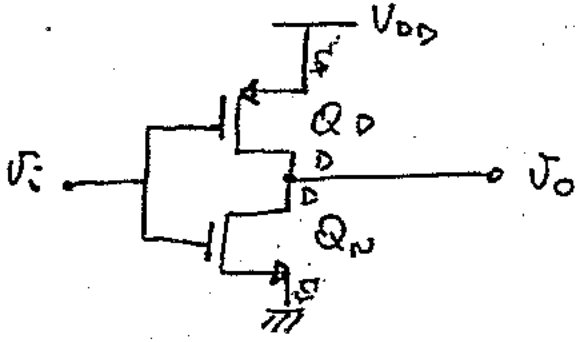


Solo se $K_n = K_p$

Margine di rumore dell'invertitore a CMOS

- $V_{OH} = V_{DD}$ $\quad V_{OL} = \emptyset$
- Quindi dobbiamo definire solo V_{iH} e V_{iL}





- CONDIZIONE $= \dfrac{dv_o}{dv_i} = -1 \Rightarrow$ SCRIVIAMO V_o IN FUNZIONE DI V_i

Margine di rumore dell'invertitore a CMOS

V_{iL} ⇒ IN QUESTA REGIONE DI FUNZIONAMENTO: Q_N SATURO & Q_P TRIODO

$$\begin{cases} V_{in} = V_{GS}^{(Q_N)} & V_{out} = V_{DS}^{(Q_N)} \\ -V_{GS}^{(Q_P)} = V_{DD} - V_{in} & -V_{DS}^{(Q_P)} = V_{DD} - V_O \end{cases} \quad \& \quad i_D^{(Q_N)} \equiv i_D^{(Q_P)}$$

$$i_D^{(Q_N)} = \text{SATURO} = K_n \left(V_{in} - V_{Tn} \right)^2 \quad \left(V_{GS} \text{ HO SOSTITUITO} \right)$$

$$i_D^{(Q_P)} = \text{TRIODO} = K_p \left[2 \left(V_{DD} - V_{in} - V_{Tp} \right) \left(V_{DD} - V_O \right) - \left(V_{DD} - V_O \right)^2 \right]$$

(V_{SG} = $V_{DD} - V_{in} - V_{Tp}$, V_{SD} = $V_{DD} - V_O$)

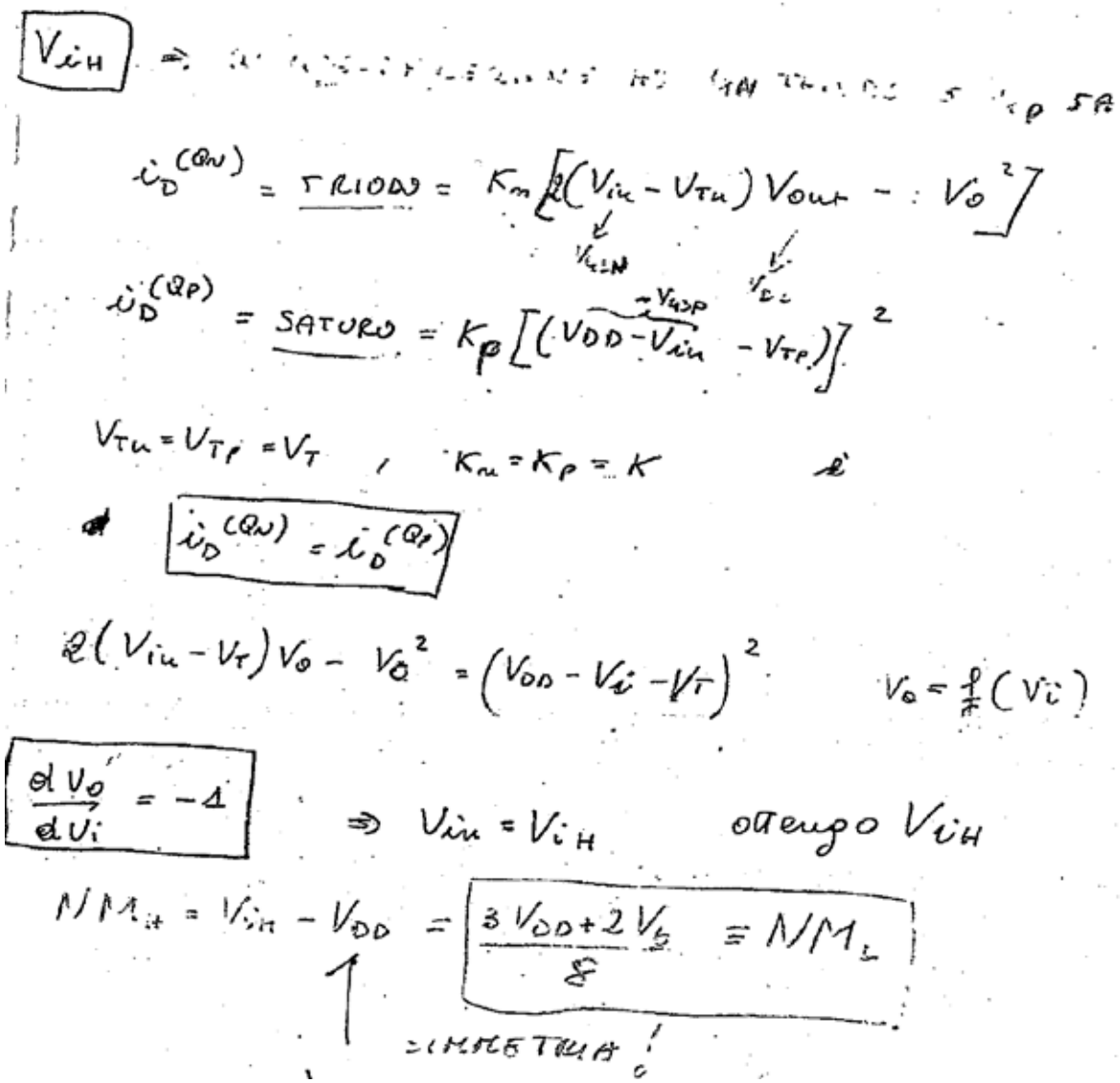
$$i_D^{(Q_N)} \equiv i_D^{(Q_P)} \quad , \quad K_n = K_p = K \quad , \quad V_{Tn} = |V_{Tp}| = V_T$$

$$\left(V_i - V_T \right)^2 = 2 \left(V_{DD} - V_i - V_T \right) \left(V_{DD} - V_O \right) - \left(V_{DD} - V_O \right)^2 \qquad V_O = f(V_i)$$

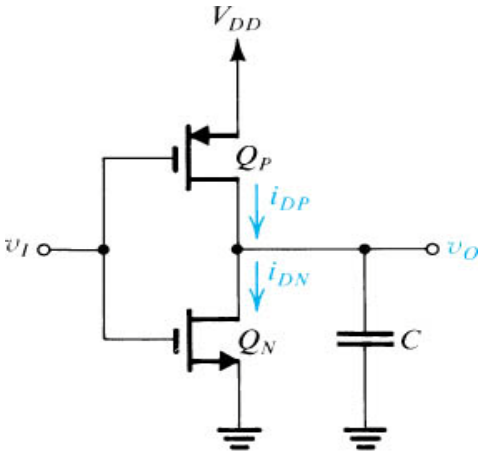
$$\frac{dV_O}{dV_i} = -1 \quad , \text{ pongo } V_i = V_{iL} \text{ & ricavo } V_{iL} \Longrightarrow \quad NM_L = \frac{3V_{DD} + 2V_T}{8}$$

6.3 31.

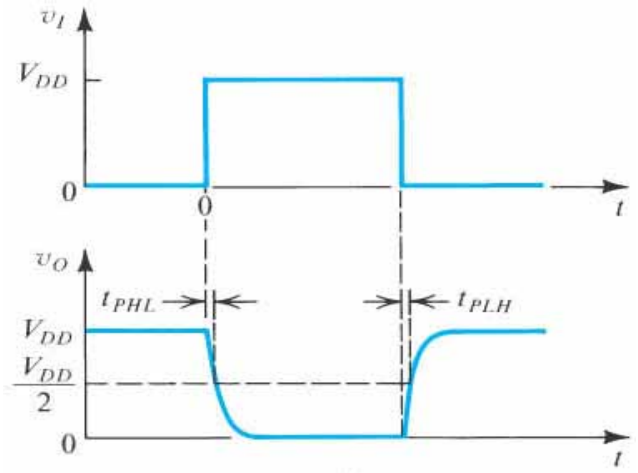
Margine di rumore dell'invertitore a CMOS



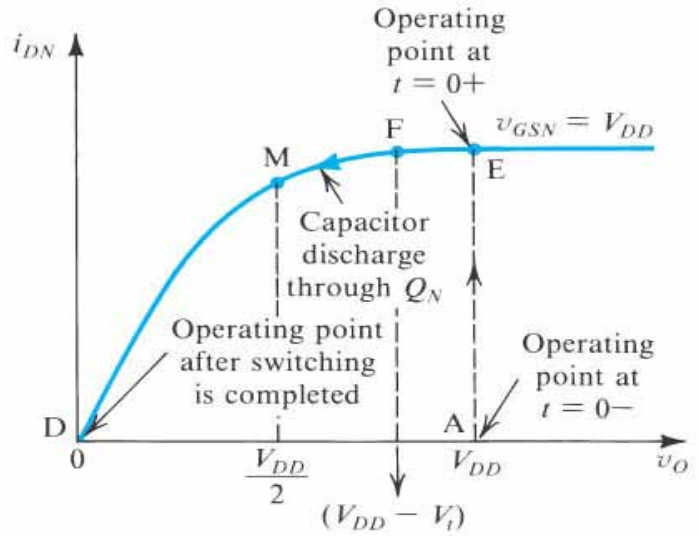
Funzionamento dinamico dell'invertitore CMOS



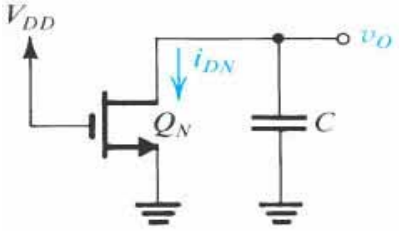
(a)



(b)



(c)



(d)

Funzionamento dinamico dell'invertitore CMOS

0 scarica da E ad F

Q_N pinch-off Q_p OFF

$$i_{DN} = K_n (V_{DD} - V_t)^2$$

$$t_{pHL1} = \frac{C[V_{DD} - (V_{DD} - V_t)]}{K_n (V_{DD} - V_t)^2}$$

$$t_{pHL1} = \frac{C V_t}{K_n (V_{DD} - V_t)^2}$$

Funzionamento dinamico dell'invertitore CMOS

scarica da F ad M

Q_N triodo Q_p OFF

$$i_{DN}\,dt = -C\,dv_O$$

$$i_{DN} = K_n\left[2(v_I - V_{tn})v_O - v_O^2\right] \qquad v_I = V_{DD}$$

$$-\frac{K_n}{C}dt = \frac{1}{2(V_{DD}-V_t)}\cdot\frac{dv_O}{\frac{1}{2(V_{DD}-V_t)}v_O^2 - v_O}$$

$$-\frac{K_n}{C}t_{pHL2} = \frac{1}{2(V_{DD}-V_t)}\cdot\int_{V_{DD}-V_t}^{V_{DD}/2}\frac{dv_O}{\frac{1}{2(V_{DD}-V_t)}v_O^2 - v_O}$$

$$\int\frac{dx}{ax^2-x} = \ln\left(1-\frac{1}{ax}\right)$$

$$t_{pHL2} = \frac{C}{2K_n(V_{DD}-V_t)}\ln\left(\frac{3V_{DD}-4V_t}{V_{DD}}\right)$$

Funzionamento dinamico dell'invertitore CMOS

$$t_{pHL} = t_{pHL1} + t_{pHL2}$$

se $V_t \simeq 0.2\, V_{DD}$

$$t_{pHL} \simeq \frac{0.8\,C}{k_n V_{DD}}$$

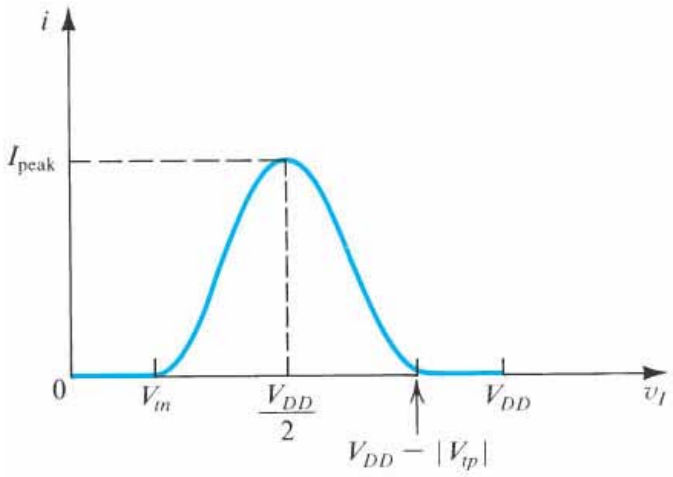
o carica di C (per simmetria)

$$t_{pLH} \simeq \frac{0.8\,C}{k_p V_{DD}}$$

$$DP \simeq f C V_{DD}^2 \cdot \frac{0.8\,C}{k V_{DD}} = 0.8 f \frac{C^2}{k} V_{DD}^2$$

$$\Rightarrow P < 1\,pJ$$

Corrente e potenza dissipata dell'invertitore a CMOS



corrente assorbita nella porta per cambiare stato in funzione della tensione applicata in ingresso

fornisce un contributo trascurabile nella dissipazione dinamica di potenza

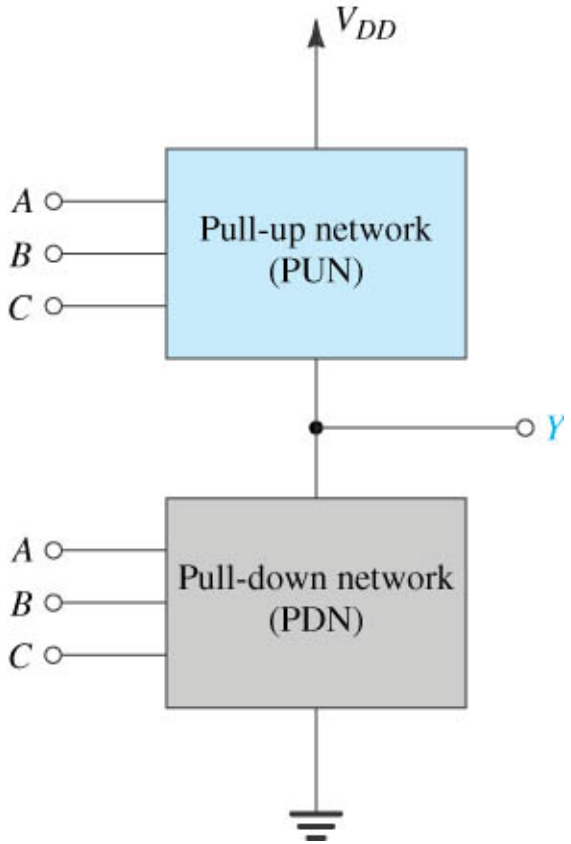
la dissipazione dinamica di potenza è dovuta principalmente ai processi di carica e scarica della capacità di uscita

$$P_D = f C V_{DD}^2$$

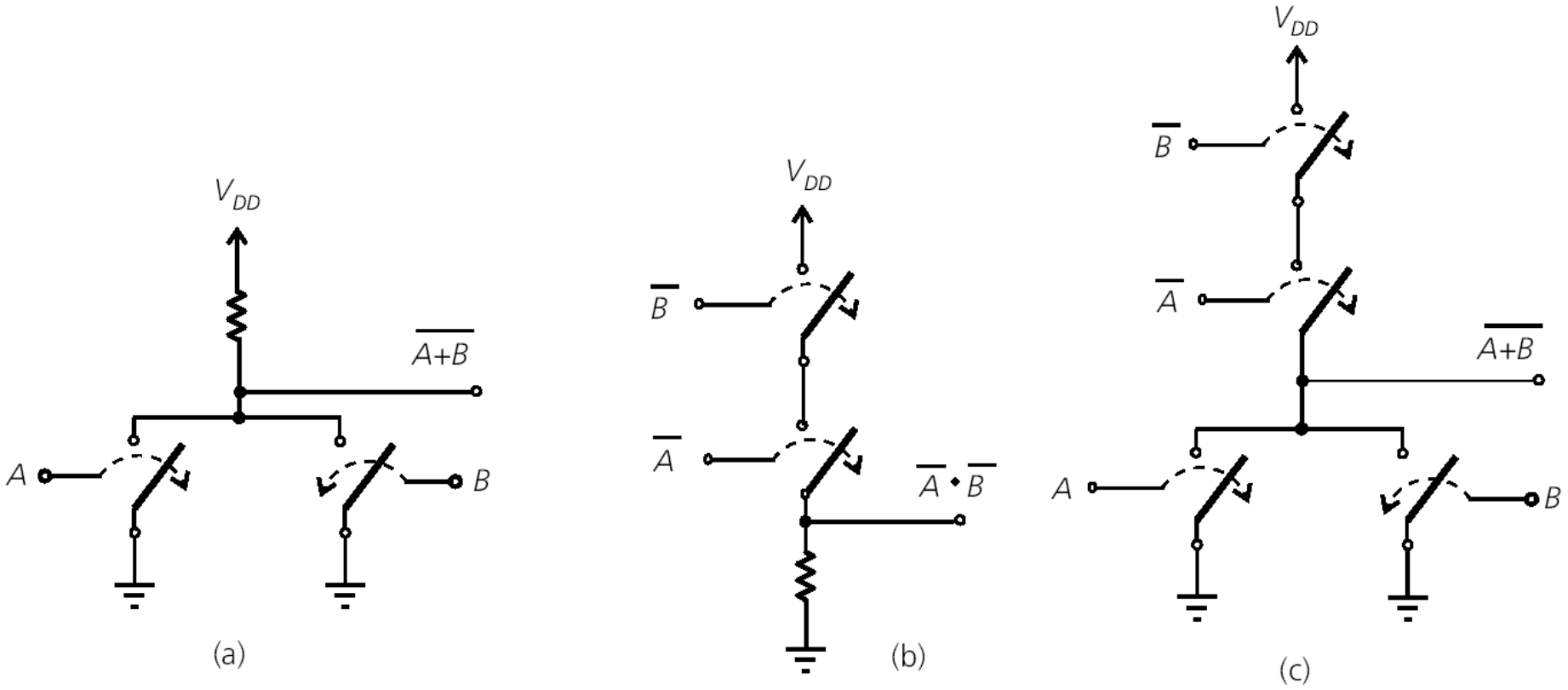
la tecnologia si valuta in base al prodotto ritardo - potenza

$$DP = P_D t_P$$

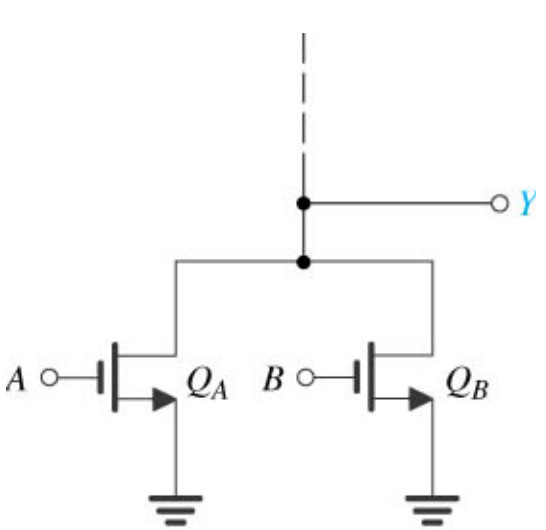
Diagramma a blocchi di una porta logica CMOS a tre ingressi



Funzione NOR con interruttori ideali

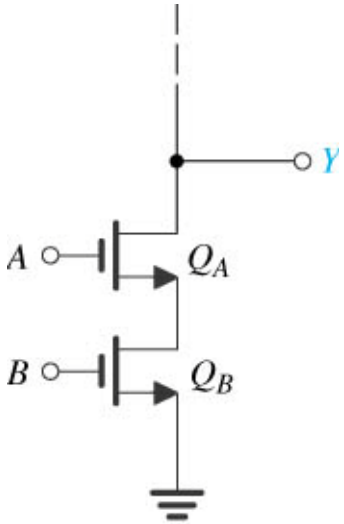


Esempi di reti pull-down



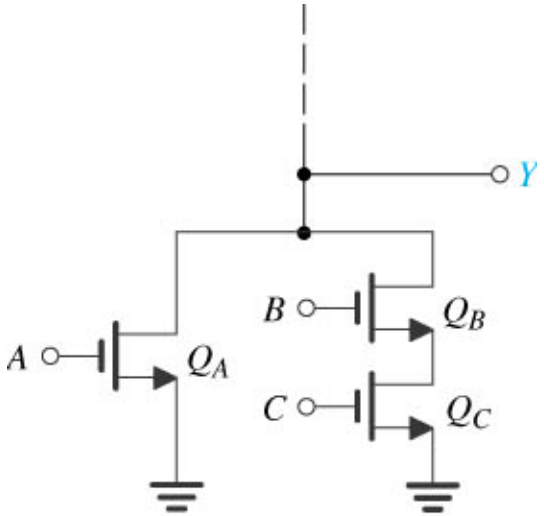
$\overline{Y} = A + B$

(a)



$\overline{Y} = AB$

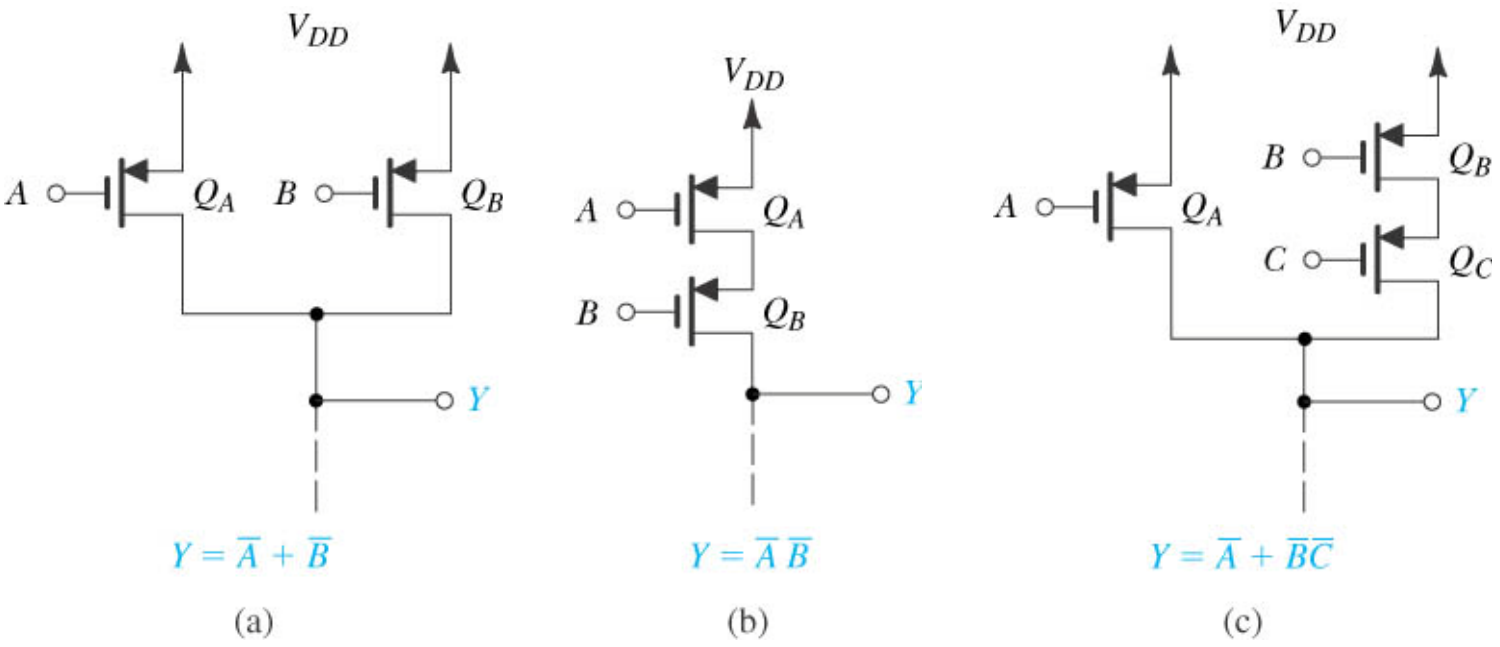
(b)



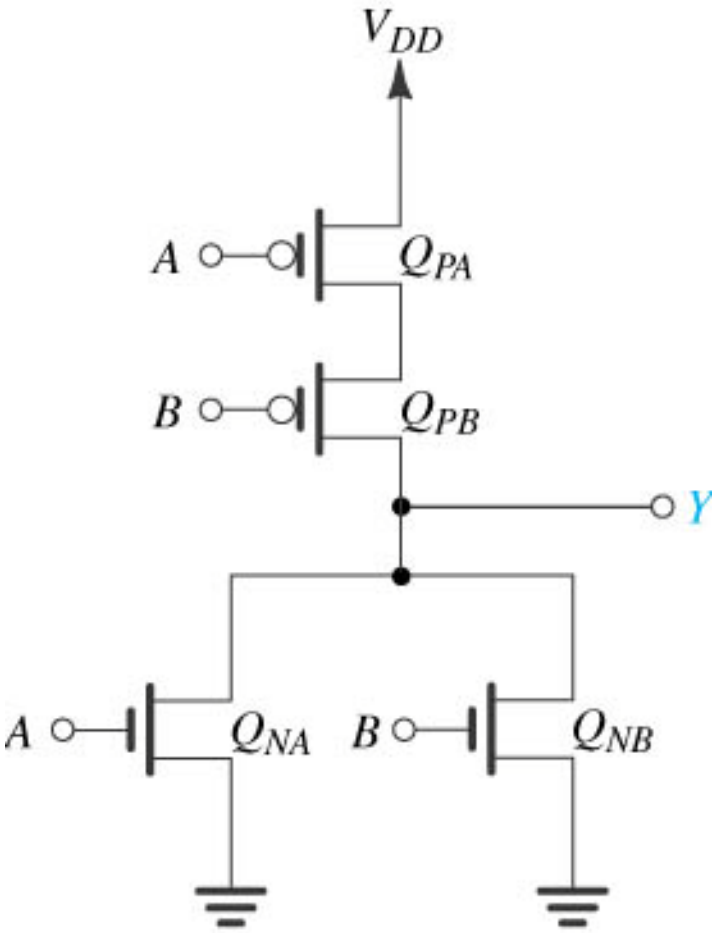
$\overline{Y} = A + BC$

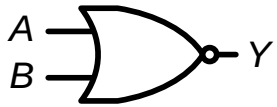
(c)

Esempi di reti pull-up



Porta NOR CMOS a due ingressi





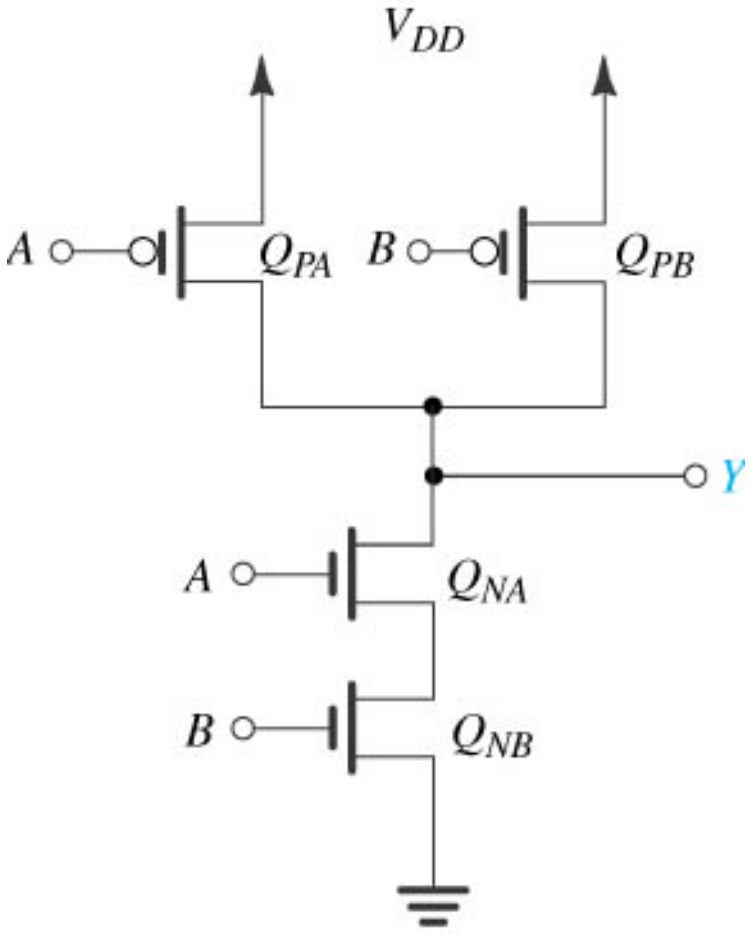
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

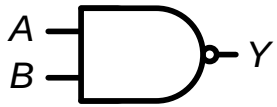
$$Y = \overline{A + B} = \overline{A} \times \overline{B}$$

Q_{PA} , Q_{PB} : PMOS

Q_{NA} , Q_{NB} : NMOS

Porta NAND CMOS a due ingressi





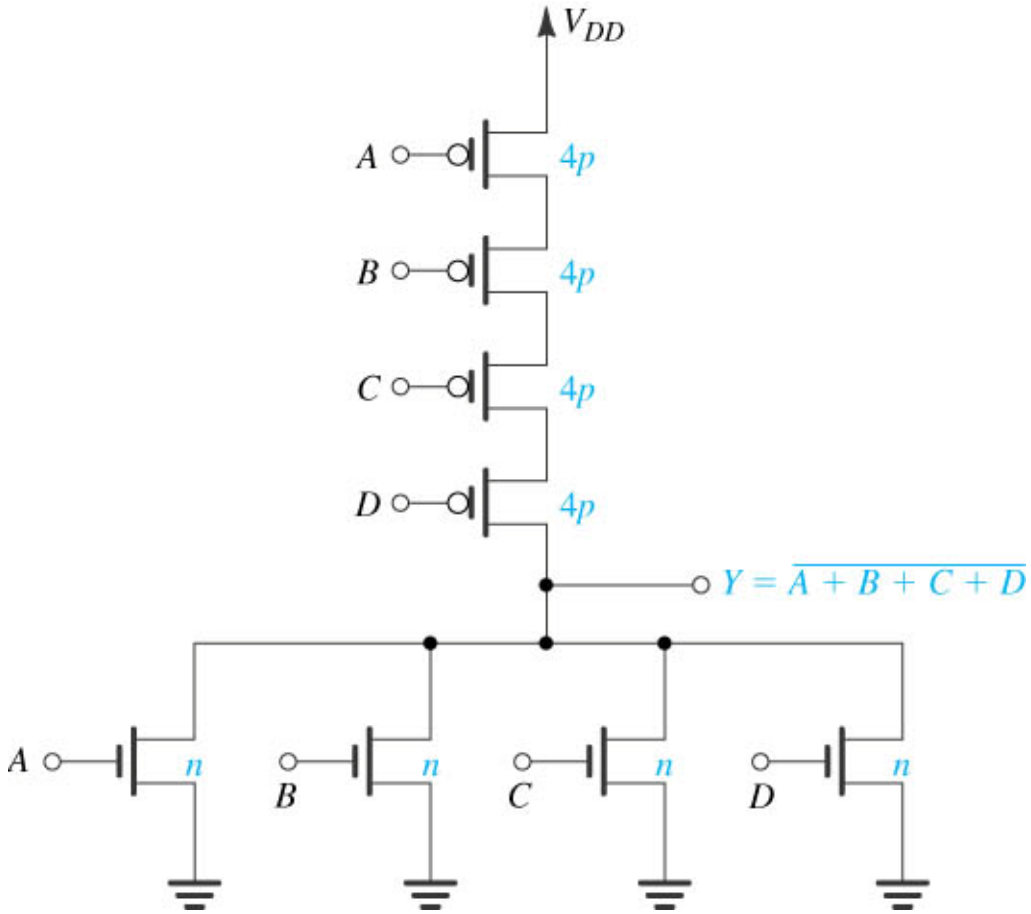
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

$$Y = \overline{A \times B} = \overline{A} + \overline{B}$$

Q_{PA} , Q_{PB} : PMOS

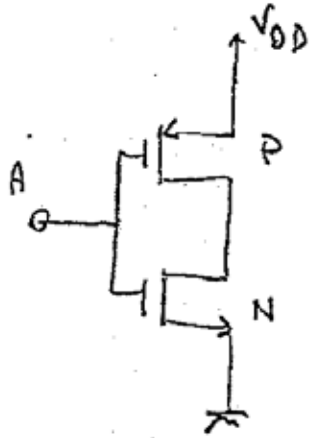
Q_{NA} , Q_{NB} : NMOS

Dimensionamento dei transistori per una porta NOR a quattro ingressi



Dimensionamento dei transistori per una porta NOR a quattro ingressi

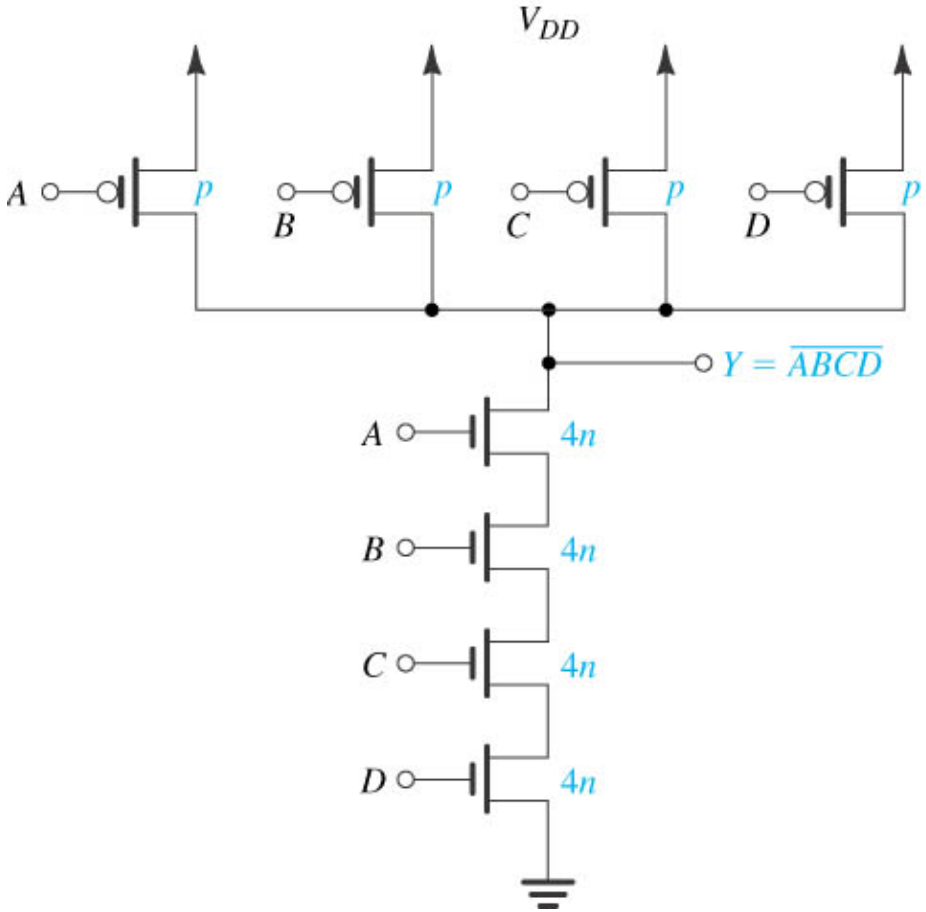
- WORST CASE DESIGN 1 solo ingresso alto: la capacità di uscita si scarica attraverso l'unico NMOS ON



$$K_{P,eq} = \frac{K_P}{N}$$

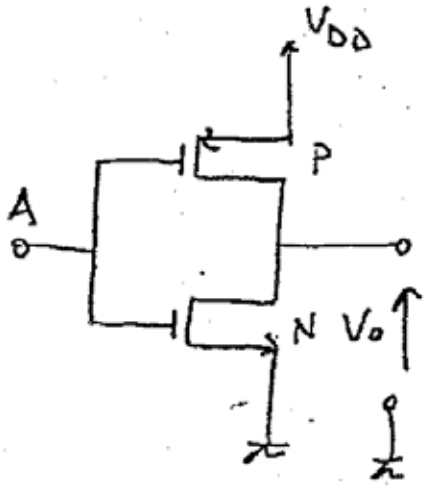
$$K_{N,eq} = K_N$$

Dimensionamento dei transistori per una porta NAND a quattro ingressi



Dimensionamento dei transistori per una porta NAND a quattro ingressi

WORST CASE DESIGN 1 solo ingresso basso: carica della capacità di uscita avviene tramite un solo PMOS ON



$$K_{P,eq} = K_P$$

$$K_{N,eq} = \frac{K_N}{N}$$

Dimensionamento dei transistori per una porta NAND a quattro ingressi

- NOR

$$\frac{1}{2}\mu_p C_{ox}\frac{W_p}{N L_p} = \frac{1}{2}\mu_n C_{ox}\frac{W_N}{L_N}$$

$$\frac{W_p}{N L_p} = 2.5\,\frac{W_N}{L_N}$$

se $L_N = L_p = F \Rightarrow \quad W_p = 2.5\,N\,W_N$

- NAND

$$\frac{1}{2}\mu_p C_{ox}\frac{W_p}{L_p} = \frac{1}{2}\mu_n C_{ox}\frac{W_N}{N L_N}$$

$$\frac{W_p}{L_p} = 2.5\,\frac{W_N}{N L_N}$$

se $L_N = L_p = F. \Rightarrow \quad W_N = \frac{N W_p}{2.5}$

Dimensionamento dei transistori per una porta NAND a quattro ingressi

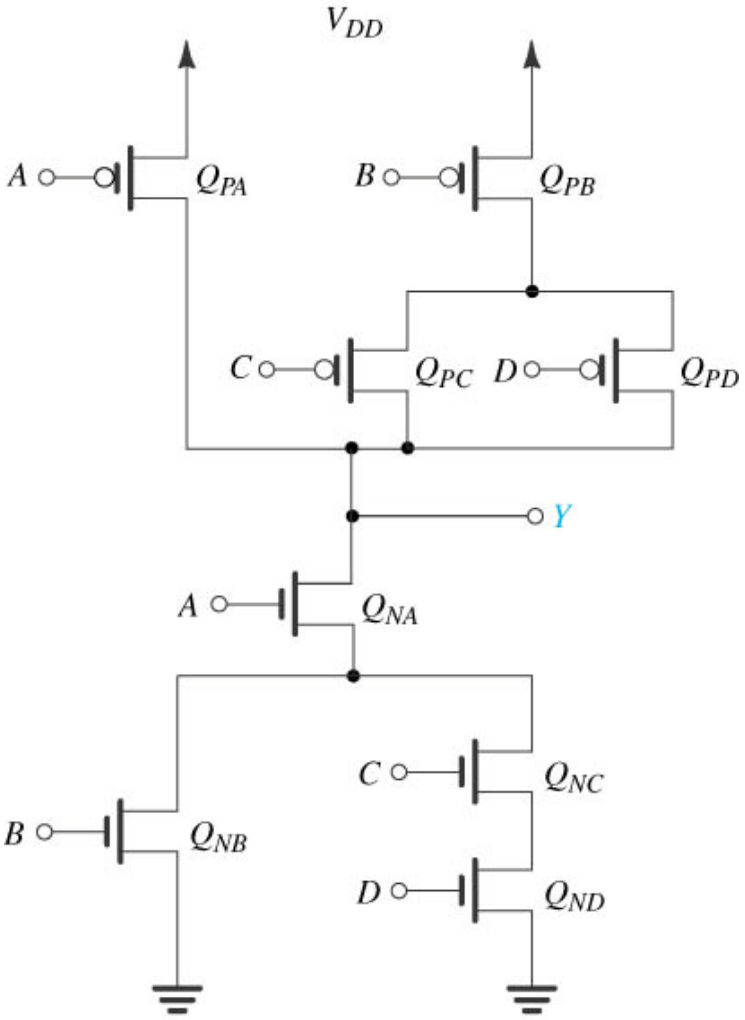
$$\text{Area minima NOR} = N W_N L_N + N W_P L_P = N\left(W_N F + 2.5 N W_N F\right) = N\left(\overbrace{W_N F}^{A_{min}} + 2.5 N W_N F\right) =$$

$$= N A_{min}\left(1 + 2.5 N\right)$$

$$\text{Area minima NAND} = N W_P L_P + N W_N L_N = N\left(W_P F + N\overbrace{\frac{W_P}{2.5} F}^{A_{min}}\right) =$$

$$= N A_{min}\left(2.5 + N\right)$$

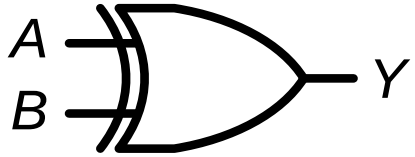
Realizzazione di una porta complessa CMOS



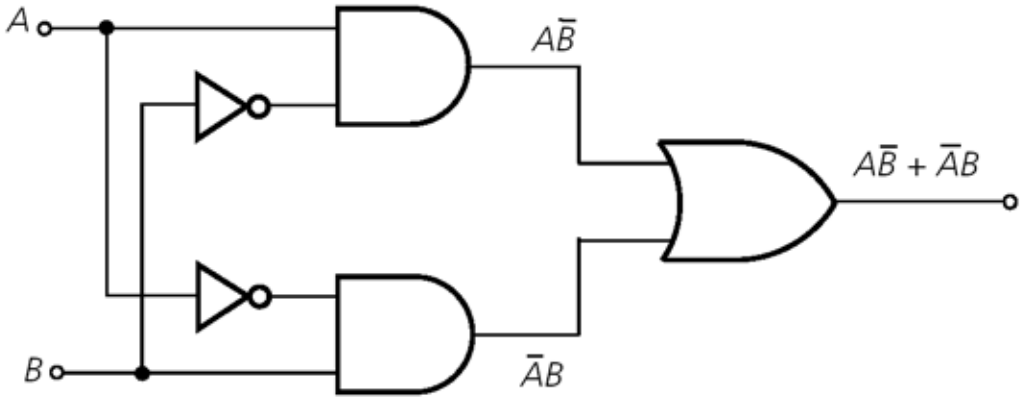
$Y = \overline{A(B + CD)}$

OR-esclusivo (XOR)

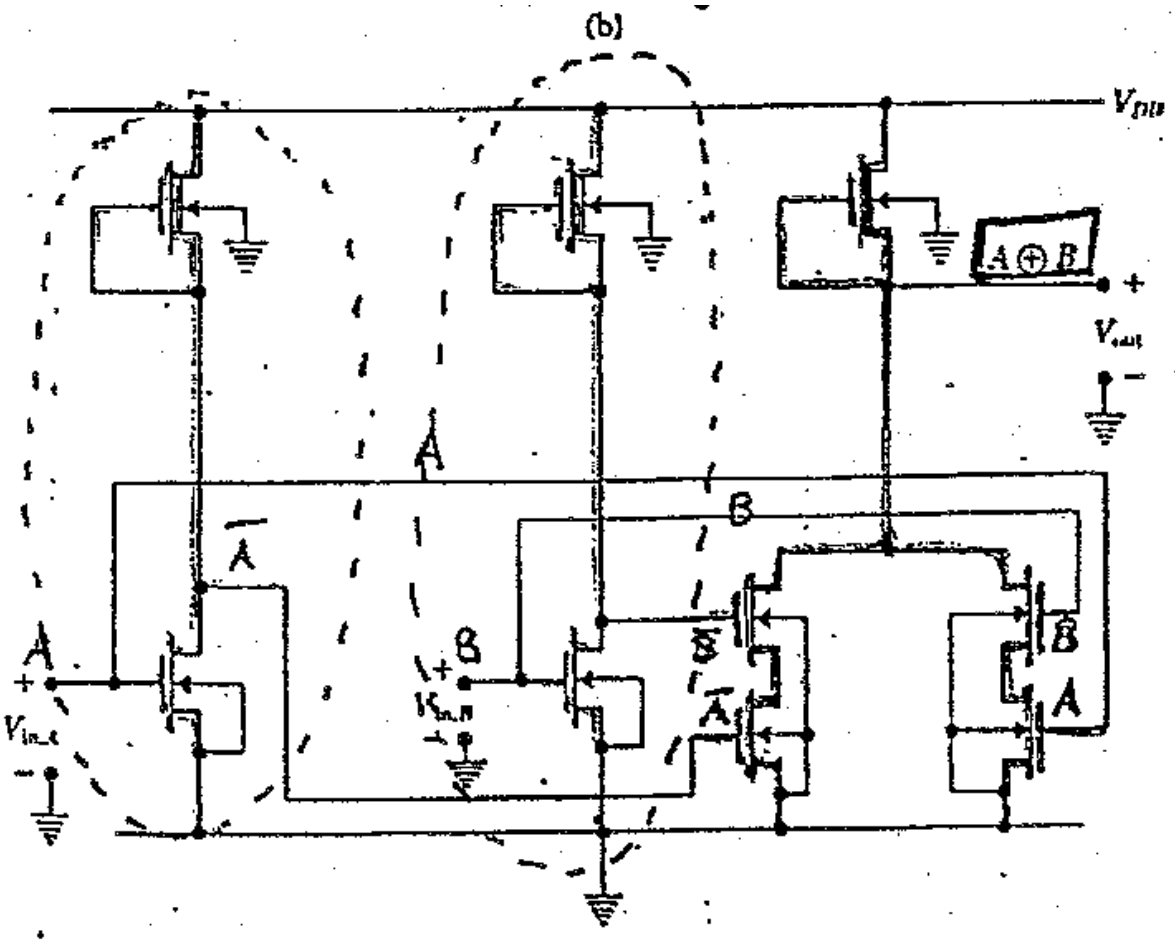
A	B	Y	
0	0	0	
0	1	1	$\rightarrow \overline{A}B$
1	0	1	$\rightarrow A\overline{B}$
1	1	0	



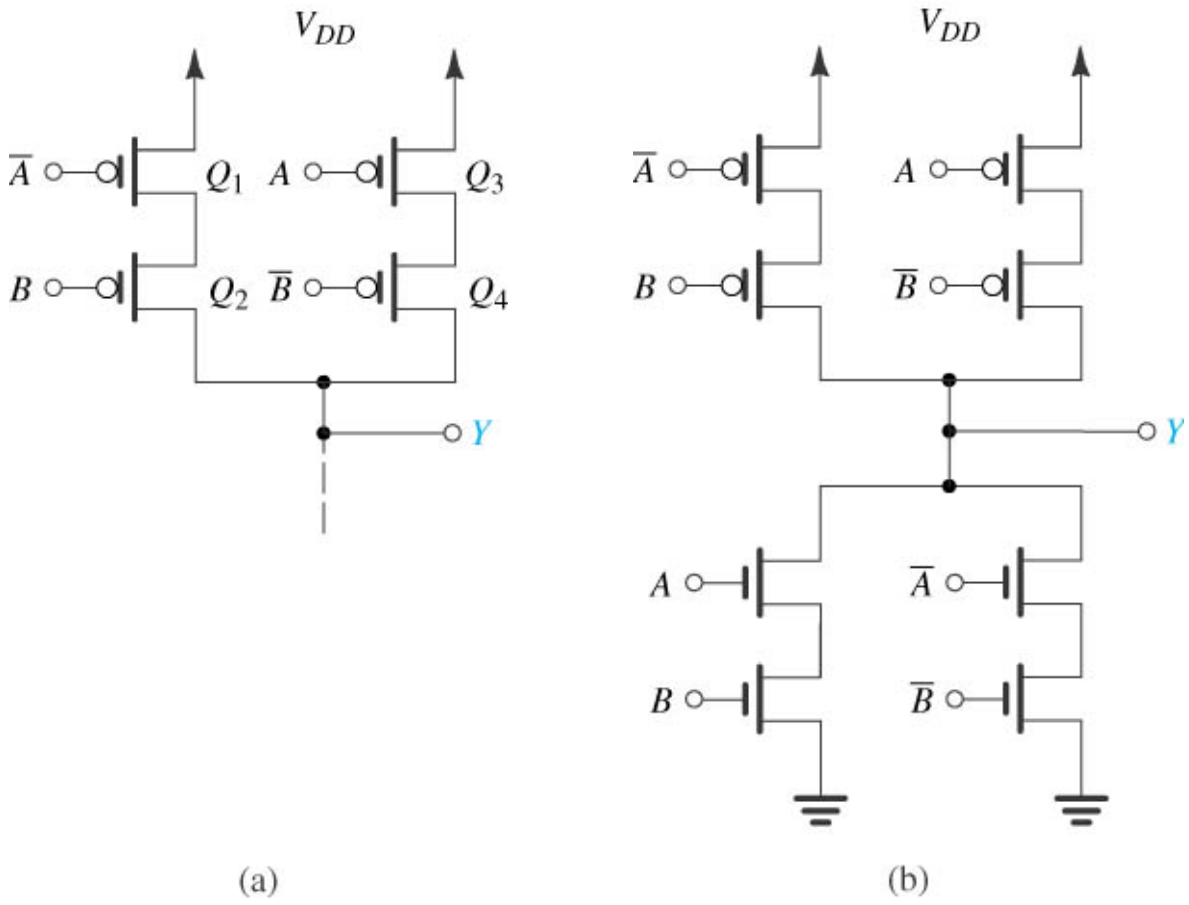
$$Y = A \text{Å } B = A\overline{B} + \overline{A}B$$



OR-esclusivo (XOR)

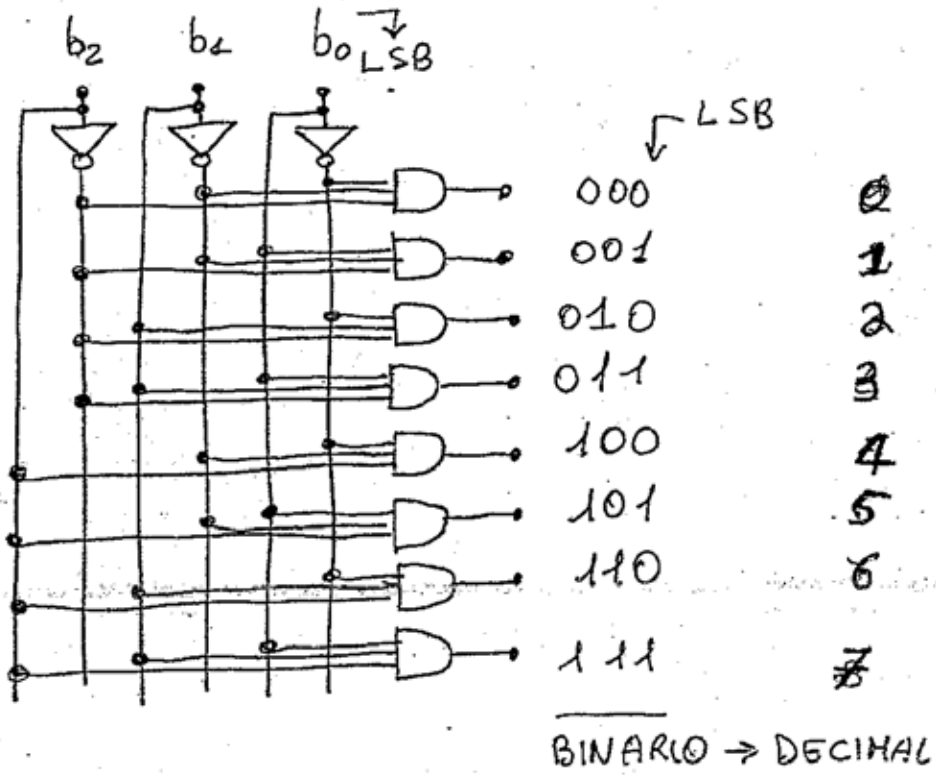


Realizzazione della funzione OR-esclusiva (XOR)



Decodificatore

DECODER = INTERPRETA UN CODICE DI n BIT
E ATTIVA UNA USCITA (TRA 2n)
CHE CORRISPONDE ALLA PAROLA IN INGRESSO



Decodificatore

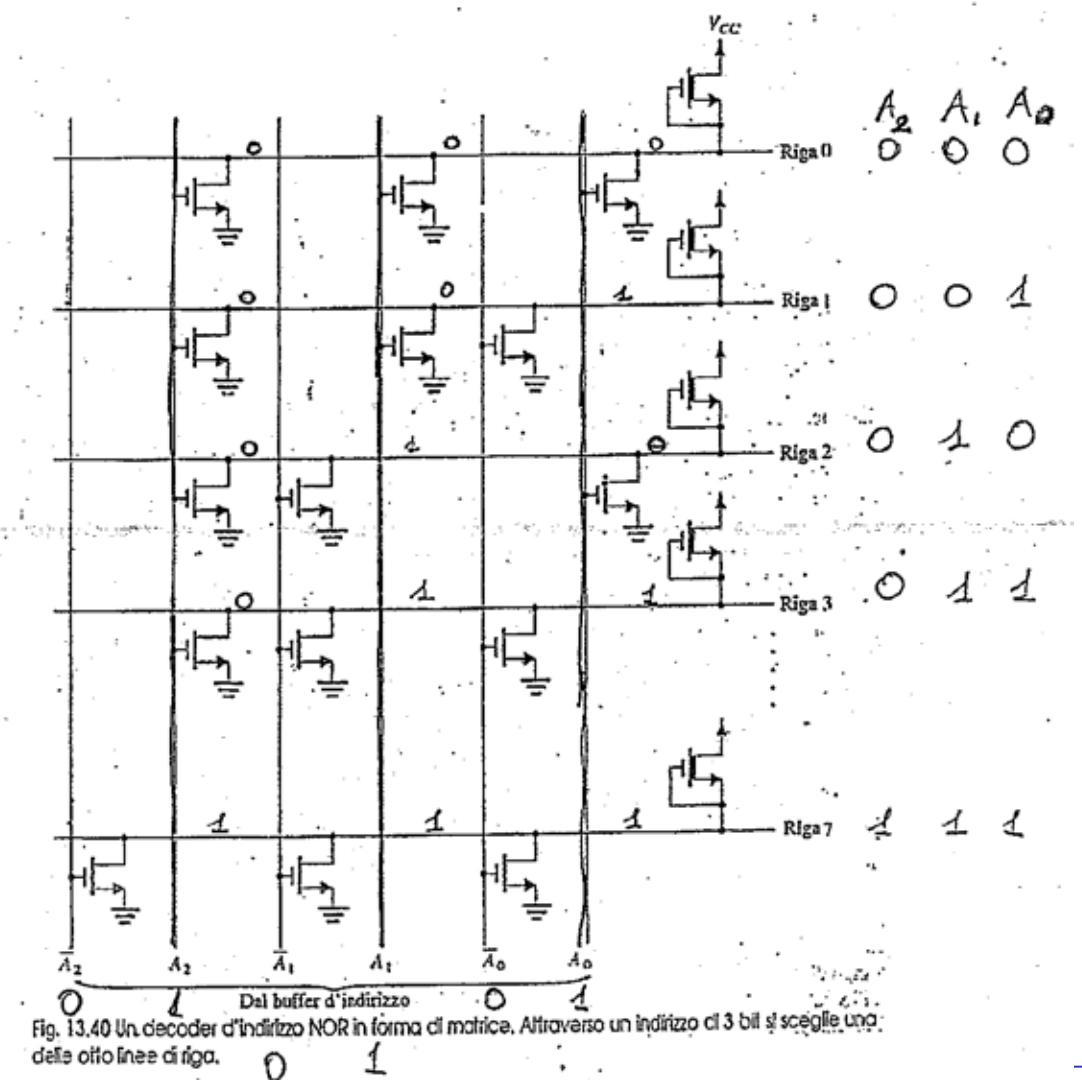
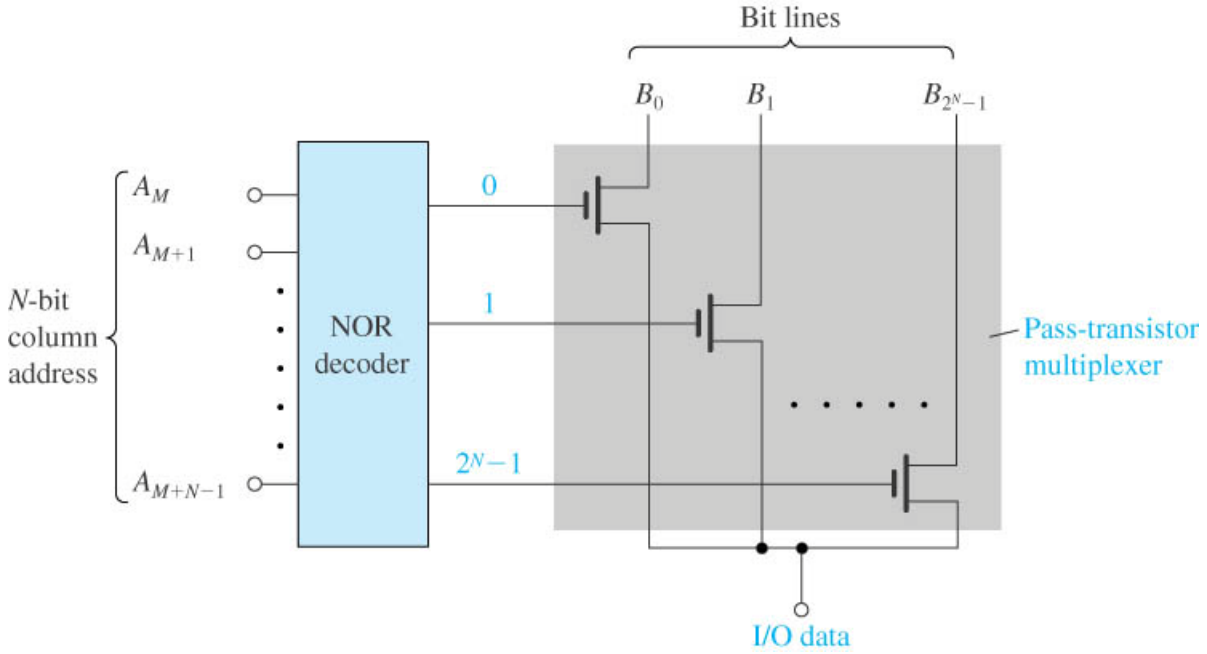


Fig. 13.40 Un decoder d'indirizzo NOR in forma di matrice. Attraverso un indirizzo di 3 bit si sceglie una delle otto linee di riga.

Decodificatore di indirizzi di colonna a CMOS



Tecnologia MOS complementare (CMOS)