Optimal Design of a Dual-Active-Bridge DC–DC Converter

Dibakar Das, *Student Member, IEEE*, and Kaushik Basu, *Senior Member, IEEE*

***Abstract*—This article presents a systematic design procedure for a dual-active-bridge (DAB) dc–dc converter. Design of a DAB converter involves determination of two key parameters, i.e., transformer turns ratio and the series inductance value. Existing literature addresses this problem through numerical optimization, which is computation intensive and does not provide much insight. In general, loss is minimized by applying equal weightage to all operating conditions, which may not be practical. Given an operating power range, terminal voltage range, and switching frequency, this article presents a way to optimally select the design variables through analytical solution of a constrained optimization problem. Analysis is carried out in the time domain, and an optimal triple-phase-shift modulation strategy is considered that ensures minimum inductor rms current and soft switching. The choice of the design parameters results in minimization of the worst-case inductor rms current over the entire operating range of the converter, which leads to both efficiency and size optimization. A procedure for selection of devices and filter capacitors and design of magnetics is given. A 2.6-kW experimental prototype is designed to validate the theoretical analysis.**

***Index Terms*—Dual active bridge (DAB), optimal design, RMS current minimization, soft switching, triple-phase-shift (TPS) modulation.**

Nomenclature

V_1	Voltage of the controlled port.
V_2	Voltage of the uncontrolled port.
i_L	Instantaneous inductor current.
I_{rms}	Actual value of inductor rms current.
i_{rms}	Scaled value of inductor rms current.
P	Average power transferred between the dc ports.
p	Scaled value of average transferred power.
f_s	Switching frequency of the converter.
n	Turns ratio of the transformer.
L	Total series inductance of the DAB converter.
d_1	Duty cycle of primary voltage waveform.
d_2	Duty cycle of secondary voltage waveform.
δ	Phase shift between primary and secondary voltage waveforms.
m	Voltage conversion ratio.

Manuscript received May 29, 2020; revised September 13, 2020 and November 10, 2020; accepted November 26, 2020. Date of publication December 23, 2020; date of current version August 25, 2021. This work was supported by the Indian Space Research Organisation, Government of India, under the project entitled "Development of ac power system for satellite applications." *(Corresponding author: Dibakar Das.)*

The authors are with the Department of Electrical Engineering, Indian Institute of Science, Bangalore 560012, India (e-mail: dibakard@iisc.ac.in; kbasu@iisc.ac.in).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TIE.2020.3044781.

Digital Object Identifier 10.1109/TIE.2020.3044781

I. Introduction

DUAL active bridge (DAB) converters are a desirable choice in dc–dc power conversion, since they have several beneficial features such as galvanic isolation, bidirectional power flow capability, soft switching leading to high efficiency, and power density [1]. These converters are used in several applications such as dc microgrids, battery chargers, solid-state transformers, etc.

In the DAB topology, two H-bridge converters apply square waveforms to transformer primary and secondary windings in series with an inductor. A phase shift is introduced between the waveforms for power transfer [2]. This modulation strategy is known as single-phase-shift (SPS) strategy in the literature. Later, it was found that introducing duty modulation in primary and secondary voltages can lead to several advantages [3]. This three-degree-of-freedom modulation (two duty cycles and phase shift) is known as triple-phase-shift (TPS) strategy in the literature [3]. The TPS strategy is considered in this article.

Several methods exist in literature, which address the optimal modulation problem based on minimization of a given objective function. In such problems, for a specified operating condition (power, voltage, and switching frequency) and a given design (transformer turns ratio and series inductance value), the objective is to determine the TPS modulation parameters, which will minimize power loss. For loss minimization, one popular approach is using fundamental approximation [4]–[7] of the voltage and current waveform and minimize the circulating [4], [5] or reactive component [6], [7] of the inductor current. Although this approach leads to a simpler analysis, the approximations may not be valid over a wide operating range of the converter. A more general method that results in accurate prediction over a wide range of operation is to use time-domain expressions for power and inductor current [3], [8]–[10].

Considering time-domain analysis, the objective function for minimization may be inductor rms current [8]–[10], peak current [11]–[15], soft switching [3], [16], or total loss [17]–[19]. Out of the above alternatives for the objective function, the rms of the inductor current with soft switching is a suitable candidate for optimization because it represents the conduction losses in the devices and the magnetic components, which form a major fraction of the total loss of the converter [8]. Moreover,

reducing the rms of inductor current also implies reduction of peak currents and capacitor ripple current ratings.

Several approaches for minimization of rms currents through time-domain exact analysis can be found in the literature. A numerical approach for choosing optimal TPS parameters can be found in [8]. The proposed strategy has three regions of operation based on the power output of the converter. A more formal treatment of the rms current minimization problem and an analytical solution can be found in [10]. Though soft switching is not included in the problem formulation, it is shown that the results satisfy the soft switching constraints.

In a typical dc–dc converter, the voltage at one port is tightly regulated despite variations in the other port voltage. The design specifications include voltage at the regulated port, the range of unregulated port voltage, range of operating power, and the switching frequency [20]–[22]. Design of the DAB dc–dc converter involves determining the turns ratio of the transformer and the series inductance [19], [23], [24]. Based on the worst-case stresses on the components, the design of magnetic components and selection of switches and capacitors can then be carried out.

In [23], the transformer turns ratio is chosen to obtain voltage conversion ratio of unity at the maximum value of unregulated voltage while applying the SPS strategy for power transfer. The inductance value is chosen to provide good controllability. This method is simple and widely used, but it does not attempt to minimize rms inductor current or losses. In [24], a numerical design approach is adopted for selection of optimal transformer turns ratio and inductance value for minimization of rms inductor current averaged over several operating voltages at fixed power. The same method is used to minimize peak inductor current or total power loss, which provide separate design parameter values. The SPS strategy is considered for the analysis. It is well known in the DAB literature [3], [8] that SPS results in large rms currents and loss of zero-voltage switching (ZVS) for wide variation of voltage and power. In [19], a numerical approach similar to that in [24] is taken, but TPS with ZVS is considered, and average efficiency is used as an objective function. Search is carried over a range of operating points resulting due to variations in unregulated port voltage and power.

Total loss or efficiency as an objective function is complex and requires knowledge of device- and magnetics-related parameters, which are usually not known before the basic design is completed. In the numerical search technique [19], [24], the search space is divided into discrete points, and the objective function is evaluated at each point to identify the optimum. This process is computation extensive, requires programming effort, and does not provide much insight. Applying equal weightage to each operating point may not be practical.

This article presents a novel analytical design procedure for a DAB dc–dc converter. The design specifications are the regulated port voltage, range of unregulated voltage, operating power range, and switching frequency. The optimal TPS strategy is considered for the analysis, which results in minimum rms current while ensuring soft switching. For accurate results, the minimization problem is formulated considering time-domain analysis. Though it may seem obvious, it is established that maximum rms current with an optimal TPS strategy flows at maximum power. This conclusion is independent of the choice of design parameters and the variation of voltage at the unregulated port. Minimization of the maximum rms current experienced by the converter over the operating range leads to optimal sizing of devices, filter capacitors, and magnetics. A constrained optimization problem to minimize worst-case inductor rms current is formulated and then solved analytically. The first-order necessary conditions are applied on the objective function to obtain algebraic equations for optimal variables. Since a closed-form expression does not exist for one of the equations, a numerical root-finding technique is used to find the optimal value. A polynomial curve fit is then provided for selection of the inductance value, which reduces the computation effort. The solution thus obtained provides optimal values of the design variables (transformer turns ratio and inductance value). The proposed solution results in the maximum rms current (at maximum power) to remain close to its minimum value despite variations of voltage at the uncontrolled port. The optimal TPS strategy can be applied to the optimal design to obtain minimum rms currents and soft switching over the entire operating range of the converter. The key steps in selecting the power devices, filter capacitors, and design of magnetics are also presented.

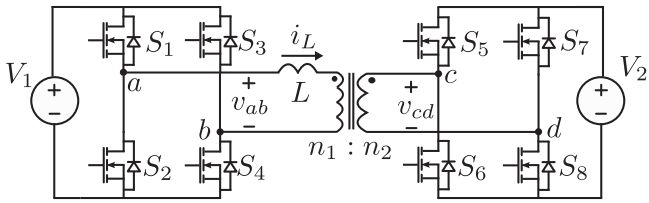

Fig. 1. DAB dc–dc converter.

The rest of this article is organized as follows. Section II describes the design problem and modeling of the converter for various zones of operation. An optimization problem is formulated for rms current minimization. A systematic procedure is discussed for the choice of design parameters. Section III demonstrates the experimental results with the proposed design strategy. Section IV concludes this article.

II. Analysis and Optimal Design

Consider the DAB dc–dc converter transferring power P between dc voltage sources V_1 and V_2 and switching at frequency f_s shown in Fig. 1. The two H-bridge converters convert the dc voltages V_1 and V_2 to duty-modulated square waveforms v_{ab} and v_{cd}, respectively. These waveforms are then applied to a transformer connected in series with an inductor. The switches of the H-bridge converters are considered ideal, and the effect of transformer magnetizing inductance is neglected in the analysis. The inductor L in Fig. 1 is the transformer leakage inductance along with the external inductance. The converter can thus be equivalently replaced by two voltage sources and an inductor L, as shown in Fig. 2(a). The power transfer between dc ports is carried out by introducing a phase shift between v_{ab} and v_{cd}.

A DAB converter can be modulated with three degrees of freedom. The primary and secondary voltage waveforms can

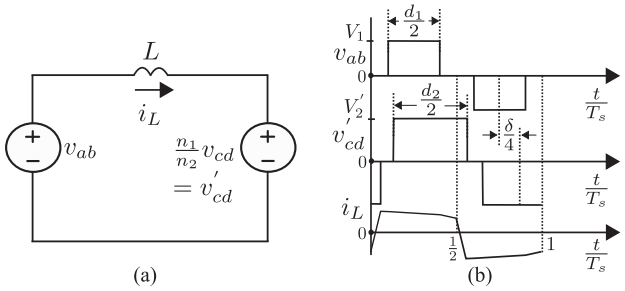

Fig. 2. (a) Equivalent circuit of DAB. (b) Typical v_{ab}, v'_{cd}, and i_L waveforms with three-degree-of-freedom control.

be duty modulated. The pulsewidths are decided by $d_1T_s/2$ and $d_2T_s/2$ for primary and secondary voltages, respectively, as shown in Fig. 2(b). The time shift $\delta T_s/4$ is provided for power transfer, where $T_s = 1/f_s$. It can be seen from Fig. 2(b) that the duty cycles $d_1,\ d_2 \in [0, 1]$. The phase shift ranges between $-\frac{T_s}{4}$ and $\frac{T_s}{4}$, which corresponds to $\delta \in [-1, 1]$. $\delta > 0$ results in power transfer from V_1 to V_2.

A. Problem Description

Consider a DAB converter with the following specifications:

Port 1 Voltage: V_1, switching frequency: f_s

Port 2 Voltage: $V_{2\text{min}} \leq V_2 \leq V_{2\text{max}}$

Power Rating: $P_{\text{min}} \leq P \leq P_{\text{max}}$.

The above problem represents a scenario, where one of the dc voltages (V_1) is tightly regulated despite variations of V_2. The converter load may also vary between two known limits. Converter design involves determination of the transformer turns ratio n and the value of series inductance L. After the design, the operation problem involves finding the modulation strategy (d_1, d_2, and δ) for a given P and V_2. The specifications of inductor, transformer, switches, and capacitor can then be determined based on worst-case operating conditions. The converter design should be carried out such that the maximum value of inductor rms current I_{rms} is minimized over the entire operating range (considering variations in P and V_2) of the converter. Moreover, ZVS should be ensured for the entire operating region of the converter. Fulfilling these design objectives results in improved size and efficiency of the converter. The subsequent section discusses the converter model in steady state, which is used for solving the optimization problem.

B. Converter Modeling

The voltage conversion ratio is defined as

$$m = \frac{n_1 V_2}{n_2 V_1} = \frac{nV_2}{V_1} \tag{1}$$

where n_1 and n_2 are the number of turns in the transformer windings.

For a given n and the variation of V_2 described above, m varies between $m_{\text{min}} := nV_{2\text{min}}/V_1$ and $m_{\text{max}} := nV_{2\text{max}}/V_1$. With the defined conversion ratio, the voltage levels in $v'_{cd} := nv_{cd}$ are $\pm mV_1$ and 0. Note that the voltage levels in v_{ab} are $\pm V_1$ and 0. The inductor current can be described by

$$L\frac{di_L}{dt} = v_{ab} - nv_{cd}. \tag{2}$$

Since the primary and secondary pulsewidths are proportional to T_s, the inductor current magnitude is proportional to $(\frac{V_1 T_s}{L})$ or $(\frac{V_1}{2\pi f_s L})$. Scaling the time axis with $\theta = 2\pi f_s t$, the inductor current at any time instant can be written as a product of $\frac{V_1}{2\pi f_s L}$ and a proportionality factor $i(m, d_1, d_2, \delta, \theta)$. The actual rms current I_{rms} can then be written as

$$I_{\text{rms}} = \frac{V_1}{2\pi f_s L}\sqrt{\frac{1}{2\pi}\int_0^{2\pi} i^2 d\theta} = \frac{V_1}{2\pi f_s L} i_{\text{rms}}(m, d_1, d_2, \delta). \tag{3}$$

Instantaneous power is the product of v_{ab} and the inductor current and hence will be proportional to $\frac{V_1^2}{2\pi f_s L}$ with a proportionality factor that is a function of m, d_1, d_2, and δ. The average power over a switching cycle can be written as

$$P = \frac{V_1^2}{2\pi f_s L} \times p(m, d_1, d_2, \delta). \tag{4}$$

The values of i_{rms}, p, and the ZVS constraints are determined for various m, d_1, d_2, and δ in the subsequent sections.

1) Converter Operating Zones: The range of values that d_1, d_2, and δ can assume is between 0 and 1. So, each feasible point (d_1, d_2, δ) belongs to a unit cube. This unit cube can be divided into five different operating zones, where the expressions for p and i_{rms} are different because the inductor voltage has different patterns [3]. The different constraints in terms of operating variables $[d_1, d_2, \delta]$ for each zone are depicted in Fig. 3(a)–(e). Considering the transformation $\theta = 2\pi f_s t$ to (2) described before, the dynamics in i can be described by the following equation:

$$\frac{di}{d\theta} = v_L(\theta) \tag{5}$$

where $v_L(\theta) := (v_{ab} - v'_{cd})/V_1$ is the scaled inductor voltage. For operation of the converter in zone V, the values of v_L and $i(\theta)$ at different time instants are indicated in Fig. 3(f). Considering the value of i at $\theta = 0$ as i_0, the value of i_1 can be determined from (5) as

$$i_1 = i_0 + m\theta_1. \tag{6}$$

The values i_2–i_5 can be similarly determined using (5). The inductor voltage v_L has half wave symmetry. Thus, i at the steady state will be free from dc offsets and will have half wave symmetry. This implies $i_0 = -i_5$. The values i_0–i_5 can now be

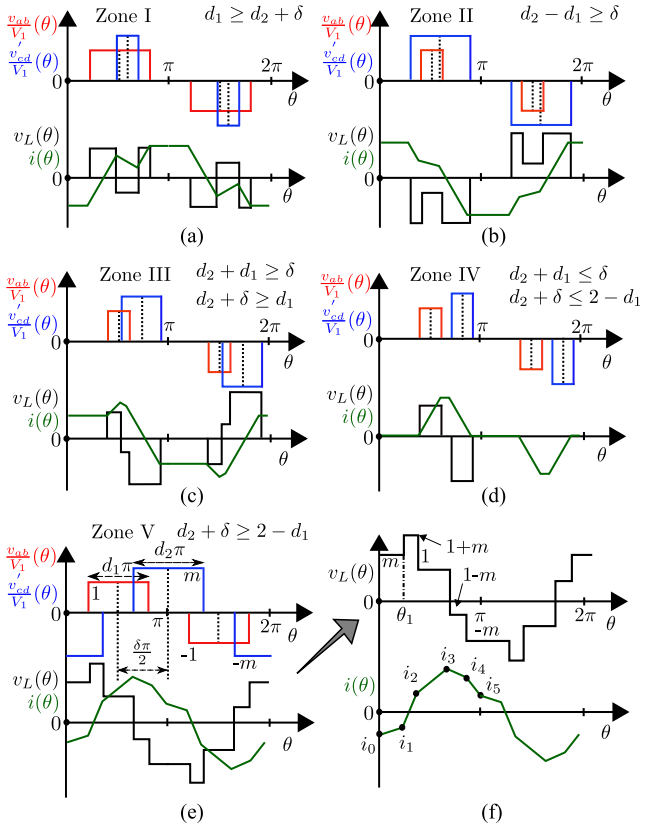

Fig. 3. (a)–(f) DAB operating zones for d_1, d_2, $\delta \in [0, 1]$.

determined as functions of m, d_1, d_2, and δ

$$\begin{aligned} i_0 &= \frac{\pi}{2}(m - d_1 - m\delta) \\ i_1 &= \frac{\pi}{2}(2m - md_1 - d_1 - m\delta) \\ i_2 &= \frac{\pi}{2}(\delta + d_2 + md_2 - 2) \\ i_3 &= \frac{\pi}{2}(\delta - d_2 + md_2) \\ i_4 &= \frac{\pi}{2}(d_1 - md_1 + m\delta) \\ i_5 &= \frac{-\pi}{2}(m - d_1 - m\delta). \end{aligned} \tag{7}$$

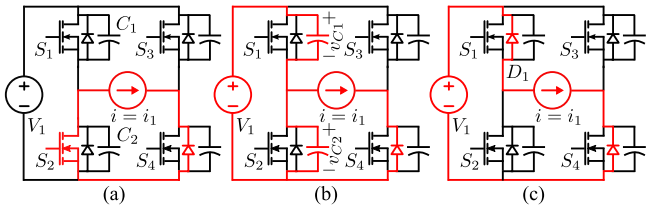

Fig. 4. (a)–(c) Capacitor-assisted soft switching.

The scaled inductor current waveform i is determined for zone V. Similar analysis can be carried out for zones I–IV.

2) Conditions for Soft Switching: Consider that the converter is operating in zone V and undergoing the switching transition at $\theta = \theta_1$, as shown in Fig. 3(f). At this instant, switch S_2 is turning OFF and switch S_1 is turned ON after dead time. This situation is depicted in Fig. 4. Assume that the current i_1 at θ_1 is less than zero. This implies that switch S_2 was conducting prior to its turn-OFF, and thus, $v_{C2} = 0$ [see Fig. 4(a)]. On removing gate pulse for S_2, the inductor current quickly shifts to the capacitors C_2 and C_1, charging and discharging them, respectively [see Fig. 4(b)]. The channel current quickly reduces before voltage v_{C2} increases, and hence, it reduces turn-OFF loss of S_2. Once the voltage v_{C1} reduces to zero, the diode D_1 starts to conduct [see Fig. 4(c)]. Turning ON the switch after this instant will lead to ZVS turn-ON of S_1. Thus, i_1 should be less than zero for soft switching, which means $(d_1 - 2m + m\delta + md_1) > 0$. Evaluation of the current polarity condition for the remaining switching transitions leads to three more inequality constraints in m, d_1, d_2, and δ. A similar analysis can be carried out for zones I–IV. The set of inequality constraints is summarized in Table I.

From Table I, it can be concluded that ZVS conditions can be simultaneously satisfied in zones I, II, and V only. All the transitions are not zero voltage switched in zones III and IV. Inequalities that cannot be satisfied simultaneously in zones III and IV are highlighted in Table I. Using the rms current expression in (3) and the current values from (7), the expression for i_{rms} is obtained in (9). Integrating the $v_{ab}i_L$ product over half line cycle, the power $p_{zV} = \frac{1}{2\pi}[(i_1 + i_2)(\theta_2 - \theta_1) + (i_2 + i_3)(\theta_3 - \theta_2) + (i_3 + i_4)(\theta_4 - \theta_3)]$. Using the current expressions from (7) and time instants from Fig. 3(f), the scaled power is obtained in (8). The values of p and i_{rms} can be similarly evaluated for zones I and II. The expressions are indicated in (8) and (9) shown at the bottom of this page.

$$p_{zI} = 0.5m\pi\delta d_2 \qquad p_{zII} = 0.5m\pi\delta d_1 \qquad p_{zV} = 0.25m\pi\left(1 - (1 - d_1)^2 - (1 - d_2)^2 - (1 - \delta)^2\right) \tag{8}$$

$$\left.\begin{aligned} i^2_{\text{rms},zI} &= \frac{\pi^2}{12}\left(-2{d_1}^3 + 3{d_1}^2 d_2 m + 3{d_1}^2 - 6d_1 d_2 m - 2{d_2}^3 m^2 + {d_2}^3 m + 3{d_2}^2 m^2 + 3d_2\delta^2 m\right) \\ i^2_{\text{rms},zII} &= \frac{\pi^2}{12}\left({d_1}^3 m - 2{d_1}^3 + 3{d_1}^2 + 3d_1{d_2}^2 m - 6d_1 d_2 m + 3d_1\delta^2 m - 2{d_2}^3 m^2 + 3{d_2}^2 m^2\right) \\ i^2_{\text{rms},zV} &= \frac{\pi^2}{12}\left(-2{d_1}^3 - 3{d_1}^2\delta m + 3{d_1}^2 m + 3{d_1}^2 + 6d_1\delta m - 6d_1 m - 2{d_2}^3 m^2 - 3{d_2}^2\delta m \right. \\ &\qquad \left. + 3{d_2}^2 m^2 + 3{d_2}^2 m + 6d_2\delta m - 6d_2 m - \delta^3 m + 3\delta^2 m - 6\delta m + 4m\right) \end{aligned}\right\} \tag{9}$$

TABLE I
ZVS CONSTRAINTS FOR DIFFERENT OPERATING ZONES

Zone I	$(d_1 - d_2 m) > 0$	$(\delta - d_2 + d_2 m) > 0$	$(d_2 + \delta - d_2 m) < 0$	
Zone II	$(d_1 - d_2 m) < 0$	$(d_1 m - d_1 + m\delta) < 0$	$(d_1 - d_1 m + m\delta) > 0$	
Zone III	$\boldsymbol{(d_1 - d_2 m) > 0}$	$(d_2 m - d_2 + \delta) > 0$	$(d_1 - d_1 m + m\delta) > 0$	$\boldsymbol{(d_1 - d_2 m) < 0}$
Zone IV	$\boldsymbol{(d_1 - d_2 m) > 0}$	$(d_1 + d_2 m) > 0$	$\boldsymbol{(d_1 - d_2 m) < 0}$	
Zone V	$(d_1 - 2m + m\delta + m d_1) > 0$	$(d_2 + \delta + m d_2 - 2) > 0$	$(\delta - d_2 + d_2 m) > 0$	$(d_1 - d_1 m + m\delta) > 0$

TABLE II
BOUNDARY POWER LEVELS [10]

	p_{c1}	p_{c2}
$m \leq 1$	$\frac{\pi m^2 (1-m)}{2}$	$\frac{(1-m^2)\pi}{2m}\left(-1 + \frac{1}{\sqrt{(1-m^2)}}\right)$
$m > 1$	$\frac{\pi(m-1)}{2m}$	$\frac{m\pi}{2}\left(1 - m^2 + m\sqrt{m^2-1}\right)$

TABLE III
OPTIMUM MODULATION PARAMETERS [10]

	$p \in [0, p_{c1})$	$p \in [p_{c1}, p_{c2})$
$m \leq 1$	$d_1 = \sqrt{\frac{2p}{(1-m)\pi}}$ $d_1 = m d_2$ $\delta = (1-m) d_2$	$\pi d_1 (1-\delta) = \pi m \left(2d_1 - d_1^2\right) - 2p$ $d_2 = 1$ $\delta = 1 - \sqrt{2d_1 - d_1^2 - \frac{4p}{m\pi}}$
$m > 1$	$d_1 = m d_2$ $d_2 = \sqrt{\frac{2p}{\pi m (m-1)}}$ $\delta = (m-1) d_2$	$d_1 = 1$ $\pi d_2 (1-\delta) = \frac{\pi}{m}\left(2d_2 - d_2^2\right) - \frac{2p}{m^2}$ $\delta = 1 - \sqrt{2d_2 - d_2^2 - \frac{4p}{m\pi}}$

C. Optimal Modulation Strategy

In general, the inductor rms current is a function of n, L, V_1, V_2, P, d_1, d_2, and δ. In the design problem, V_1 and f_s are fixed, which from now onwards will be treated as known constants. V_2 and P change over a range. Since n and V_2 (both unknown at this point) appear to impact on I_{rms} and P as a product $m = (\frac{nV_2}{V_1})$, their variation can be represented as m. The objective of design is to find n and L so that maximum rms current over a variation of V_2 and P is minimized. As a first step, we need to determine I_{rms} as a function of m, P, and L. For one such given operating point (V_2 and P) and given n and L or in other words for a given P, m, and L, it is possible to find d_1, d_2, and δ so that I_{rms} is minimized. This optimization problem, where (3) is the objective function with (4) and ZVS conditions as the constraints, is solved in [10]. The solution is known as the optimal modulation strategy. Using (3) and (4), the problem can be written as

$$\min_{\substack{0 \leq d_1, d_2, \delta \leq 1, \text{ ZVS} \\ p = P \times (2\pi f_s L)/V_1^2 = \\ p|_m(d_1, d_2, \delta)}} \quad i_{\text{rms}}|_m(d_1, d_2, \delta). \tag{10}$$

Note that $p|_m(d_1, d_2, \delta)$ implies p is a function of all four variables, but m is treated as a constant. The solution depends on both m and p. For any given m, p must be smaller than $\frac{m\pi}{4}$ for solution of (10) to exist. Solution of the problem leads to three regions of operation [10]. For operating powers p up to p_{c1} (indicated in Table II), the converter operates in zone I (zone II) for $m > 1$ ($m < 1$) with the modulation parameters listed in Table III. For $p \in [p_{c1}, p_{c2}]$, the modulation parameters are obtained by solving simultaneous equations in d_1 and δ for $m \leq 1$ and in d_2 and δ for $m > 1$. These equations are indicated in the second column of Table III. Beyond power levels of p_{c2}, the converter operates with the conventional phase shift strategy ($d_1 = 1, d_2 = 1$). The value of δ is given by $\delta = 1 - \sqrt{1 - \frac{4p}{m\pi}}$.

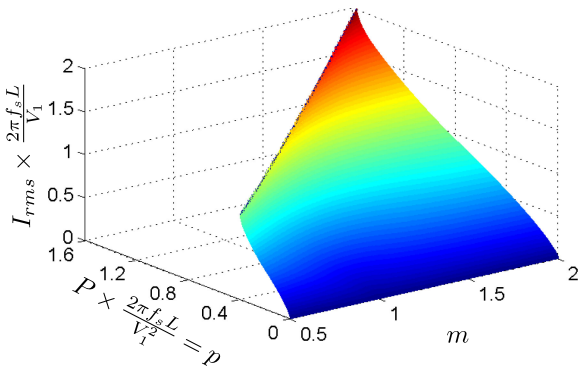

Fig. 5. Optimum value of i_{rms} for various m and p.

The optimal value of i_{rms} for various $m \in [0.5, 2]$ and $p \in [0, m\pi/4]$ is shown in Fig. 5. It can be seen that for any fixed m (which means fixed nV_2) and any arbitrary choice of L (provided $p_{\max} \leq m\pi/4$ is ensured), the value of i_{rms} (hence I_{rms}) monotonically increases as p (or P) is increased. Thus, I_{rms} is maximum when $P = P_{\max}$. It is now established that once m and L are fixed, the maximum value of rms current always occurs at $P_{\max}$.

D. Design Problem Formulation

At this point, we restate the design problem: 1) V_1 and f_s are known and fixed quantities; 2) n and V_2 appears as a product in (3) and (4), which is represented by m; and 3) m and L need to be determined so that rms inductor current I_{rms} is minimized for $P = P_{\max}$. Substituting L [using $P = P_{\max}$ in (4)] into (3), we obtain (11)

$$I_{\text{rms}} = \frac{i_{\text{rms}}(m, d_1, d_2, \delta)}{p(m, d_1, d_2, \delta)} \frac{P_{\max}}{V_1} = \left(\frac{i_{\text{rms}}}{p}\right) \times \frac{P_{\max}}{V_1}. \tag{11}$$

As $P_{\max}/V_1$ is constant and known *a priori* from specifications, minimization of I_{rms} is equivalent to minimization of the ratio $(\frac{i_{\text{rms}}}{p})$. Operation of the converter in zones I, II, and V is considered since ZVS constraints can be only satisfied in these zones. For solving the multidimensional optimization problem, m is fixed as a parameter and the optimal d_1^*, d_2^*, and δ^* are determined, which leads to minimum $(\frac{i_{\text{rms}}}{p})$ for that particular m. We obtain the following optimization problem with unknown

variables m, d_1, d_2, and δ:

$$\min_{\substack{d_1,d_2,\delta\in[0,1]\\ \text{ZVS}}} \left(\frac{i_{rms}}{p}\right)\Big|_{m>0} (d_1, d_2, \delta). \tag{12}$$

E. Solution for a Given m

Minimization of (12) is carried out by fixing m as a parameter and analytically solving the problem through Karush–Kuhn–Tucker conditions. The ZVS conditions are met only in zones I, II, and V, which form mutually exclusive subsets of the unit cube. The optimization problem is solved in zones I, II, and V separately, and the minima among these three zones is identified. For the converter operating in zone V, the objective function to be minimized is $(\frac{i_{\text{rms},zV}}{p_{zV}})$. The expressions for p_{zV} and $i_{\text{rms},zV}$ are given in (8) and (9), respectively. The inequality constraints are given in the last row of Table I. Similar process is followed for zones I and II. The global optimum value of $(\frac{i_{\text{rms}}}{p})$ is found to be in zone V for all $m > 0$. For $m \in [0, 1]$, $d_2^* = 1$ and the value of d_1^* can be obtained by solution of (13a) shown at the bottom of this page, in the range $[0, 1]$. δ^* can be obtained from (13b) shown at the bottom of this page. For $m > 1$, $d_1^* = 1$ and the value of d_2^* is obtained by determining the root of (14a) shown at the bottom of this page, in the range $[0, 1]$. δ^* can be obtained from (14b) shown at the bottom of this page. The optimum value of the ratio $(\frac{i_{\text{rms}}}{p})^* = I^*_{\text{rms}} \times \frac{V_1}{P_{\text{max}}}$ is obtained for any given m by evaluating the ratio (i_{rms}/p) at $d_1^*(m)$, $d_2^*(m)$, and $\delta^*(m)$. This value is shown in Fig. 6(a) (blue) for $m \in [0.5, 2]$. For validating the analytical solution, the optimization problem in (12) is solved numerically through *fmincon* package of MATLAB. The optimal rms current has close agreement with the analytical result [see Fig. 6(a)]. The optimum modulation parameters are shown in Fig. 6(b). The values of d_1^*, d_2^*, and δ^* for a given m can be substituted in the zone V power expression (8) to obtain the value of $p^*(m) = p(m, d_1^*, d_2^*, \delta^*) = \frac{2\pi f_s P_{\text{max}} L^*(m)}{V_1^2}$. This process is repeated for other m, and the result obtained is shown in Fig. 7 (blue curve). Some important observations can be made from the solution.

1) The global optimum of the problem occurs at $m = 1$. At this point, $d_1^* = 1$, $d_2^* = 1$, and $\delta^* = 0$. This means $p^* = 0$ (or $L^* = 0$) and $i^*_{\text{rms}} = 0$. However, their ratio converges to unity. Operation at the global optimum point is thus not possible.

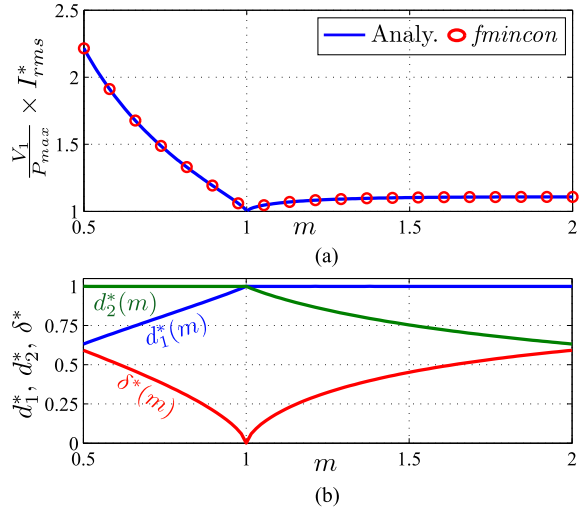

Fig. 6. (a) Variation of optimum I_{rms} with m. (b) Optimum operating point $(d_1^*,\ d_2^*,\ \delta^*)$.

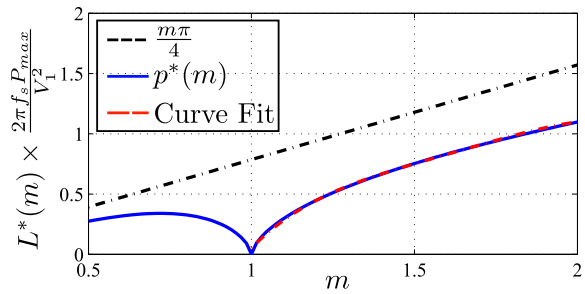

Fig. 7. Optimum L^* (or p^*) as a function of m.

2) As m is increased beyond 1, the value of $I^*_{\text{rms}} \times \frac{V_1}{P_{\text{max}}}$ slowly increases from its global optimum of 1 and then stays almost constant at 1.1.
3) For $m < 1$, the rms current increases rapidly as m reduces from unity. This value crosses 1.1 at $m = 0.95$. Thus, for achieving rms current less than or equal to 1.1 for an $m < 1$, m must be greater than 0.95.

Fig. 7 shows a plot of $p^*(m)$ and the maximum power $(\frac{m\pi}{4})$, which can be transferred for a given m. Close to $m = 1$, $p^*(m) \ll \frac{m\pi}{4}$, which implies poor controllability. For example, at $m = 0.95$, $p^*(m) = 0.175$ is just 23% of the maximum power. This value reduces to zero as $m = 1$ point is approached. So, it is not suggested to design L^* for $m < 1$.

$$\left(1+m^2\right)^2 d_1^{*6} - 6m^2\left(m^2+1\right) d_1^{*5} + 3m^2\left(4m^2+1\right) d_1^{*4} - 2m^2\left(5m^2+1\right) d_1^{*3} + 6m^4 d_1^{*2} - m^6 = 0 \tag{13a}$$

$$\delta^* = 1 - \frac{d_1^*}{m} + \sqrt{d_1^{*2} - 2d_1^* + \frac{d_1^{*2}}{m^2}} \tag{13b}$$

$$\left(1+m^2\right)^2 d_2^{*7} - \left(2m^4+10m^2+8\right) d_2^{*6} + \left(15m^2+24\right) d_2^{*5} - \left(8m^2+34\right) d_2^{*4} + \left(4m^2+26\right) d_2^{*3} - 12 d_2^{*2} - \frac{1}{m^2} d_2^* + \frac{2}{m^2} = 0 \tag{14a}$$

$$\delta^* = 1 - \frac{d_2^*}{m} + \sqrt{d_2^{*2} - 2d_2^* + m^2 d_2^{*2}} \tag{14b}$$

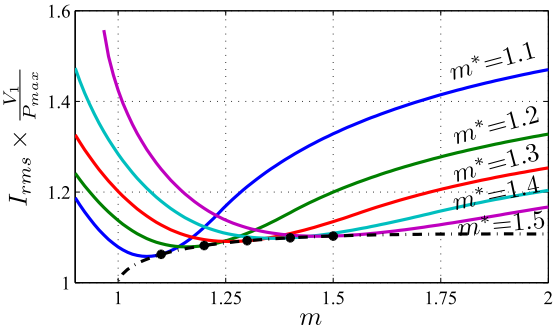

Fig. 8. Variation of rms current due to change in V_2 (here m) for a given $L = L^*(m^*)$.

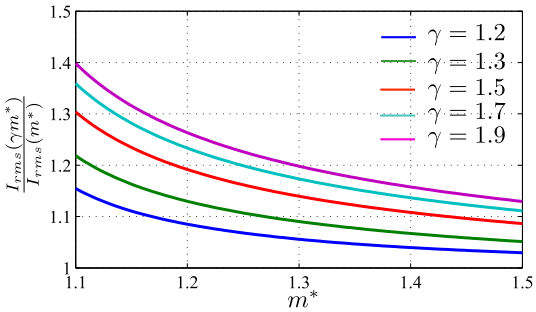

Fig. 9. Variation of $\frac{I_{\text{rms}}(\gamma m^*)}{I_{\text{rms}}(m^*)}$ with m^* for various γ.

F. Fixing m and Finalizing Design

Note that V_1 and f_s are fixed and known *a priori*. For a given choice of m^*, the optimal value of inductance L^* is obtained by evaluation of p^* at $m = m^*$. For $P = P_{\text{max}}$, $L = L^*$ and m, the optimal modulation strategy, as given in Section II-C, can be used to obtain minimum rms current with soft switching. The optimal parameters can then be substituted into (9) to obtain the rms current. Now, if we vary the chosen L^*, which is same as changing m^*, and repeat the process, we obtain a set of curves with I_{rms} as a function of m with m^* as a parameter (cf. Fig. 8). Note that for a given plot with particular m^*, the rms current will be minimum when $m = m^*$. This minimum current in Fig. 8 (black dotted points) for a given m^* is same as the optimal rms current $I^*_{\text{rms}}(m^*)$ in Fig. 6(a) when $m = m^*$.

From the plots in Fig. 8, it is possible to see that rms current rises faster with change in m for $m < m^*$ when compared with $m > m^*$. Thus, the range of m in which we should operate must always be greater than m^*, which implies $m^* = m_{\text{min}}$. For any given m^*, the rms current rises for $m > m^*$. From Fig. 8, it can be observed that the rate of this current increase reduces with increasing m^*. This implies that a higher value of m^* should be chosen during design. With given converter specifications, the value of $\gamma := \frac{m_{\text{max}}}{m_{\text{min}}} = \frac{V_{2\text{max}}}{V_{2\text{min}}}$ is known *a priori*. The ratio of rms currents at $m_{\text{max}} = \gamma m^*$ and m_{min}, i.e., $\frac{I_{\text{rms}}(m_{\text{max}}=\gamma m^*)}{I_{\text{rms}}(m^*=m_{\text{min}})}$, for variation of m^* is indicated in Fig. 9 (for different γ). For a given value of γ, and a permissible limit on the variation of rms current, this curve can be used to determine m^*. For example with $\gamma = 1.3$, if we want the variation of rms current with respect to its minimum value to be less than 10%, then minimum $m^* = 1.3$. A higher value of m^* (> 1.3) is not desirable since it leads to increase of the value of the required L^* (cf. Fig. 7). Once $m_{\text{min}} = m^*$ is fixed, the turns ratio is evaluated, $n = m^* V_1 / V_{2\text{min}}$. From Section II-E, $L = L^*(m^*) = p^*(m^*) \times \frac{V_1^2}{2\pi f_s P_{\text{max}}}$. For determining L^*, $p^*(m)$ should be known, which is given in Fig. 7. A polynomial function is fitted on Fig. 7 to determine $p^*(m)$ once m is fixed

$$p^*(m) = -1.9m^4 + 12.6m^3 - 30.9m^2 + 34.3m - 14.07. \tag{15}$$

For operation of the converter at points different than $(P_{\text{max}}, V_{2\text{min}})$, the modulation strategy described in Section II-C is used [10]. The design steps are indicated as a flowchart in Fig. 10. For a designed n and L, the per unit power varies between p_{min} and p_{max} and m varies between m_{min} and m_{max}. Thus, any operating point lies in a rectangle on the m–p plane bounded by the points A, B, C, and D, as shown in Fig. 11. For $P = P_{\text{max}}$ and $\gamma = 1.3$ (say), the design strategy in Fig. 10 gives $m^* = 1.3$. Thus, $p_{\text{max}} = p^*(m = 1.3) = 0.56$, $V_{2\text{min}}$ corresponds to $m_{\text{min}} = 1.3$. Point A in Fig. 11 has coordinates (1.3,0.56), $m_{\text{max}} = 1.3\frac{V_{2\text{max}}}{V_{2\text{min}}}$, and $p_{\text{min}} = 0.56\frac{P_{\text{min}}}{P_{\text{max}}}$.

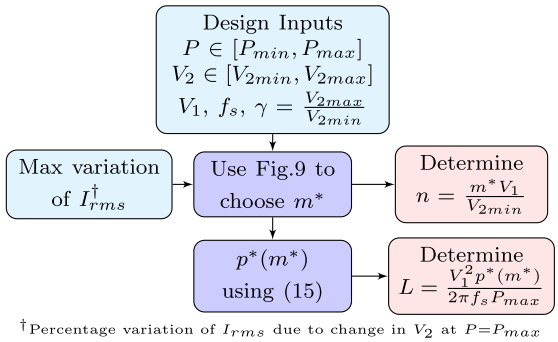

Fig. 10. Steps involved in converter design.

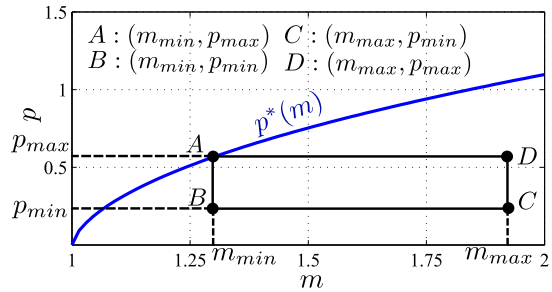

Fig. 11. Operating region of converter on the m–p plane.

G. Component Ratings

For a converter operating in the region shown in Fig. 11, the maximum values of peak and rms currents need to be identified for switch selection. The rms current is maximum at operating point D (m_{max}, p_{max}). The peak current is also maximum at D. The values of these currents can be determined using the design strategy in Section II-F. The values of input and output ripple rms currents can then be determined, which decides the capacitor ratings (for a given primary and secondary voltage

TABLE IV
DEVICE, CAPACITOR, AND MAGNETICS RATING

Switch	**RMS**		**Peak**
Pri.	$0.84P_{max}/V_1$		$2.13P_{max}/V_1$
Sec.	$0.84nP_{max}/V_1$		$2.13nP_{max}/V_1$
Capacitor	**Rip. RMS**		**Capacitance**
Pri.	$0.645P_{max}/V_1$		$0.1027P_{max}/(f_sV_1\Delta V_1)$
Sec.	$0.702nP_{max}/V_1$		$0.112nP_{max}/(f_sV_1\Delta V_2)$
Transformer	$\boldsymbol{A_cA_w}$	$\boldsymbol{n}$	$\boldsymbol{I_{rms}}$
	$\frac{0.641P_{max}}{Jf_sB_mk_w}$	$\frac{m^*V_1}{V_{2min}}$	$1.19\frac{P_{max}}{V_1}$
Inductor	$\boldsymbol{A_cA_w}$	$\boldsymbol{I_p}$	$\boldsymbol{I_{rms}}$
	$\frac{LI_pI_{rms}}{JB_mk_w}$	$2.13\frac{P_{max}}{V_1}$	$1.19\frac{P_{max}}{V_1}$

TABLE V
HARDWARE SPECIFICATIONS

V_1	V_{2min}	V_{2max}	P_{min}	P_{max}	f_s
400 V	325 V	425 V	1 kW	2.6 kW	75 kHz

ripple ΔV_1 and ΔV_2, respectively). These values are indicated in Table IV. For designing the transformer, the area product needs to be determined. The core area is dependent on the volt-seconds applied to the magnetizing inductance, which in this case is $A_c = \frac{mV_1d_2}{4n_snB_mf_s}$, where B_m is the peak flux density in core. The value of A_c is maximum when m and d_2 are maximum. The worst-case value of rms current (which happens at point D) decides the window area since $A_w = \frac{2n_snI_{\text{rms}}}{k_wJ}$, where k_w and J are window factor and the current density, respectively. The required area product is indicated in Table IV.

An external inductance may be required to be added in series with the transformer for obtaining the desired optimal L^*. In such a scenario, the required area product is given by $A_cA_w = \frac{LI_{pk}I_{\text{rms}}}{JB_mk_w}$. The rms and peak values are shown in Table IV.

III. EXPERIMENTAL RESULTS

To validate the converter design and operation methodology, a dc–dc converter was designed with the specifications provided in Table V using the method outlined in Section II-F. The value of m^* is chosen to be 1.3, which gives $p^* = 0.56$, resulting in $n = 1.6$ and $L = 73.13\ \mu$H. With these fixed values of n, L, and the modulation strategy described in Section II-C, the maximum transformer primary rms and peak currents (at P_{max} and $V_{2\text{max}}$) are 7.8 and 14.0 A, respectively. The secondary-side rms and peak currents are 12.5 and 22.4 A, respectively. SiC MOSFETs (28-A current rating) are used for primary- and secondary-side switches. Isolated gate driver (ADuM4135) is used for generation of gating pulses. The primary and secondary capacitor ripple currents are calculated to be 4.29 and 7.38 A, respectively. Film capacitors of 2.5 μF are used. The transformer area product is calculated to be 9.26 cm^4. A planar transformer is ordered from Payton with turns ratio of 24:15 and area product of 17.5 cm^4. The leakage inductance of the transformer is measured to be 20 μH at 75 kHz. Accordingly, an external inductor of 53 μH (area product: 2.44 cm^4) is designed using ferrite core (Part No: 0R45530EC). The experimental setup is shown in Fig. 12.

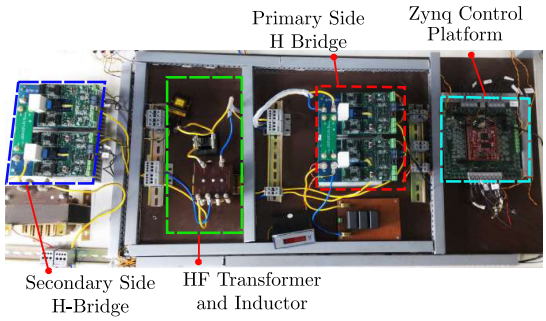

Fig. 12. Experimental setup.

TABLE VI
COMPARISON AT FOUR OPERATING POINTS OF THE CONVERTER

	P	V_2	(d_1,d_2,δ)	I_{rms}(T)	I_{rms}(S)	I_{rms}(E)	Zone
A	2.6	325	(1,0.82,0.35)	7.18	7.23	7.14	V
B	1.0	325	(0.77,0.59,0.18)	3.28	3.23	3.23	I
C	1.0	425	(0.58,0.34,0.24)	3.79	3.74	3.69	I
D	2.6	425	(0.93,0.55,0.38)	7.78	7.65	7.42	I

The values of $d_1^* = 1$, $d_2^* = 0.82$, and $\delta^* = 0.35$ are obtained using the modulation strategy described in Section II-C. Fig. 13(a) shows the operation of the converter at point A ($V_{2\text{min}} = 325$ V and $P_{\text{max}} = 2.6$ kW). The converter operates in zone V (since $d_1^* + d_2^* + \delta^* = 2.17 > 2$) for the set of modulation parameters, which can be seen from Fig. 13(a). The experimental value of inductor rms current is 7.14 A, which is close to the theoretically predicted rms value, as indicated in Table VI. The operating waveforms for four boundary points of the operating area with the modulation strategy in Section II-C are given in Fig. 13(b)–(d), respectively. The converter operation is simulated in Simulink for the operating conditions in Fig. 13. The modulation parameters along with the theoretical (T), simulation (S), and experimental (E) rms currents for the four operating conditions are indicated in Table VI. A close agreement between theoretical, simulation, and experimental values can be observed. It can be seen that for all these operating conditions, the power is less than $\frac{nV_1V_2}{8f_sL}$, which is the maximum deliverable power. Thus, the converter is able to operate in the entire operating region of Fig. 11.

A. Soft Switching—Experimental Validation

Consider the converter operating in zone V at $V_2 = V_{2\text{min}}$ and $P = P_{\text{max}}$ (point A in Fig. 11). Current i_1 should be less than zero, and the currents i_2, i_3, and i_4 should be greater than zero to ensure switch to diode transition (ZVS). For operation of the converter at point A, the currents i_1–i_4 are indicated in Fig. 13(a). It can be seen that all the current polarities are maintained as desired, which ensures soft switching. The switching transition described in Section II-B2 (when $i_L = i_1$) is shown in Fig. 14 to demonstrate soft turn-OFF of S_2 and soft turn-ON of S_1. Switch S_2 is conducting prior to its turn-OFF (at t_0) since $i_L = i_1 < 0$ (cf. Fig. 13(a)). After $t = t_0$, the gate voltage $v_{gs,S2}$ starts to reduce. The gate voltage reduces below threshold implying that channel current is zero before $v_{ds,S2}$ starts to increase at $t = t_1$.

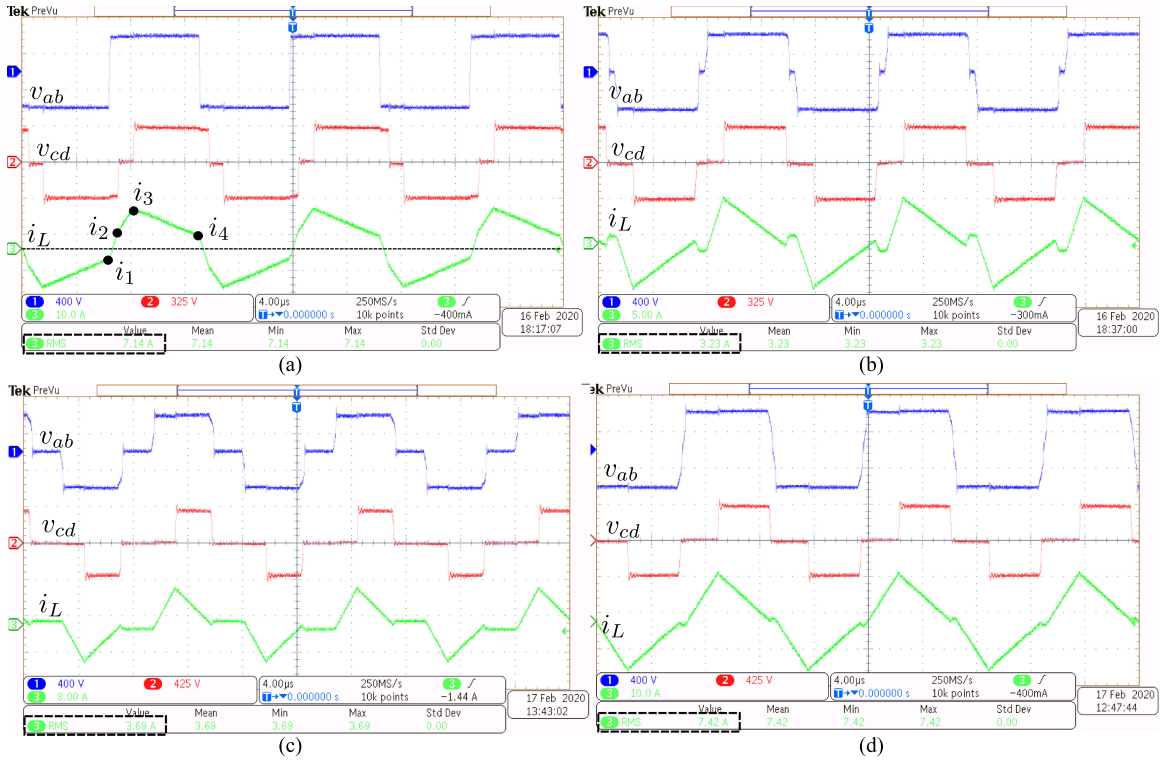

Fig. 13. Experimental results showing v_{ab}, v_{cd}, i_L, and its rms value for (a) $P_{\text{max}} = 2.6$ kW and $V_{2\text{min}} = 325$ V, (b) $P_{\text{min}} = 1$ kW and $V_{2\text{min}} = 325$ V, (c) $P_{\text{min}} = 1$ kW and $V_{2\text{max}} = 425$ V, and (d) $P_{\text{max}} = 2.6$ kW and $V_{2\text{max}} = 425$ V.

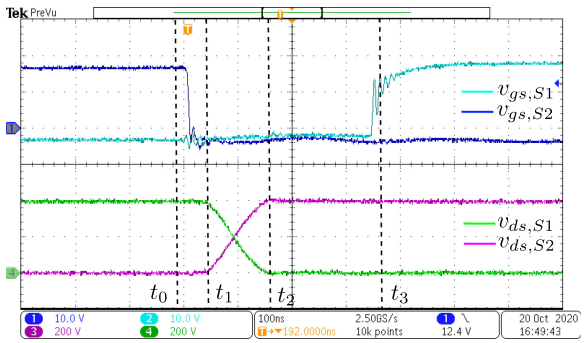

Fig. 14. Experimental evidence of soft turn-OFF of S_2 and soft turn-ON of S_1 when $i_L = i_1$ in Fig. 13(a).

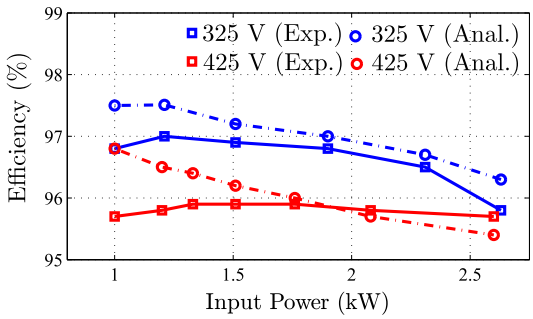

Fig. 15. Converter efficiency.

This results in ZVS turn-OFF of S_2. At $t = t_2$, $v_{ds,S1}$ reduces to zero and diode D_1 starts conducting. The turn-ON of S_1 at $t = t_3$ happens at zero voltage indicating ZVS. Similar behavior was observed for the remaining switching transitions of the converter.

B. Efficiency and Loss Breakup

The analytical and experimental converter efficiency is shown in Fig. 15 for operation at minimum (along AB) and maximum (along CD) V_2 (see Fig. 11). A close agreement between the results can be observed. The peak efficiency of the converter is 97% for operation at $V_2 = 325$ V. The efficiency of the converter is slightly reduced for operation of the converter at maximum V_2 due to increased conduction losses.

Theoretical loss estimation is carried out for operation at the four boundary points in the operating area of the converter. A comparison of experimental loss and theoretical calculation is given in Fig. 16(a). Variation of ON-state resistance with current and dependence of core loss on temperature leads to slight mismatch between the values. A theoretical loss breakup for $P_{\text{max}} = 2.6$ kW and $V_{2\text{min}} = 325$ V (point A) is shown in Fig. 16(b). The primary and secondary switch rms currents are $I_{\text{rms}}/\sqrt{2} = 5.08$ A and $nI_{\text{rms}}/\sqrt{2} = 8.13$ A. With $r_{ds,\text{on}} = 0.125\ \Omega$ for primary and secondary MOSFETs, the primary and secondary conduction losses are 12.9 and 33.04 W, respectively. The transformer and inductor resistance is found to be $r_c = 0.5\ \Omega$ at 75 kHz. For rms current of 7.18 A (cf. Table VI), the conduction loss is 25.8 W. The core loss in the transformer is evaluated through improved Steinmetz equation. The core parameters $\alpha = 1.098$, $\beta = 2.196$, and $k_c = 0.025$ are obtained from the loss density

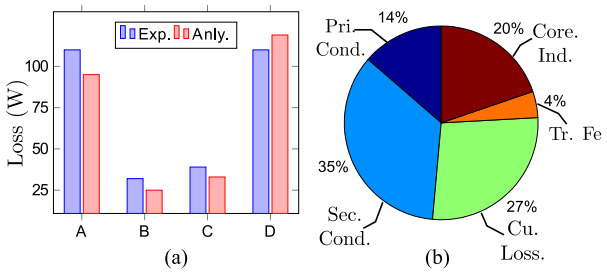

Fig. 16. (a) Comparison of analytical and experimental losses for the operating points A, B, C, and D in Fig. 11. (b) Theoretical loss breakup for $P_{\text{max}} = 2.6$ kW and $V_{2\text{min}} = 325$ V.

curve given in the datasheet. The time averaged loss density is evaluated as $\langle p_v \rangle = k_i |\Delta B|^{(\beta-\alpha)} |\frac{dB(t)}{dt}|^{\alpha}$, where ΔB is the peak-to-peak flux density. The empirical relation for k_i can be found in [25]. Evaluating ΔB and $|\frac{dB(t)}{dt}|$ from transformer applied volt-seconds, $\langle p_v \rangle = 50.43$ mW/cm^3. Multiplying by the core volume, the core loss in the transformer is 4.13 W. This process is repeated for the inductor core ($\alpha = 0.845$, $\beta = 2.099$, and $k_c = 0.467$), and the core loss obtained is 18.66 W. The total loss at this operating condition is 94.8 W. It can be seen that major losses are the conduction losses in the bridges and copper loses in the transformer.

IV. Conclusion

In this article, a design procedure for a DAB based dc–dc converter with a given set of specifications (power range, uncontrolled port voltage range, controlled port voltage, and switching frequency) was presented. The design aimed at minimization of worst-case inductor rms current in the operating range of the converter. Modeling of the converter was carried out in the time domain, and the optimal TPS strategy was considered for minimum rms current and soft switching in the entire operating range. It was identified that the maximum rms current with optimal TPS strategy always happens at maximum power. For the converter operating at maximum power and a given value of uncontrolled port voltage, an optimization problem was formulated for minimization of rms current with soft switching. Analytical solution of the optimization problem provided the optimal values of the design variables, i.e., transformer turns ratio and the value of the series inductance. As the voltage of the uncontrolled port deviates from the value chosen for optimal design, the rms current deviates from its optimal value. Further analysis showed if the optimal design is done at the minimum value of the uncontrolled port voltage, the rms inductor current stays close to its optimal value, despite variation in the voltage. Closed-form expressions for optimal design variables obtained through curve-fitting were provided. A simple step-by-step procedure for obtaining the design parameter values from converter specifications was provided. Details of the selection of power devices, filter capacitors, and design of transformer and inductor were also given. A 2.6-kW hardware prototype was designed based on the outlined procedure. Experimental results confirmed the effectiveness of the design.

TABLE VII
Computation Comparison With [24]

Proposed strategy	Method in [24] with N discrete points
4 A, 16 M, 2 D, 0 S	$7N^3$ A, $22N^3$ M, $4N^3$ D, $2N^3$ S

A: addition, M: multiplication, D: division, S: square root.

TABLE VIII
Worst-Case Performance Comparison

	Factor	This paper	[23]
$I_{rms,in}$, I_{rms} (Worst)	$\frac{P_{max}}{V_1}$	1.19	1.87
I_{pk} (Worst)	$\frac{P_{max}}{V_1}$	2.13	2.54
$I_{rms,out}$ (Worst)	$\frac{P_{max}}{V_{2min}}$	1.64	1.84

TABLE IX
Comparison of Component Sizes

	Factor	This paper	[23]
Trans. A_cA_w	$\frac{P_{max}}{Jf_sB_mk_w}$	0.641	0.935
Ind. A_cA_w	$\frac{P_{max}}{Jf_sB_mk_w}$	0.229	0.459
Cap. Rip. RMS (Pri.)	$\frac{P_{max}}{V_1}$	0.645	1.581
Cap. Rip. RMS (Sec.)	$\frac{P_{max}}{V_{2min}}$	0.922	1.023

Appendix A
Comparison With Literature

A comparison of computational effort of the proposed method with [24] is provided in Table VII. The proposed method is simple to implement, whereas the computational complexity is high in [24] for higher number of discrete points N in the range of optimization variables. A detailed performance comparison of the presented method with [23] is given. Same converter specifications (cf. Table V) are considered for both the methods. Following the design strategy in [23], $n = 0.94$ and $L = 78.4$ μH. The SPS modulation strategy is used. The worst-case inductor rms current I_{rms} (same as the input rms current $I_{\text{rms,in}}$) in [23] occurs for $V_2 = V_{2\text{min}}$, and its value is indicated in Table VIII. With the proposed design method, an improvement in the worst-case rms current can be observed. A considerable reduction in the worst-case peak current and the output rms current can be similarly observed. With the proposed design and modulation strategy in [10], the converter achieves soft switching in the entire operating range. With the strategy in [23], the converter is partially soft switched for low power and voltage.

For comparing the power density and component sizes, the area products of transformer, inductor, and the capacitor ripple rms requirement are indicated in Table IX for both the methods. Area product and ripple rms currents are calculated for the method in [23] using the strategy in Section II-G. The proposed method results in reduction of magnetic component and capacitor size. For comparing the efficiency, a loss comparison is provided in Table X for operation of the converter at $P = 2.6$ kW and $V_2 = 325$ V. It can be seen that the proposed method results in reduction of conduction losses in both the bridges and copper losses in the transformer and the inductor. Thus, the proposed

TABLE X
LOSS COMPARISON: $P = 2.6$ kW AND $V_2 = 325$ V

	Factor	This paper	[23]
Cond.-Pri.	$\left(\frac{P}{V_1}\right)^2 r_{on,p}$	2.387	6.996
Cond. - Sec.	$\left(\frac{P}{V_{2min}}\right)^2 r_{on,s}$	4.034	4.092
Copper Loss	$\left(\frac{P}{V_1}\right)^2 r_c$	1.194	3.498

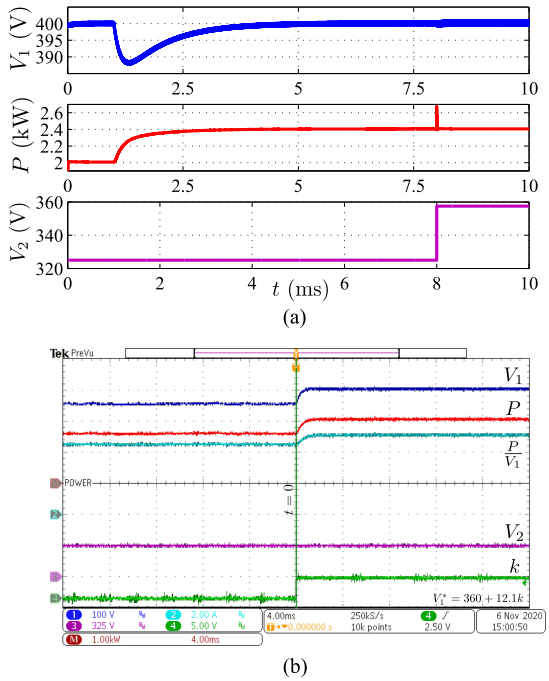

Fig. 17. (a) Simulation showing closed-loop performance. (b) Experimental result showing response to change in V_1^*.

method results in improvement of circuit performance in terms of efficiency, component size, and worst-case current stresses.

APPENDIX B
CLOSED-LOOP OPERATION

The modulation technique in [10] is used for converter operation once design parameters are fixed according to Section II-F. A closed-loop voltage controller having structure as [10] is implemented in simulation and experiment for regulating the controlled port voltage to given value V_1^* during disturbances. The proportional–integral controller parameters are obtained as $k_p = 20$ and $k_i = 25 \times 10^3$ following design process in [10]. Fig. 17(a) shows the dynamic performance of the converter for step changes in load and V_2. The converter was initially operating with $P = 2$ kW, $V_1 = 400$ V, and $V_2 = 325$ V. At $t = 1$ ms, the load of the converter is increased by 10%, after which the closed-loop action brings the delivered power to 2.4 kW and V_1 to 400 V. At $t = 8$ ms, V_2 is increased by 10%. The power settles to the same value after an initial short transient. For experimental verification, the response of the converter is shown in Fig. 17(b) for a step change in V_1^* (CH4) from 360 to 400 V. Following the step change at $t = 0$, a first-order dynamics can be observed

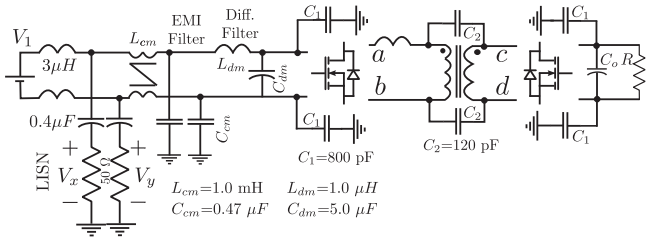

Fig. 18. Circuit to study electromagnetic compatibility response (C_1 and C_2 from [26]).

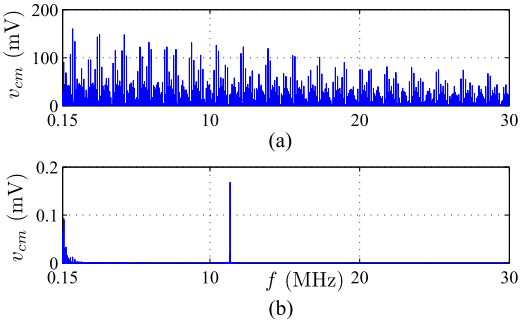

Fig. 19. Simulated electromagnetic compatibility response without and with a common-mode filter.

in V_1, after which it settles to 400 V (CH1). Since the load resistance is constant, the current accordingly increases from 4.5 to 5 A (CH2). The measured power also increases to 2 kW. V_2 is kept constant during this event (CH3).

APPENDIX C
DISCUSSION ON ELECTROMAGNETIC COMPATIBILITY

The DAB circuit along with a line impedance stabilization network shown in Fig. 18 is simulated to analyze the common-mode noise. According to Federal Communications Commission regulation, the common-mode voltage ($v_{\rm cm} = 0.5(v_x + v_y)$) developed across 50-Ω resistance should be less than 1 mV in 150 kHz–30 MHz [27]. This regulation is violated without the electromagnetic interference (EMI) filter [cf. Fig. 19(a)]. An EMI filter is designed to attenuate the peak (150 mV) by 150 times (43.5 dB) . Accordingly, the LC filter (formed by $L_{\rm cm}$ and $C_{\rm cm}$) should have a cutoff frequency of $150 \times 10^{-\frac{43.5}{40}} = 12.24$ kHz. Fig. 19(b) shows the common-mode voltage spectrum with the EMI filter. It can be seen that the voltage is below 1 mV conforming to the regulation. Similar design can be carried out for load side.

REFERENCES

[1] R. De Doncker, D. Divan, and M. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, Jan./Feb. 1991.
[2] M. Kheraluwala, R. Gascoigne, D. Divan, and E. Baumann, "Performance characterization of a high-power dual active bridge dc-to-dc converter," *IEEE Trans. Ind. Appl.*, vol. 28, no. 6, pp. 1294–1301, Nov./Dec. 1992.
[3] A. K. Jain and R. Ayyanar, "PWM control of dual active bridge: Comprehensive analysis and experimental verification," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1215–1227, Apr. 2011.

[4] H. Bai and C. Mi, "Eliminate reactive power and increase system efficiency of isolated bidirectional dual-active-bridge DC/DC converters using novel dual-phase-shift control," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2905–2914, Nov. 2008.
[5] S. Wang, Z. Zheng, C. Li, K. Wang, and Y. Li, "Time domain analysis of reactive components and optimal modulation for isolated dual active bridge DC/DC converters," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7143–7146, Aug. 2019.
[6] B. Zhao, Q. Song, W. Liu, G. Liu, and Y. Zhao, "Universal high-frequency-link characterization and practical fundamental-optimal strategy for dual-active-bridge DC-DC converter under PWM plus phase-shift control," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6488–6494, Dec. 2015.
[7] H. Shi, H. Wen, J. Chen, Y. Hu, L. Jiang, and G. Chen, "Minimum-reactive-power scheme of dual active bridge DC-DC converter with 3-level modulated phase-shift control," *IEEE Trans. Ind. Appl.*, vol. 53, no. 6, pp. 5573–5586, Nov./Dec. 2017.
[8] F. Krismer and J. Kolar, "Closed form solution for minimum conduction loss modulation of DAB converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 174–188, Jan. 2012.
[9] S. Chakraborty and S. Chattopadhyay, "Fully ZVS, minimum RMS current operation of the dual-active half-bridge converter using closed-loop three-degree-of-freedom control," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10188–10199, Dec. 2018.
[10] A. Tong, L. Hang, G. Li, X. Jiang, and S. Gao, "Modeling and analysis of dual-active-bridge isolated bidirectional DC/DC converter to minimize RMS current with whole operating range," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5302–5316, Jun. 2018.
[11] B. Zhao, Q. Song, W. Liu, and W. Sun, "Current stress optimized switching strategy of isolated bidirectional DC-DC converter with dual phase shift control," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4458–4467, Oct. 2013.
[12] N. Hou, W. Song, and M. Wu, "Minimum current stress scheme of dual active bridge DC-DC converter with unified phase shift control," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8552–8561, Dec. 2016.
[13] J. Huang, Y. Wang, Z. Li, and W. Lei, "Unified triple phase shift control to minimize current stress and achieve full soft switching of isolated bidirectional DC/DC converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4169–4179, Jul. 2016.
[14] Q. Gu, L. Yuan, J. Nie, J. Sun, and Z. Zhao, "Current stress minimization of dual active bridge DC-DC converter within the whole operating range," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 129–142, Mar. 2019.
[15] S. Shao, M. Jiang, W. Ye, Y. Li, J. Zhang, and K. Sheng, "Optimal phase shift control to minimize reactive power for a dual active bridge DC-DC converter," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 10193–10205, Oct. 2019.
[16] G. Oggier, G. O. Garcia, and A. R. Oliva, "Modulation strategy to operate the dual active bridge DC-DC converter under soft switching in the whole operating range," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1228–1236, Apr. 2011.
[17] G. G. Oggier, G. O. Garcia, and A. R. Oliva, "Switching control strategy to minimize dual active bridge converter losses," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1826–1838, Jul. 2009.
[18] B. Zhao, Q. Song, and W. Liu, "Efficiency characterization and optimization of isolated bidirectional DC/DC converter based on dual phase shift control for dc distribution application," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1711–1727, Apr. 2013.
[19] F. Krismer and J. W. Kolar, "Efficiency optimized high current dual active bridge converter for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2745–2760, Jul. 2012.
[20] U. Kundu, B. Pant, S. Sikder, A. Kumar, and P. Sensarma, "Frequency domain analysis and optimal design of isolated bidirectional series resonant converter," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 356–366, Jan./Feb. 2018.
[21] V. J. Thottuvelil, T. G. Wilson, and H. A. Owen, "Analysis and design of a push-pull current-fed converter," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 1981, pp. 192–203.
[22] J. Biela, U. Badstuebner, and J. W. Kolar, "Design of a 5kW, 1U, 10kW/dm^3 resonant DC-DC converter for telecom applications," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1701–1710, Jul. 2009.
[23] C. Gammeter, F. Krismer, and J. W. Kolar, "Comprehensive conceptualization, design, and experimental verification of a weight-optimized all-SiC 2 kV/700 V DAB for an airborne wind turbine," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 638–656, Jun. 2016.
[24] V. M. Iyer, S. Gulur, and S. Bhattacharya, "Optimal design methodology for dual active bridge converter under wide voltage variation," in *Proc. IEEE Transport. Electrific. Conf. Expo.*, Jun. 2017, pp. 413–420.
[25] W. G. Hurley and W. H. Wölfle, *Transformers and Inductors for Power Electronics: Theory, Design and Applications*. New York, NY, USA: Wiley, 2013.
[26] D. Bellan, "Symmetrical-component approach for circuit modeling of EMI emissions in three-phase inverters," in *Proc. IEEE PES Asia-Pacific Power Energy Eng. Conf.*, 2019, pp. 1–5.
[27] C. R. Paul, *Introduction to Electromagnetic Compatibility*, vol. 184. New York, NY, USA: Wiley, 2006.

Dibakar Das (Student Member, IEEE) received the B.Tech. degree from the National Institute of Technology, Durgapur, India, in 2014, and the M.S. degree, in 2017 from the Indian Institute of Science, Bangalore, India, where he is currently working toward the Ph.D. degree, all in electrical engineering.

His research interests include dual-active-bridge converters.

Kaushik Basu (Senior Member, IEEE) received the B.E. degree from the Bengal Engineering and Science University, Shibpore, India, in 2003, the M.S. degree from the Indian Institute of Science, Bangalore, India, in 2005, and the Ph.D. degree from the University of Minnesota, Minneapolis, MN, USA, in 2012, all in electrical engineering.

He was a Design Engineer with Cold Watt India in 2006 and an Electronics and Control Engineer with Dynapower Corporation, Union City, CA, USA, from 2013 to 2015. He is currently an Associate Professor with the Department of Electrical Engineering, Indian Institute of Science. He has authored or coauthored several technical papers published in peer-reviewed journals and conferences. His research interests include various aspects of the general area of power electronics.

Dr. Basu is the Founding Chair of both IEEE Power Electronics Society's and IEEE Industrial Electronics Society's Bangalore Chapter.