**ADC (ADS8320)  
  
The ADS8320 is a 16-bit successive approximation register (SAR) analog-to-digital converter (ADC) with a sample rate of up to 100 kHz. Here are the key points regarding bit configuration and timing constraints:**

**Conversion Configuration:**

**The ADS8320 uses a serial interface to communicate with an external microcontroller or processor.**

**The conversion process starts by asserting the CS/SHDN (Chip Select/Shutdown) signal low.**

**The ADC requires a clock signal (DCLOCK) to perform the conversion. The falling edge of DCLOCK initiates each conversion step.**

**The input voltage is sampled on the rising edge of DCLOCK.**

**Timing Constraints:**

**The ADS8320 requires a minimum conversion time (tCONV) to complete the conversion process.**

**The timing diagram provided in the documentation shows the various timing parameters and their relationship to clock cycles and conversion steps.**

**The minimum tCONV is 22 clock cycles, but it's recommended to use a few extra clock cycles for stability and settling time.**

**Output Data Format:**

**The output of the conversion is a 16-bit binary number.**

**The Most Significant Bit (MSB) is transmitted first followed by the remaining 15 bits.**