*Project: RMC75E FPGA TEST BENCH*

*Module: module.vhd*

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# High Level

The **CPULED** module is responsible for driving CPU status LEDs on the RMC75E Rev 3.0 board. It takes input signals, processes them, and generates output signals to control the LEDs. The module receives a 32-bit data input (**intDATA**) and a control signal (**CPULEDWrite**) to update the status of the CPU status LEDs. It also receives a reset signal (**RESET**) and a clock signal (**H1\_CLKWR**) for synchronization. The module includes a 2-bit signal (**CPUStatusLED**) that represents the state of the two CPU status LEDs.

# Low level

The **CPULED** module is a simple implementation for driving CPU status LEDs on the RMC75E Rev 3.0 board. It takes input signals, processes them, and generates output signals to control the LEDs. The module receives a 32-bit data input (**intDATA**) and a control signal (**CPULEDWrite**) to update the status of the CPU status LEDs. It also receives a reset signal (**RESET**) and a clock signal (**H1\_CLKWR**) for synchronization. The module includes a 2-bit signal (**CPUStatusLED**) that represents the state of the two CPU status LEDs.

The **CPULED** module is implemented in the **CPULED\_arch** architecture. It consists of signal declarations and a process block that updates the **CPUStatusLED** signal based on the input conditions.

Signal Declarations:

* **CPUStatusLED**: A 2-bit signal representing the state of the CPU LEDs.

Output Signals:

* **cpuLedDataOut**: The output signal concatenates **CPUStatusLED** with other fixed values to control the CPU status LEDs.

Process Block: The process block inside the architecture updates the **CPUStatusLED** signal based on the input conditions. When the **RESET** signal is active, the **CPUStatusLED** is set to "00" to clear the status of the LEDs. When the **CPULEDWrite** signal is active and there is a rising edge on the **H1\_CLKWR** signal, the **CPUStatusLED** is updated with the two least significant bits of the **intDATA** input. This action effectively sets the CPU status LEDs based on the incoming data.

LED Control Logic: The **CPUStatLEDDrive** signal controls the behavior of the CPU status LEDs. When the **CPUStatusLED** signal is "00" (undefined state), the output is set to high-impedance (**ZZ**). This behavior is intentional to allow external circuitry to force the LEDs to turn red when the FPGA is not driving them. For all other states of **CPUStatusLED**, the **CPUStatLEDDrive** signal inverts the **CPUStatusLED**, determining the state of the LEDs.

## Simulation

To verify the functionality of the **CPULED** module, simulation tests can be performed. In the simulation, appropriate test vectors for the input signals (**RESET**, **H1\_CLKWR**, **intDATA**, and **CPULEDWrite**) are provided. Observing the behavior of the **CPUStatLEDDrive** and **cpuLedDataOut** signals over time will show how the CPU status LEDs change according to the inputs provided and how the LEDs are driven based on the internal logic of the module.