*Project: RMC75E TEST BENCH*

*Module:* WatchDogTimer*.vhd*

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# High Level

The "WDT" entity represents a WatchDogTimer unit responsible for counting down from a user-defined value. When the counter reaches 0x1, the WDT expiration value is set. The module has various inputs and outputs used to control its functionality.

# Low level

**Inputs:**

* RESET: Asynchronous reset input.
* SysRESET: System reset input.
* H1\_CLKWR: Clock input for synchronization.
* SysClk: System clock input.
* intDATA: Input data from the CPU.
* FPGAAccess: Flag indicating if the CPU is reading or writing to the FPGA.
* WDTConfigWrite: Input to write configuration data to the WDT.
* FPGAProgrammedWrite: Input used to verify if the FPGA is programmed.
* SlowEnable: Enable signal to operate the WDT in slow mode.
* HALT\_DRIVE\_L: Input from Drive Enable hardware watchdog timer.
* WD\_TICKLE: Input from CPU to tickle the watchdog timer.

**Outputs:**

* wdtDataOut: Output data from the WDT.
* FPGAProgDOut: Output data for verifying FPGA existence and programming.
* WD\_RST\_L: Output to trigger module reset.
* WDT\_RST\_L: Output indicating the WDT reset status.

**Internal Signals:**

* Various internal signals, such as WDTCounter, WDTDelay, FirstKey, AccessKey, and others, are used for internal control and synchronization.

**Functionality:**

1. The WDT unit counts down from a user-defined value specified in the WDTDelay signal.
2. The WDTExpiration flag is set when the counter reaches 0x1.
3. The WDTConfigWrite input allows the CPU to write configuration data to the WDT, such as WDTDelay, FPGAResetStatus, DriveHaltStatus, and FPGA\_RstReq.
4. The FirstKey and AccessKey signals are used to enable access to specific configuration settings in the WDT based on specific writes from the CPU.
5. The WDTKick and LoadWDTCount signals are used to restart the watchdog counter based on specific conditions, including CPU tickling or special sequences of writes to the WDT configuration register.
6. The FPGAProgrammedWrite input is used for verifying the FPGA existence and programming. The WDT provides output data in FPGAProgDOut for this verification.
7. The SlowEnable signal enables the WDT to operate in slow mode.
8. The WD\_RST\_L signal is generated to trigger a module reset based on the WDT expiration.
9. The PowerUp process detects power-up conditions by monitoring PUReg.

## Simulation