*Project: RMC75E TEST BENCH*

*Module:* Clock\_Gen*.vhd*

*Author: Satchel Hamilton*

*Company: Delta Motion*

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# High Level

The "Clock\_Gen" entity represents a clock generator module. It takes inputs from the FPGA's CLK1\_PAD, PLL\_ARST\_N (PLL Active Reset), and PLL\_POWERDOWN\_N (PLL Power-Down) signals. The module generates three clock outputs, GL0, GL1, and GL2, and an output signal LOCK to indicate the PLL's lock status.

# Low level

**Inputs:**

* CLK1\_PAD: The input clock signal to the clock generator.
* PLL\_ARST\_N: Active-low reset signal for the PLL (Phase-Locked Loop).
* PLL\_POWERDOWN\_N: Active-low signal to enable the PLL.

**Outputs:**

* GL0: Clock output 0.
* GL1: Clock output 1.
* GL2: Clock output 2.
* LOCK: Output signal indicating the lock status of the PLL.

**Architecture:** The architecture "RTL" declares the instantiation of a component named "Clock\_Gen\_Clock\_Gen\_0\_FCCC," which is the actual implementation of the clock generator.

**Internal Signals:**

* GL0\_net\_0, GL1\_net\_0, GL2\_net\_0, LOCK\_net\_0: Internal signals to store clock generator outputs.
* GL0\_net\_1, GL1\_net\_1, GL2\_net\_1, LOCK\_net\_1: Internal signals used for sequential updates of the clock outputs.
* GND\_net: Internal signal representing a constant ground (logic 0).
* PADDR\_const\_net\_0: Internal signal storing a constant value for the address.
* PWDATA\_const\_net\_0: Internal signal storing a constant value for the write data.

**Functionality:**

1. The module connects the CLK1\_PAD input directly to the "Clock\_Gen\_Clock\_Gen\_0\_FCCC" component.
2. The clock generator component takes input signals and generates three clock outputs (GL0, GL1, and GL2) and a LOCK signal that indicates whether the PLL is locked.
3. Internal signals are used to store the clock generator outputs and update them sequentially to avoid glitches.

## Simulation