*Project: RMC75E TEST BENCH*

*Module:* Clock\_Gen\_Clock\_Gen\_0\_FCCC*.vhd*

*Author: Satchel Hamilton*

*Company: Delta Motion*

*Date: 7/13/2023*

*Last updated: July 13, 2023*

Contents

[High Level 1](#_Toc140670735)

[Low level: 3](#_Toc140670736)

[Simulation: 4](#_Toc140670737)

# High Level

The "Clock\_Gen\_Clock\_Gen\_0\_FCCC" entity represents a clock generator module responsible for generating the raw clock signals used by the RMC75E modular motion controller. These raw clock signals will be further processed and conditioned by the subsequent "clock\_gen" module. The module has several input and output ports, including LOCK, PLL\_ARST\_N, PLL\_POWERDOWN\_N, and CLK1\_PAD, and outputs GL0, GL1, and GL2.

# Low level

**Inputs:**

* PLL\_ARST\_N: Active-low reset signal for the PLL (Phase-Locked Loop).
* PLL\_POWERDOWN\_N: Active-low signal to enable the PLL.
* CLK1\_PAD: The input clock signal to the clock generator.

**Outputs:**

* LOCK: Output signal indicating the lock status of the PLL.
* GL0: Clock output 0.
* GL1: Clock output 1.
* GL2: Clock output 2.

**Internal Components:**

1. CLKINT: An internal component that generates a clock output based on its input.
2. INBUF: An internal component that buffers its input signal.
3. VCC: An internal component responsible for voltage supply.
4. GND: An internal component providing a constant ground signal.
5. CCC: An internal component responsible for generating clock signals with specific configurations.

**Internal Signals:**

* Various internal signals, such as GL0\_net, GL1\_net, GL2\_net, and others, are used for internal connections and signal routing.

**Functionality:**

1. The module uses internal components to handle buffering, voltage supply, and clock generation functionalities.
2. The CCC component is instantiated, which is responsible for generating clock signals with specific configurations based on its inputs.
3. The clock generator provides the raw clock signals (GL0, GL1, GL2) that will be further processed and conditioned by the "clock\_gen" module.

## Simulation