*Project: RMC75E TEST BENCH*

*Module: ControlOutput.vhd*

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# High Level

**Description:** The entity "ControlOutput" represents a module in the source code for the RMC75E modular motion controller. This VHDL module is responsible for controlling the output data to the digital-to-analog converter (DAC). The module takes input data (intDATA) from the processor and converts it to the MAX5541 format to drive the DAC. It uses a state machine to control the timing of data shifting and clocking into the DAC.

# Low level

**Inputs:**

* H1\_CLKWR: The write clock signal from the processor, used to latch intDATA into the DataBuffer.
* SysClk: The system clock signal used for synchronous operations.
* RESET: A synchronous reset signal to initialize the module.
* SynchedTick: A synchronized tick signal used to synchronize operations with other modules in the system.
* intDATA: The input data (16-bit) from the processor to be sent to the DAC.
* ControlOutputWrite: A control signal that indicates when new data is available for the module to process.
* PowerUp: A signal indicating that the system is powering up.
* Enable: A control signal that enables the module's functionality.

**Outputs:**

* M\_OUT\_CLK: The output clock signal used for clocking data into the DAC.
* M\_OUT\_DATA: The output data signal sent to the DAC.
* M\_OUT\_CONTROL: The control signal used to select the DAC (chip select).

**Architecture:** The architecture of the ControlOutput module, named ControlOutput\_arch, consists of several signals and processes.

**Signal Descriptions:**

* ShiftRegister: A 16-bit shift register used to shift data to the DAC.
* DataBuffer, DataBufferOut: A 16-bit word buffer that stores the input data (intDATA) coming from the processor. DataBufferOut is used to convert the data from two's complement to MAX5541 format.
* Count: A 5-bit synchronous counter used for timing control during the shift process.
* ControlOutputWriteLatched0, ControlOutputWriteLatched1, ControlOutputWriteLatched2: Signals used to detect the falling edge of ControlOutputWrite to start the shift process.
* ControlOutputOneShot: A one-shot signal that becomes active for a single SysClk cycle after a data write or during power-up.
* OutputClock: An output clock signal used for clocking data into the DAC.
* ShiftEnable: A control signal to enable data shifting.
* ShiftComplete: A signal indicating the completion of the shift process.
* ShiftDataOutput: The data output of the shift register to be sent to the DAC.

**Processes:**

1. H1\_CLKWR Process: This process handles the latching of the input data (intDATA) into the DataBuffer when ControlOutputWrite is asserted.
2. DataBufferOut Process: This process converts the data from two's complement to MAX5541 format by inverting the 14-bit data and appending the sign bit.
3. StateMachine Process: This process controls the state transitions based on the system clock (SysClk), SynchedTick, ControlOutputOneShot, and ShiftDataOutput. It manages the states s0 and s1. In s0 state, the module waits for the falling edge of ControlOutputWrite to transition to the s1 state and start the shift process.
4. Shift Register and Counter Process: This process handles the data shifting operation. It uses the ShiftEnable and OutputClock signals to load data into the ShiftRegister, and it performs the shift operation during the OutputClock's rising edge.

## Simulation

To simulate the ControlOutput module, a testbench can be created with appropriate stimuli for the inputs (H1\_CLKWR, SysClk, RESET, SynchedTick, intDATA, ControlOutputWrite, PowerUp, Enable). The simulation should observe the behavior of the M\_OUT\_CLK, M\_OUT\_DATA, and M\_OUT\_CONTROL signals and verify that the data is correctly shifted into the DAC according to the state machine's control. The testbench should test various scenarios, including the data write process, shift operation, and module functionality during power-up, to ensure the correct functionality of the module.