*Project: RMC75E FPGA TEST BENCH*

*Module: module.vhd*

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# High Level

The module "Decode" is responsible for generating WRITE control lines and READ control lines based on the input address and control signals. It is a decoder module for interfacing with various peripheral devices.

Key features of the module:

1. It takes various inputs, including the address (ADDR), read (RD\_L), write (WR\_L), and chip select (CS\_L) control signals, as well as several other control signals for different peripheral devices.
2. The module supports multiple peripheral devices, such as FPGA, analog interface, quadrature decoder, etc. Each peripheral has its read and write control signals.
3. The module provides various output control signals, one for each peripheral, to enable/disable read or write operations to the respective peripherals.
4. Some of the peripherals supported include FPGA (with read and write enable), CPU configuration (read and write), CPU LED (read and write), Watch Dog Timer (read and write), PROFIBUS address, Serial Memory Interface (read and write), etc.
5. The module seems to handle different peripheral addressing, allowing communication with multiple instances of a peripheral type (e.g., multiple axes).
6. The decoding process is carried out through conditional assignments of signals based on the input address and control signals, allowing the appropriate peripheral control signals to be activated when the correct conditions are met.

Key functionalities of the decoder include:

1. Handling control signals for the FPGA and CPU board.
2. Decoding CPU board configuration reads and writes.
3. Decoding CPU board LED reads and writes.
4. Handling control signals for Axis 0 and Axis 1 modules.
5. Decoding signals related to the MDT and Analog modules.
6. Decoding signals related to the Quadrature (QUAD) module.
7. Decoding expansion card control signals, including analog and digital I/O.

# Low level

Low-level section overview:

The architecture "Decode\_arch" consists of signal declarations and logic for address decoding and signal routing. The module performs address decoding based on the input ADDR signal to determine which control signals should be activated for different read and write operations. It also uses various control signals like CS\_L (chip select), RD\_L (read enable), and WR\_L (write enable) to further refine the decoding process.

The decoder connects to multiple modules, such as the FPGA, CPU board, and various expansion cards (Exp0, Exp1, Exp2, and Exp3). For each module, specific read and write operations are decoded, and relevant control signals are generated accordingly. The module also handles conditional checks for the presence of specific modules like MDTPresent, ANLGPresent, and QUADPresent to activate appropriate control signals related to those modules.

The signal declarations define various control and data lines for communication with different modules, including inputs, outputs, and bidirectional signals. These signals represent different functionalities, like reading from and writing to configuration registers, reading analog and quadrature data, accessing the CPU and FPGA, etc.

Overall, the "Decode\_arch" architecture serves as a crucial component in the digital system, enabling proper communication and control between different modules based on address decoding and control signal generation.

## Simulation