*Project: RMC75E FPGA TEST BENCH*

*Module: module.vhd*

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# High Level

**Description:** The entity "DiscoverControlID" represents a module in the source code for the RMC75E modular motion controller. This VHDL module is responsible for controlling the discovery of the control ID for the motion controller. The module handles the process of capturing the control ID using a state machine and shifting the ID into the ControlID signal.

# Low level

**High-Level Documentation - DiscoverControlID Module**

**Description:** The entity "DiscoverControlID" represents a module in the source code for the RMC75E modular motion controller. This VHDL module is responsible for controlling the discovery of the control ID for the motion controller. The module handles the process of capturing the control ID using a state machine and shifting the ID into the ControlID signal.

**Low-Level Documentation - DiscoverControlID Module**

**Design Details:** The DiscoverControlID module is designed to discover the control ID for the motion controller. It uses a state machine and a shift register to capture the control ID data provided by an external module through M\_Card\_ID\_DATA. The module generates an output clock signal (M\_Card\_ID\_CLK) and controls the signals M\_Card\_ID\_LOAD and M\_Card\_ID\_LATCH to facilitate the data capturing process.

**Inputs:**

* RESET: A synchronous reset signal to initialize the state machine and shift register.
* SysClk: The system clock signal used for synchronous operations.
* SlowEnable: A control signal that enables the generation of a 5MHz clock output for the serial communication state machine.
* M\_Card\_ID\_DATA: The data input signal containing the control ID data from an external module.

**Outputs:**

* ControlID: A 17-bit bidirectional signal that holds the captured control ID data.
* M\_Card\_ID\_CLK: The output clock signal for the state machine.
* M\_Card\_ID\_LATCH: The output signal to control the latch signal for capturing the control ID data.
* M\_Card\_ID\_LOAD: The output signal to control the load signal for capturing the control ID data.

**Architecture:** The architecture of the DiscoverControlID module, named DiscoverControlID\_arch, consists of two processes.

1. StateMachine process: This process controls the state transitions based on the system clock (SysClk) and the SlowEnable signal. It drives the control signals M\_Card\_ID\_LOAD, M\_Card\_ID\_LATCH, and ShiftEnable. The state machine goes through different states to perform the capture operation. It starts with s0\_LatchState, proceeds to s1\_DelayState1, s2\_LoadState, s3\_DelayState2, s4\_ClockState, and finally reaches s5\_StopState.
2. Process for Shift Register and Counters: This process handles the data capture and shifting process. It captures the M\_Card\_ID\_DATA and performs a shift operation on the ControlID signal based on the OutputClock signal generated by the state machine. It also handles the Count signal, which serves as a 4-bit synchronous counter with count enable and asynchronous reset. The process uses TerminalCountValue (X"F") to determine the terminal count value, and when the count reaches this terminal count and SlowEnable is '1', the ShiftComplete signal is set to '1'. ShiftComplete is used to indicate the completion of the shift operation.

## Simulation

To simulate the DiscoverControlID module, a testbench can be created with appropriate stimuli for the inputs (RESET, SysClk, SlowEnable, M\_Card\_ID\_DATA). The simulation should observe the behavior of the ControlID signal, M\_Card\_ID\_CLK, M\_Card\_ID\_LATCH, and M\_Card\_ID\_LOAD. The testbench should test different scenarios, including the reset condition, state transitions, and successful data capture, to ensure the correct functionality of the module.