*Project: RMC75E FPGA TEST BENCH*

*Module: module.vhd*

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# High Level

**Description:** The LatencyCounter module is responsible for receiving clock and control signals and providing output data based on its internal latency calculations. The module accepts three inputs: a 60MHz clock signal (H1\_CLK), a control signal to synchronize the operation (SynchedTick), and a signal to read the latency count (LatencyCounterRead). The output of this module is a 32-bit data output (latencyDataOut) representing the latency calculation.

# Low level

**Design Details:** The LatencyCounter module is designed as a synchronous process, triggered by the falling edge of the H1\_CLK signal. It uses two internal signals, "LatencyCounter" and "latencyDataOut," both of which are 32-bit vectors.

**Functionality:**

1. On each falling edge of H1\_CLK, the process checks the SynchedTick signal.
   * If SynchedTick is '1', indicating the start of a new latency measurement, the LatencyCounter is reset to zero.
   * If SynchedTick is '0' (low), and LatencyCounterRead is '0' (low) as well, the LatencyCounter is incremented by one.
2. The latencyDataOut output always reflects the current value of the LatencyCounter register, representing the calculated latency in clock cycles.

## Simulation

The LatencyCounter module will be thoroughly tested using ModelSim. The testbench will provide various input scenarios, including different combinations of H1\_CLK, SynchedTick, and LatencyCounterRead signals, to verify the correct behavior of the module. The simulation will check that the latency calculation accurately reflects the time between the falling edge of H1\_CLK and the activation of the SynchedTick signal. Additionally, edge cases and corner cases will be considered to ensure the module's robustness and reliability. The simulation results will be analyzed to ensure that the module operates correctly under different conditions and that the latencyDataOut output is accurate. Any issues or discrepancies identified during simulation will be debugged and addressed to ensure the module's correctness and effectiveness.