*Project: RMC75E FPGA TEST BENCH*

*Module: MDTSSIRoute.vhd*

*Author: Satchel Hamilton*

*Company: Delta Motion*

*Date: 7/13/2023*

*Last updated: July 13, 2023*

Contents

[High Level 1](#_Toc140670735)

[Low level: 1](#_Toc140670736)

[Simulation: 2](#_Toc140670737)

# High Level

The MDTSSIRoute module describes the interface and behavior of a routing module for the Magnetostrictive Displacement Transducer (MDT) and Synchronous Serial Interface (SSI) clocks in the RMC75E modular motion controller. It takes input signals related to the SSI select, internal MDT clock, SSI clock, and MDT interrupt, and provides output signals for the internal clocks of Axis0 and Axis1.

# Low level

Design Details:

The MDTSSIRoute module is designed as a synchronous process, controlled by conditional assignments. It uses the SSISelect signal to select the appropriate clock source for each axis.

Inputs:

SSISelect: A 2-bit signal that selects the clock source for each axis. '00' selects the MDT internal clock, and '01' selects the SSI clock.

M\_AX0\_SSI\_CLK: Input SSI clock signal for Axis0.

M\_AX1\_SSI\_CLK: Input SSI clock signal for Axis1.

M\_AX0\_MDT\_INT: Input MDT interrupt signal for Axis0.

M\_AX1\_MDT\_INT: Input MDT interrupt signal for Axis1.

Outputs:

M\_AX0\_INT\_CLK: Output internal clock signal for Axis0.

M\_AX1\_INT\_CLK: Output internal clock signal for Axis1.

Functionality:

On each clock cycle, the MDTSSIRoute module checks the value of the SSISelect signal and performs the following assignments:

M\_AX0\_INT\_CLK is assigned the value of M\_AX0\_MDT\_INT when SSISelect(0) is '0', indicating that the MDT internal clock is selected for Axis0. Otherwise, it is assigned the value of M\_AX0\_SSI\_CLK, indicating that the SSI clock is selected.

M\_AX1\_INT\_CLK follows a similar assignment logic as M\_AX0\_INT\_CLK but for Axis1.

The MDTSSIRoute module provides the functionality to select the appropriate clock source for each axis based on the SSISelect signal. It enables the routing of clock signals between the MDT internal clock and the SSI clock, allowing flexible control over the timing and synchronization of operations within the modular motion controller.

## Simulation

The MDTSSIRoute module will be thoroughly tested using ModelSim. The testbench will provide various input scenarios, including different combinations of SSISelect, M\_AX0\_SSI\_CLK, M\_AX1\_SSI\_CLK, M\_AX0\_MDT\_INT, and M\_AX1\_MDT\_INT signals, to verify the correct behavior of the module. The simulation will check that the output signals, M\_AX0\_INT\_CLK, and M\_AX1\_INT\_CLK, reflect the selected clock sources based on the SSISelect input. Additionally, edge cases and corner cases will be considered to ensure the module's robustness and reliability. The simulation results will be analyzed to confirm that the module operates correctly under different conditions, meeting the intended functionality requirements.

**Version Control:** The MDTSSIRoute module will be under version control using Git. Proper commit messages and version tagging will be used to track changes, enhancements, and bug fixes over time. This version control will enable efficient collaboration among team members during the development process.