*Project: RMC75E FPGA TEST BENCH*

*Module: module.vhd*

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# High Level

The TickSync module synchronizes the incoming control loop clock tick with the internal clock, making it synchronous and usable by the internal logic. It provides the Sync'edTick pulse, which is output immediately after syncing up to the incoming tick pulse.

# Low level

**Design Details:** The TickSync module is designed to synchronize the incoming LOOPTICK signal with the SysClk signal. It also generates a 60 MHz H1\_CLK signal to simulate the incoming clock. The module includes the following ports:

**Inputs:**

* SysReset: Asynchronous reset signal to initialize loop ticks low.
* SysClk: The system clock.
* H1\_CLK: Input clock with a frequency of 60 MHz.
* LOOPTICK: The incoming control loop clock tick.

**Outputs:**

* SynchedTick: Synchronized tick output.
* SynchedTick60: Synchronized 60 MHz tick output.

**Functionality:** Upon reset, the SysReset signal initializes LOOPTICK and SynchedTick to low. The TickSync module then synchronizes LOOPTICK to SysClk by using rising\_edge detection on SysClk. The synchronized tick output, SynchedTick, is set to high during the rising edge of SysClk when LOOPTICK is high. The module generates a 60 MHz clock, H1\_CLK, using rising\_edge detection on SysClk, which will serve as an input clock for testing purposes. Additionally, the SynchedTick60 output is set to high during the rising edge of H1\_CLK when LOOPTICK is high.

## Simulation

The TickSync module will be extensively tested using a ModelSim testbench, "tb\_TickSync." The testbench includes clock stimuli to generate SysClk and H1\_CLK. It verifies the correct functionality of the TickSync module by running multiple test sequences:

1. Test LOOPTICK Pulse: It checks if SynchedTick becomes '1' when LOOPTICK is high and SysClk is at a rising edge.
2. Test Reset During LOOPTICK: It verifies that SynchedTick becomes '0' when a reset is triggered during a high LOOPTICK.
3. Test SynchedTick60: It checks if SynchedTick60 becomes '1' when LOOPTICK is high and H1\_CLK is at a rising edge.

The simulation results will be analyzed to ensure the TickSync module operates correctly, meeting the synchronization requirements and providing the expected output signals. The simulation will include various scenarios and edge cases to validate the module's robustness and reliability.