Project: RMC75E Test Bench  
  
Problem: Type mismatch between Boolean and std\_logic types. Version mismatch between VHDL version 2002 and the used version 2008.

Solution:

1. Launch ModelSim by double-clicking on its icon or running the corresponding executable. You should be able to access the GUI interface.
2. Open your VHDL source file(s) in ModelSim by selecting "File" from the menu bar and choosing "Open". Navigate to the directory where your VHDL files are located and select the relevant file(s).
3. Once the file(s) are open, go to the "Compile" menu and select "Compile Options". This will open the compile options dialog box.
4. In the compile options dialog box, you should find an option to specify the VHDL version. Look for a dropdown menu or a text field where you can specify the VHDL version. Choose "VHDL-2008" if available. Otherwise, select the highest available version that is compatible with your code.
5. Additionally, look for an option to change the interpretation of signals between **std\_logic** and **boolean** types. It may be labeled as "Signal Representation" or something similar. Select "Boolean" or "Boolean Logic" if available.
6. Once you have made the necessary changes to the compile options, click "OK" to close the dialog box.
7. Finally, recompile your VHDL code by selecting "Compile" from the menu bar and choosing "Compile" or by using the corresponding toolbar button. ModelSim will recompile your code with the updated settings.

By adjusting the compile options within the ModelSim GUI, we can potentially resolve the VHDL version and type mismatches that you encountered.  
  
Solved most of the compile issues with step 3.  
  
Was able to solve the other two by doing the following:  
  
controlio:  
Added a catch-all statement to resolve dangling states.  
  
ExpModuleLED:  
vcom -work work -2008 -explicit -stats=none -suppress 1339 {C:\Users\SHAMILTON\Desktop\Test\_Bench\_RMC75E\ExpModuleLED.vhd}