Project Code	Title	Remarks
ESC17	**Scalable Control-flow graph (CFG) generation for Verilog Input files**	Embedded systems can be analyzed through CFG analysis. You are asked to write a code to generate CFG for any size of code (verilog input provided to you). You receive a ZERO if your code fails on random test cases or you copy code from somewhere else.
ESC18	**ZipCPU (RISC core) simulation**	Follow from here: https://github.com/ZipCPU/zipcpu/
ESC19	**FreeRTOS (Real Time Operating System) implementation for resource-constrained mobile devices**	Implement some version of FreeRTOS (at a small model) for resource-constrained mobile devices
ESC20	**Data leakage or data integrity attacks in CPUs/embedded systems**	Apply any technique to perform a data leakage or data integrity attacks in CPUs/embedded systems (the embedded system could be written in C/C++)
ESE15	**Floating-point unit implementation for embedded systems in Verilog**	Make a floating-point CPU for connecting with other peripherals. You receive a ZERO if you copy code from somewhere else.
ESE16	**Digital Signal Processor implementation for a Multiply-accumulate (MAC) unit in Verilog**	Follow from here https://microchipdeveloper.com/dsp0201:mac-overview and do simulation for large number of MAC operations