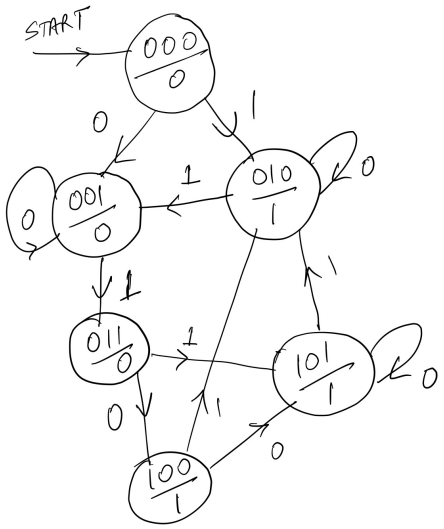
Indian Institute of Technology Jodhpur
Department of Electrical Engineering
End Term Examination
[EEL2020/CSL2070] Digital Design

MM: 60 April 28, 2022
Time: 2 hours

1. A car parking system employs sensors to detect the occupancy of a parking area. Design the hardware to implement the following minimum functionalities.
   - Space of parking 12 cars with sensors S1 to S12.
   - In each parking slot, the sensor gives output 1 when a car is parked, and 0 when the parking area is empty.
   - An LED indicator outside to show whether the parking is full (RED LIGHT) or vacant (GREEN LIGHT).
   - A counter to show the number of vacant parking slots.

   Write a Verilog Code for the design. Give a clear block diagram to explain the inputs, outputs and various parts of the code. [Do not write a code for display unit. It is understood that the counter output will go to display unit. Only show this in the block diagram] [10]

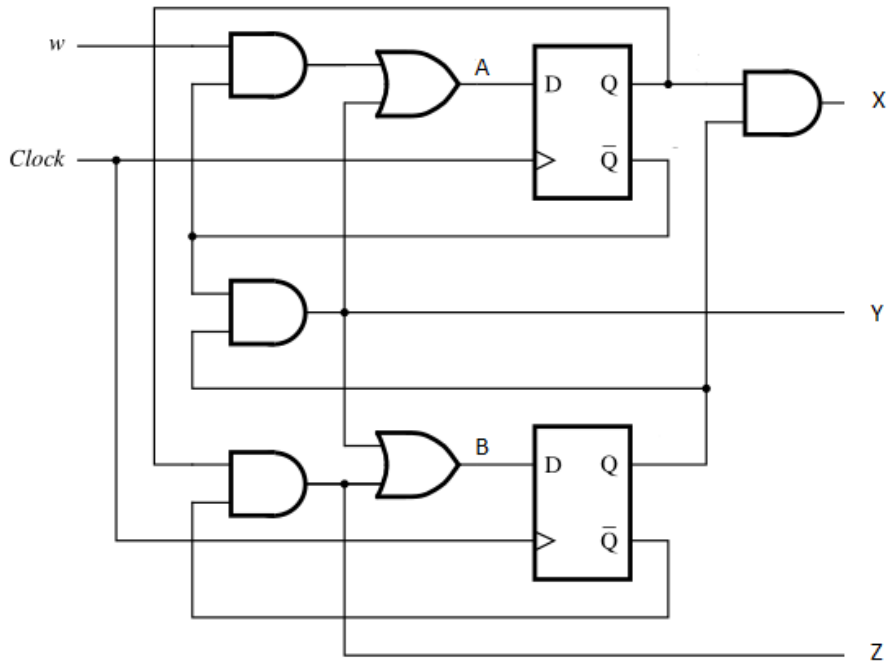
2. Reduce the following state diagram [2]

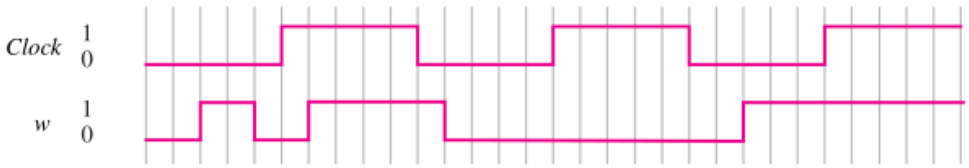


   Implement the minimum design using
   a) D flip-flops [4]
   b) J-K flip-flops [4]
   c) T-flip-flops [4]
   d) Analyze the design of (b) to show unused states in the final design. [3]

3. A circuit is shown below with the following timing parameters for individual components.
   - AND Gate propagation delay: 3 ns
   - OR Gate propagation delay: 2 ns

   The input and clock signals are also shown in the figure, with markings at 1 ns.





a) Provide the sequences for A,B,X,Y,Z (with 1 ns timing). Assume that the flip-flops are ideal, and in reset state initially. [2 × 5]

b) Suppose, the following timing parameters are available for the D flip-flops.
   - Setup time [Data must be available at D before the active edge]: 1 ns.
   - Hold time [Data must be available at D after the active edge]: 1 ns.
   - Propagation delay [Data is available at Q and Q' after the active edge of clock]: 4 ns.

   What is the maximum frequency at which this circuit can operate. Justify your answer. [5].

4. A combinational circuit is given by $Z = AC' + A'C + BC' + AB'$

   a) Show the internal structure/connections of the LUT, and SRAM data for implementing Z with

      i. 2 input LUTs [3]

      ii. 3 input LUTs [3]

   b) Show the implementation (programming) of Z on FPGA with 2 input LUTs of part (a). [6]

5. A synchronous counter is desired that provides a 3 bit gray code output sequence with the following properties.

   - State 000,111 does not occur. These are skipped in the sequence.
   - States 001,010,100 stays for 1 clock cycle.
   - States 011,101,110 stays for 2 clock cycles.

   a) Provide the state diagram for the design. [3]

   b) Provide the state table for the design. [3]