Parallelization in CosmoLattice

September 2025, Daejeon

Franz R. Sattler

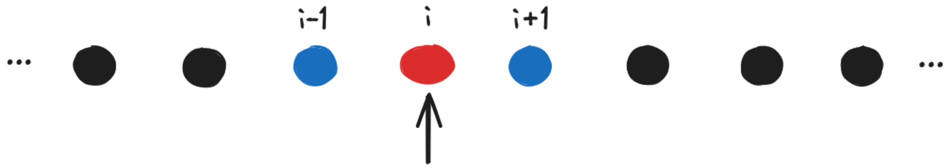
Bielefeld University

Why can we parallelize?

And why would we want to?

Example: Solving massless Klein-Gordon equation, $d = 1$

$$\partial_t^2 \phi(i) = \Delta_i^+ \Delta_i^- \phi(i)$$



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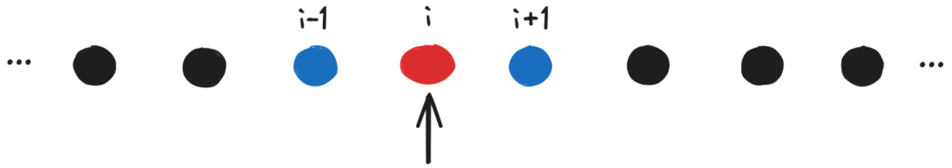
$$\begin{aligned} \partial_t \pi(i) &= \Delta_i^+ \Delta_i^- \phi(i)\,, \\ \partial_t \phi(i) &= \pi(i)\,. \end{aligned}$$

(Leapfrog scheme.)



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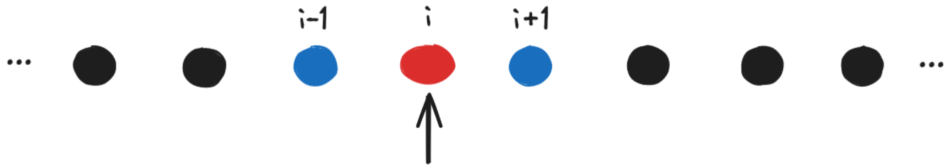

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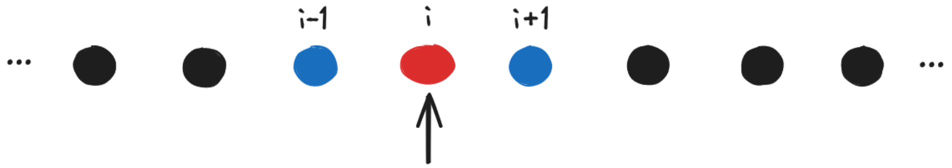

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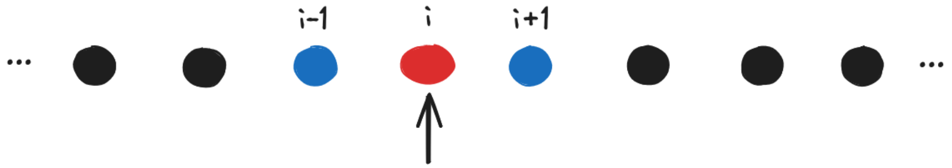

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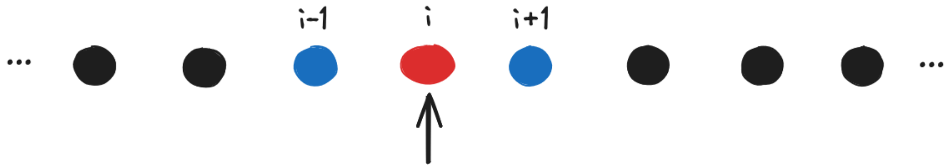

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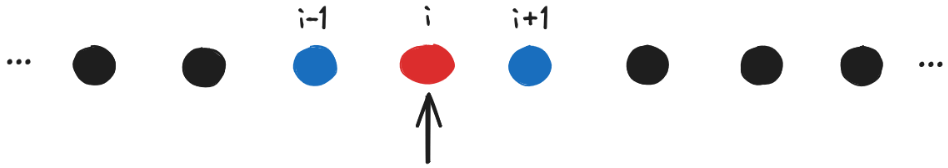

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Less granular: split sub-regions of lattice across many computers (nodes)

Parallelization of CosmoLattice

simulations requires to split both computation and data across cores.

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Cores: **Nodes** (distributed) and **Threads** (shared).

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Type	distributed	shared
Data	split between **nodes**	shared by all **threads**
Computation	split between **nodes**	split between **threads**

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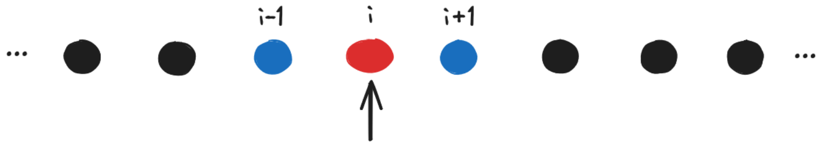

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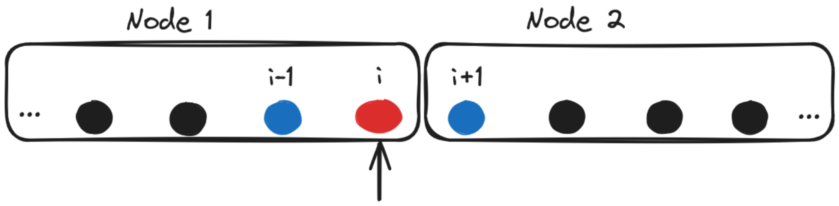

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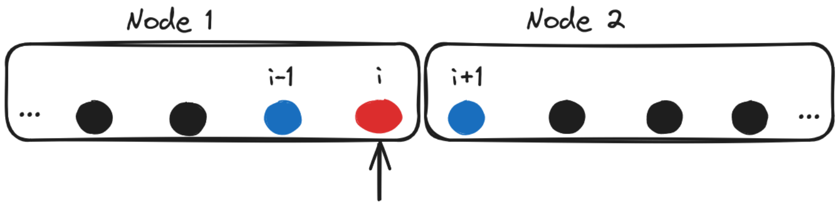

Problem: Data is missing on node 1

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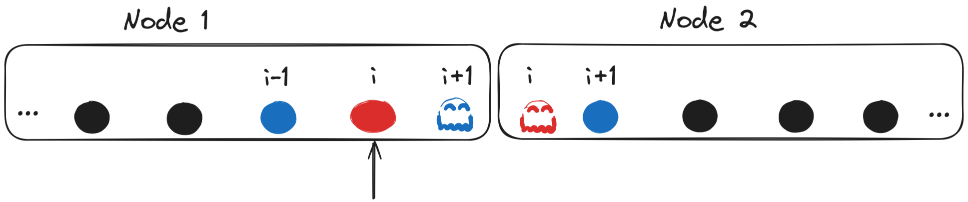

Solution: Use ghosts.

Ghosts are local copies of data on other nodes.

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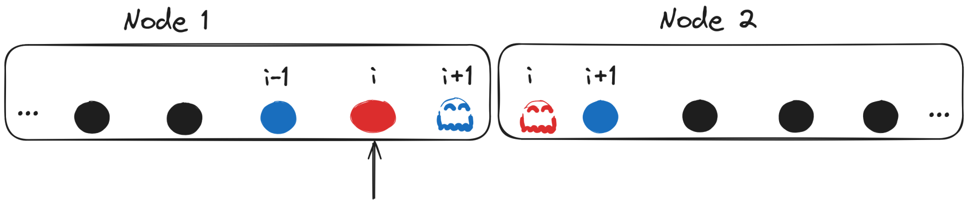


Solution: Use ghosts.

Ghosts are local copies of data on other nodes.

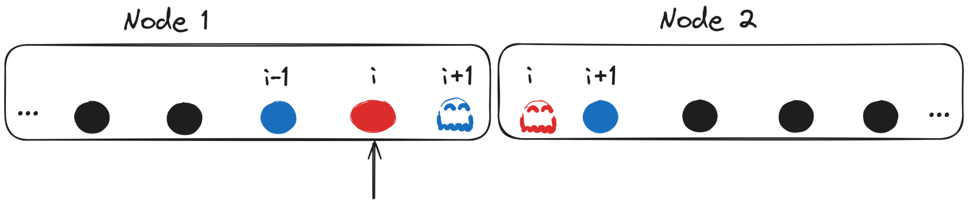
Need to update ghosts after every time-step.

Data communication

The standard for communication in distributed-memory applications:

Message **P**assing **I**nterface (MPI)

Exchange ghost data between **nodes** over the **network** automatically if anything changes.



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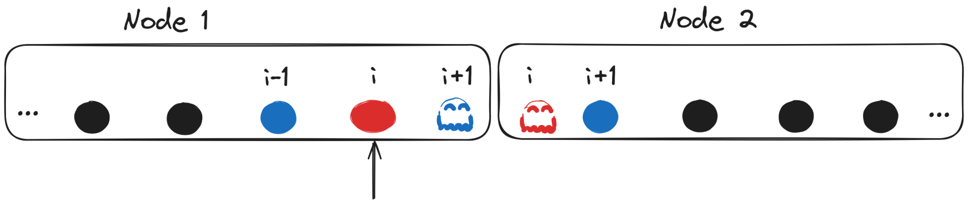

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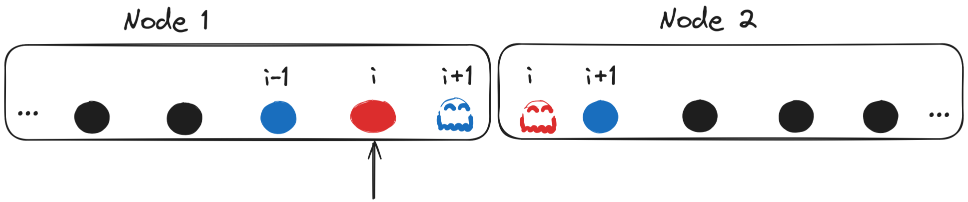

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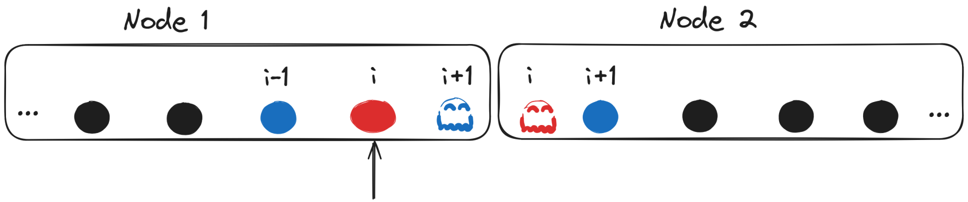

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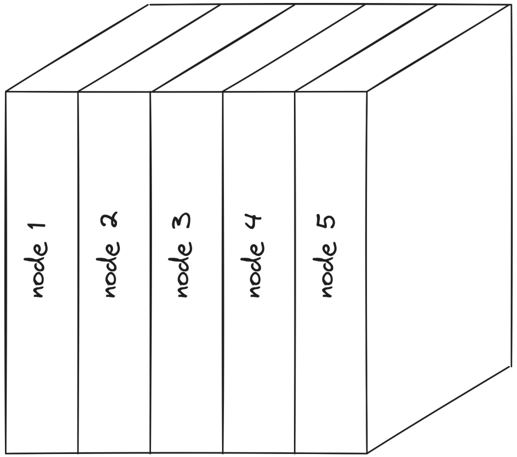
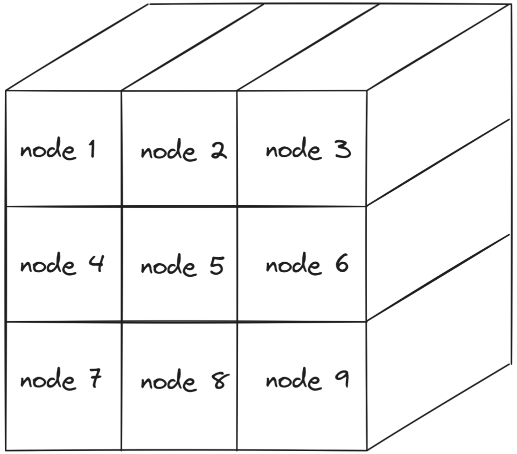
You may need to install fftw3 with MPI support.

```
$ sudo apt-get install libfftw3-mpi-dev
```

FFT parallelization

- **FFTW** supports parallelization along 1 direction.





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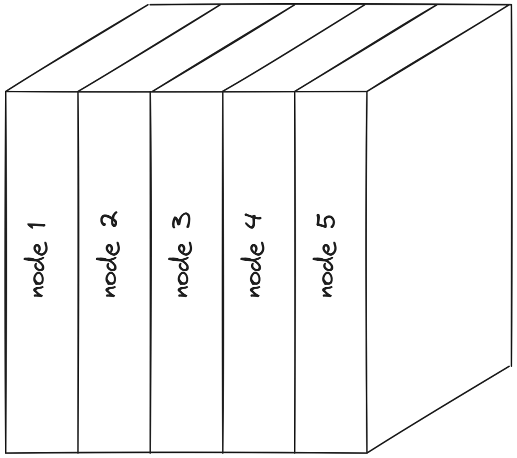
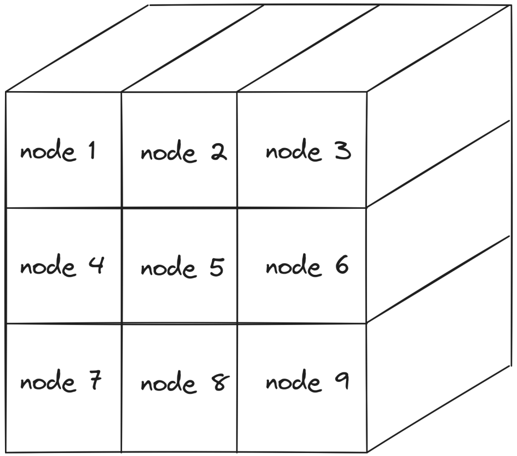
- Improved scaling for many nodes: **PFFT** allows for parallelization in any dimensions.





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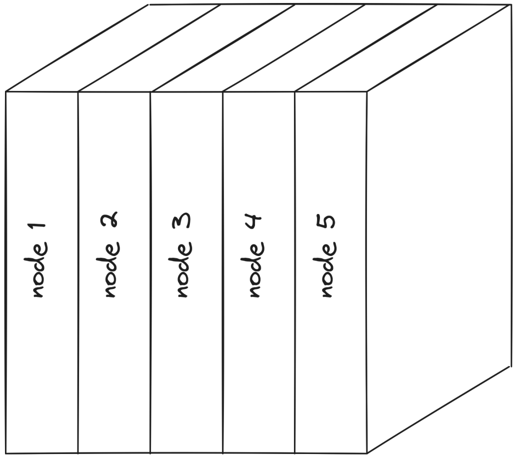

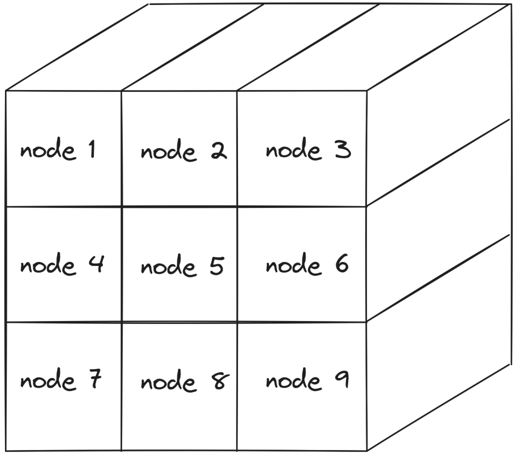

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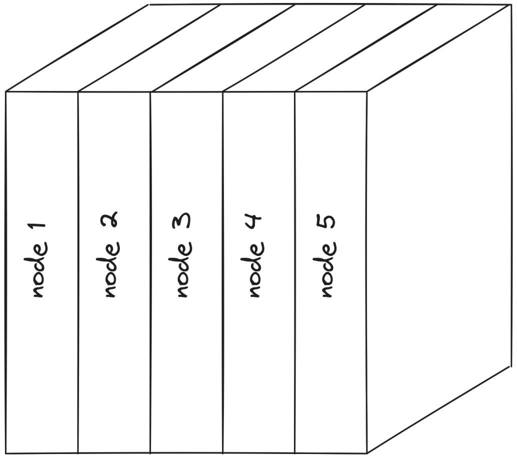

1D

$$N = n_p * m$$

$$N = 50$$

2D

$$N = n_p^{(1)} * m$$
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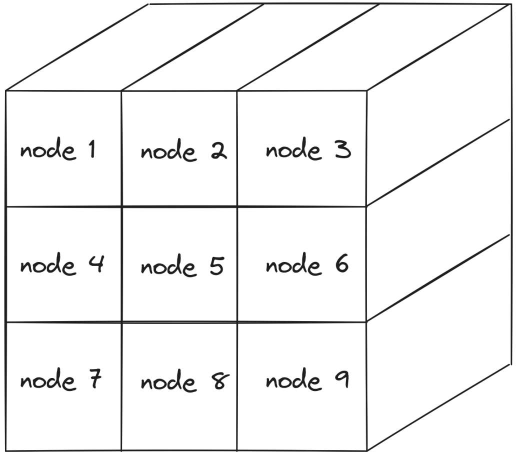

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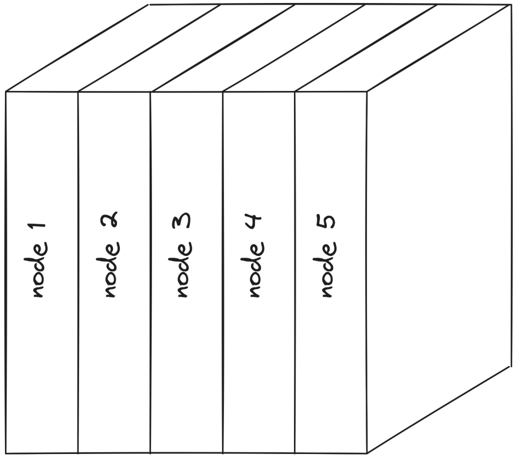

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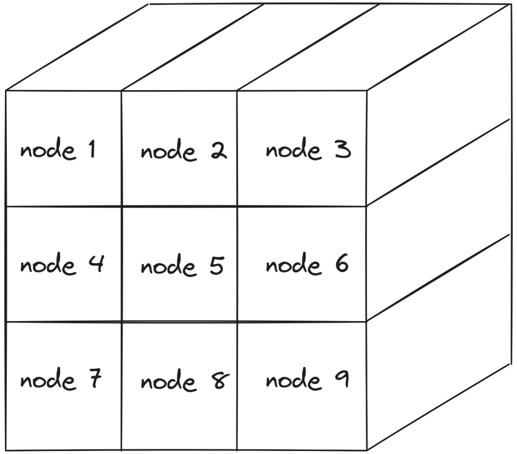

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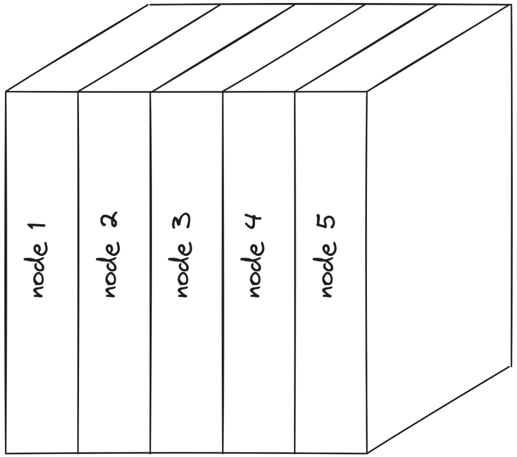

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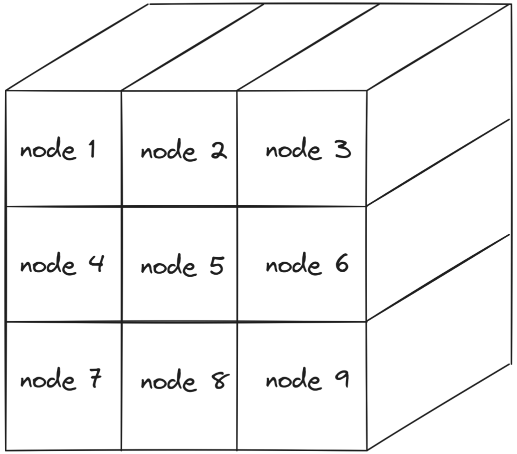
Maximum parallelization

50 nodes.

$25^2 = 625$ nodes.



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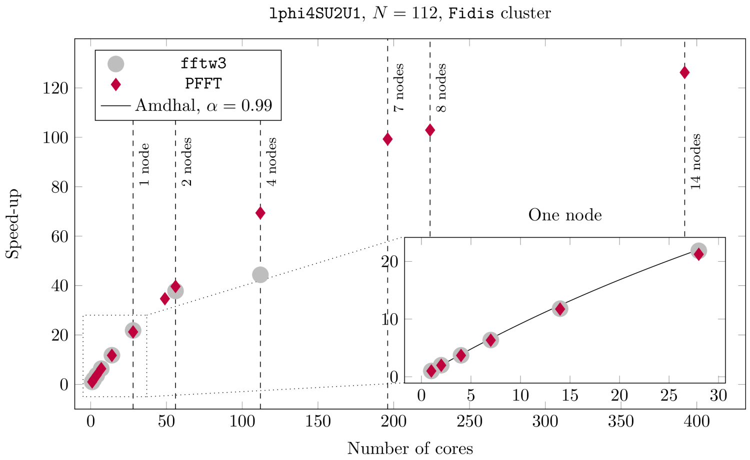
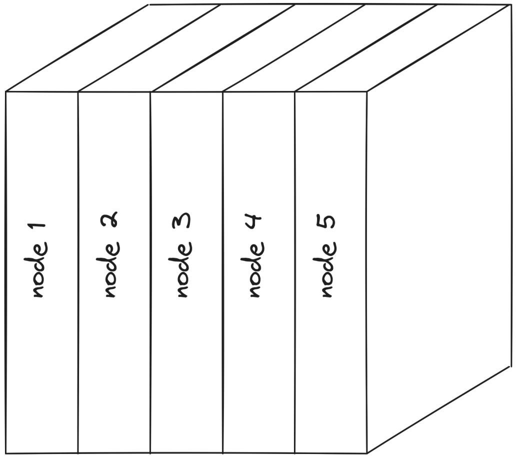
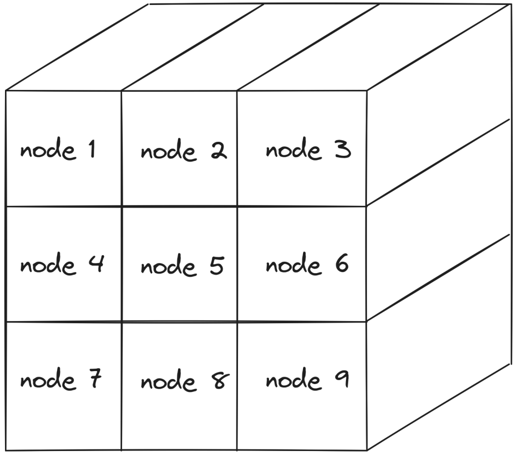


Figure 3: Speed up factor in parallelized simulations as a number of cores (tested on the Gacrux cluster from the EPFL HPC center SCITAS, Switzerland).





Questions?

Tomorrow: Shared-memory parallelization with GPUs.

CosmoLattice on GPUs

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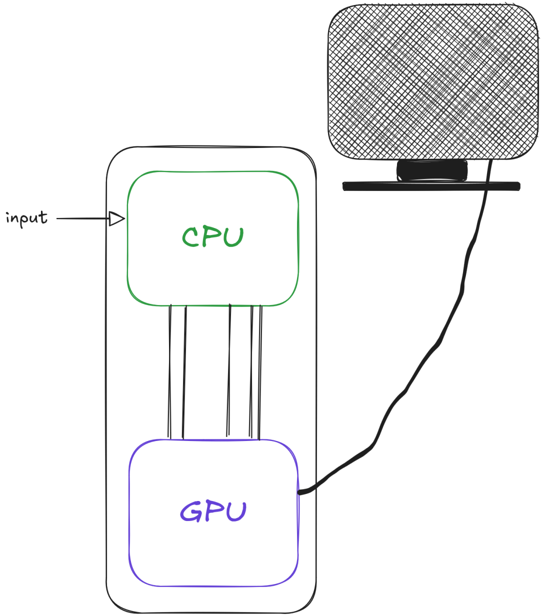

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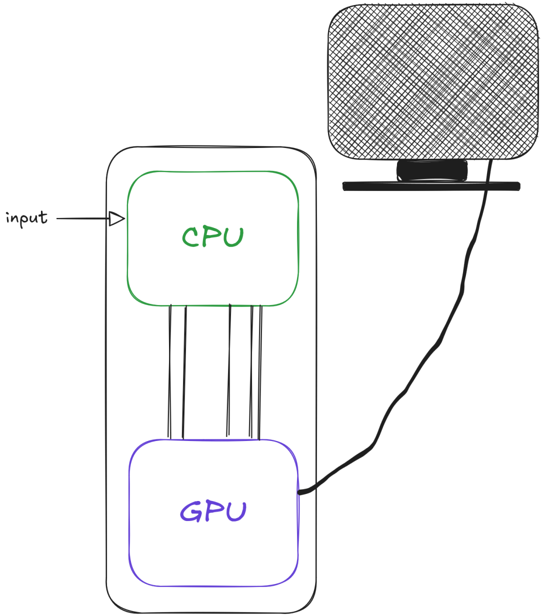
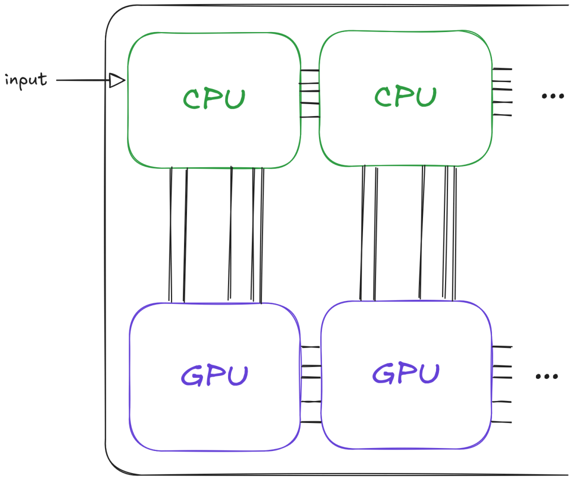


A consumer machine

Current (heterogeneous) clusters have both CPUs and GPUs for **computations**.



A typical heterogeneous computing cluster

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- AMD EPYC 7763: **64**
- Intel Xeon 6148 (Skylake): **20**
- AMD Ryzen 9 7945HX: **16**

	CPU	GPU
Cores/Node	$\mathcal{O}(10 - 100)$	$\mathcal{O}(10000)$
Clock speed	~ 3 GHz	~ 1.5 GHz

- Nvidia H100: **~15000**
- Nvidia RTX4070m: **~5000**

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CPU: Low parallelization, high clock speed

GPU: High parallelization, moderate clock speed

→ CosmoLattice on GPUs has the potential for *massive parallelism* with $\gg 10^5$ simultaneous operations.

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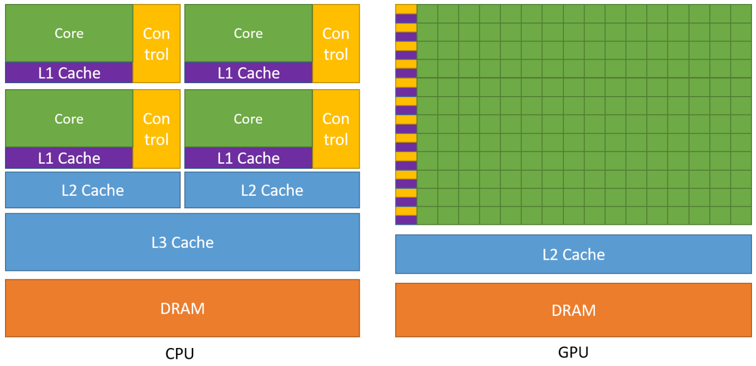
	CPU	GPU
Cache/Thread	64KB / 16MB	1KB
Local Cache	64MB	256KB / 50MB

CPU: **Thread-constrained**

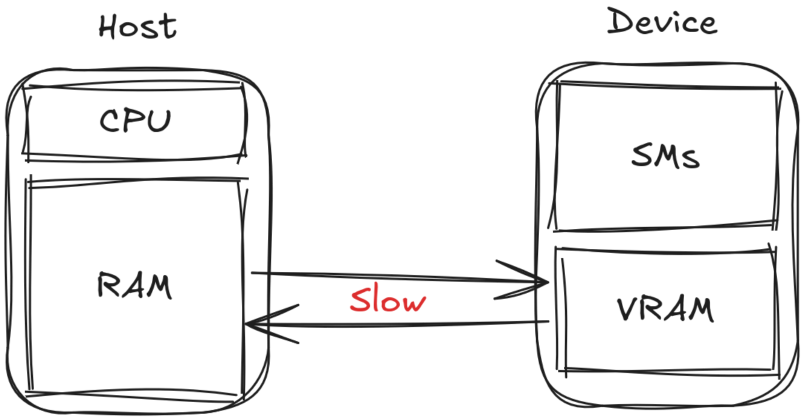
GPU: **Memory-constrained**



Hardware layouts [docs.nvidia.com]

Redesigning TempLat for GPUs

Device-centric programming.



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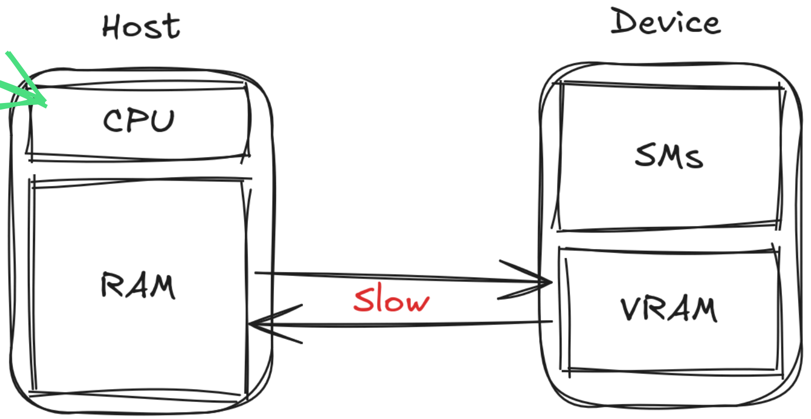
Sequential work,

- ~~expression~~ construction
- program flow logic
- device dispatch.



$$\text{expression} = \pi(t) + dt \cdot \Delta\phi(t)$$

Time evolution

Redesigning TempLat for GPUs

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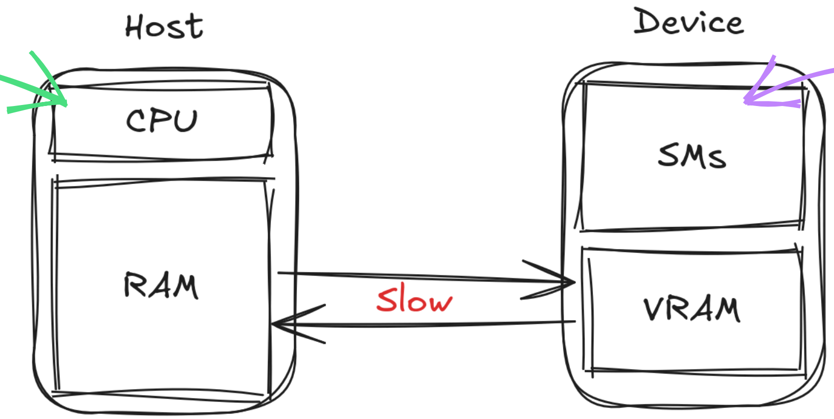

Parallel (grid-based) work,

- ~~time evolution~~
- measurements
- memory reordering.

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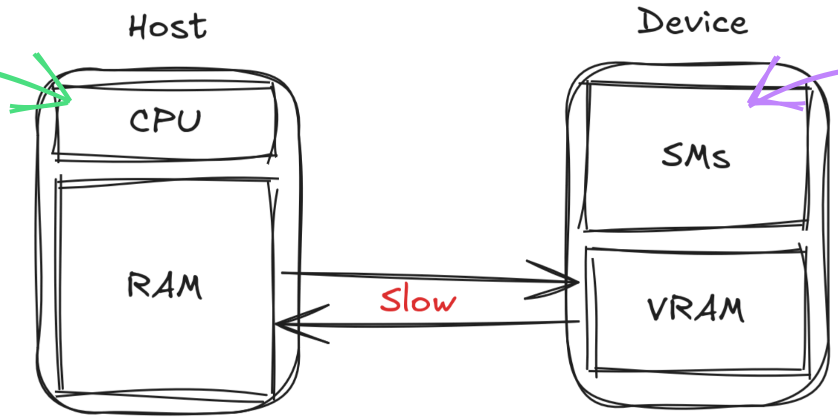

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auto functor = DEVICE_LAMBDA(device::IdxArray<NDim> idx,
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};
double maximum = 0.;
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Maximum

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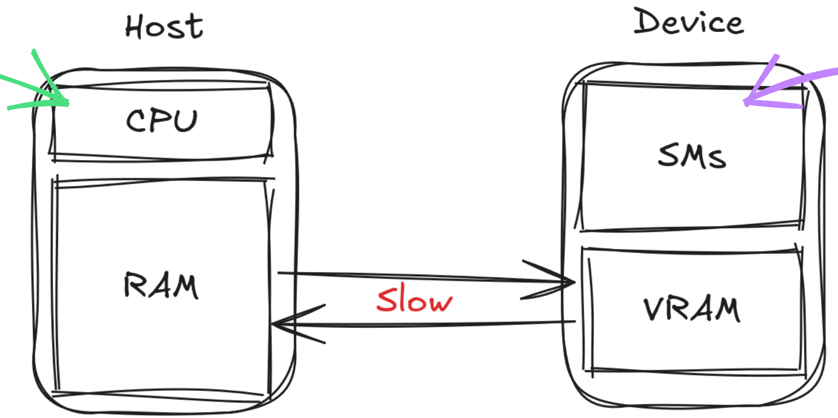

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Maximum

```
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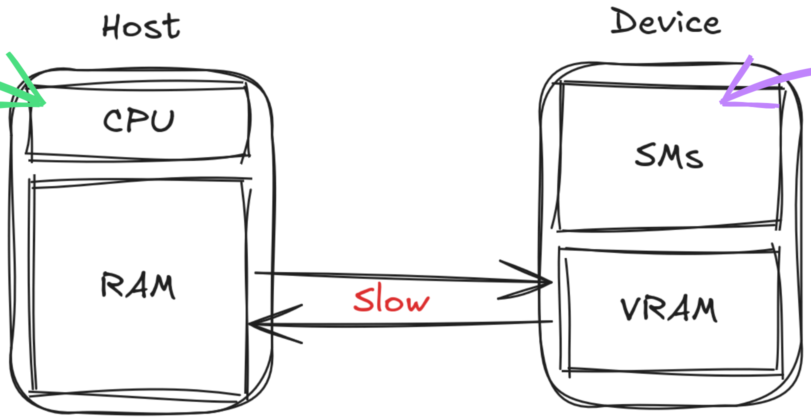


Parallel (grid-based) work,

- ~~time evolution~~
- measurements
- memory reordering.

Standard C++ on CPU

Hardware-dependent

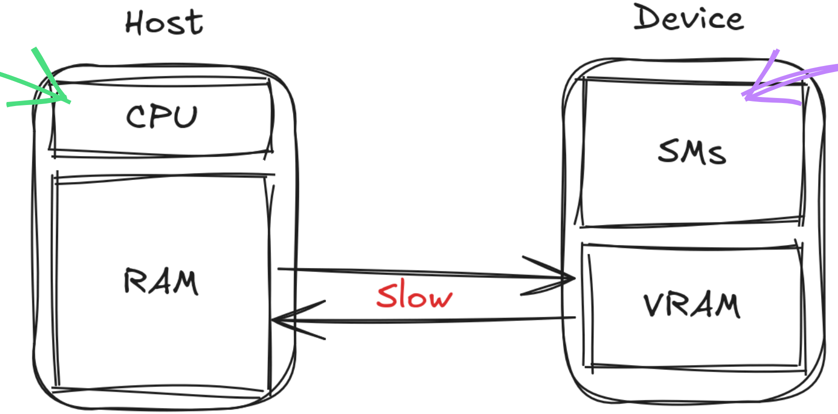
- NVIDIA: CUDA
- AMD: ROCM
- Intel: SYCL
- shared-memory CPUs
- FPGPAs

Redesigning TempLat for GPUs

Device-centric programming.

Sequential work,

- ~~[illegible] construction~~
- program flow logic
- device dispatch.



Parallel (grid-based) work,

- ~~time evolution~~
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- memory reordering.

Standard C++ on CPU

Backends

- *Kokkos*
- *Sequential STL (2020/2023)*
- …

Abstracted away in TempLat

- `device::iterate::foreach`
- `device::iterate::reduce`
- `device::memory::copyHostToDevice`
- …

Does this make CosmoLattice harder to use?

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No, but…

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Model file

```
public:

  MODELNAME(ParameterParser &parser, RunParameters<double> &runPar,
      std::shared_ptr<MemoryToolBox> toolBox)
    ...
```

Does this make CosmoLattice harder to use?

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Model file

```
public:
  static constexpr size_t NDim = Model<MODELNAME>::NDim;

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      ...
```

TempLat

```
vType computeConfigurationSpace() {
  vType localResult{};

  auto& it = mT.getToolBox()->itX();
  for(it.begin();it.end();++it)
  {
    const ptrdiff_t i = it();
    localResult += GetValue::get(mT,i);
  }

  return mWorkspace;
}
```

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```cpp
  public:
    static constexpr size_t NDim = Model<MODELNAME>::NDim;

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      ...
```

TempLat

```cpp
vType computeConfigurationSpace() {
  auto functor = DEVICE_CLASS_LAMBDA(const device::IdxArray<NDim> &idx,
                                     vType &update) {
    device::apply([&](const auto &...args) {
          update += GetValue::get(mT, args...);
        },
        idx);
  };

  vType localResult{};
  device::iteration::reduce("Averager", cLayout, functor, localResult);
  return localResult;
}
```

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    static constexpr size_t NDim = Model<MODELNAME>::NDim;

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      ...
```

Building

Cosmolattice up to now:

```
$ cmake .. -DMODEL=lphi4
...
```

TempLat

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```

Building

New version: CUDA is detected automatically:

```
$ cmake .. -DMODEL=lphi4
...
```

TempLat

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```

Building

Granular control: shared memory OpenMP through Kokkos

```
$ cmake .. -DMODEL=lphi4 -DDEVICE=KOKKOS -DCUDA=OFF
...
```

TempLat

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vType computeConfigurationSpace() {
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  return localResult;
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```
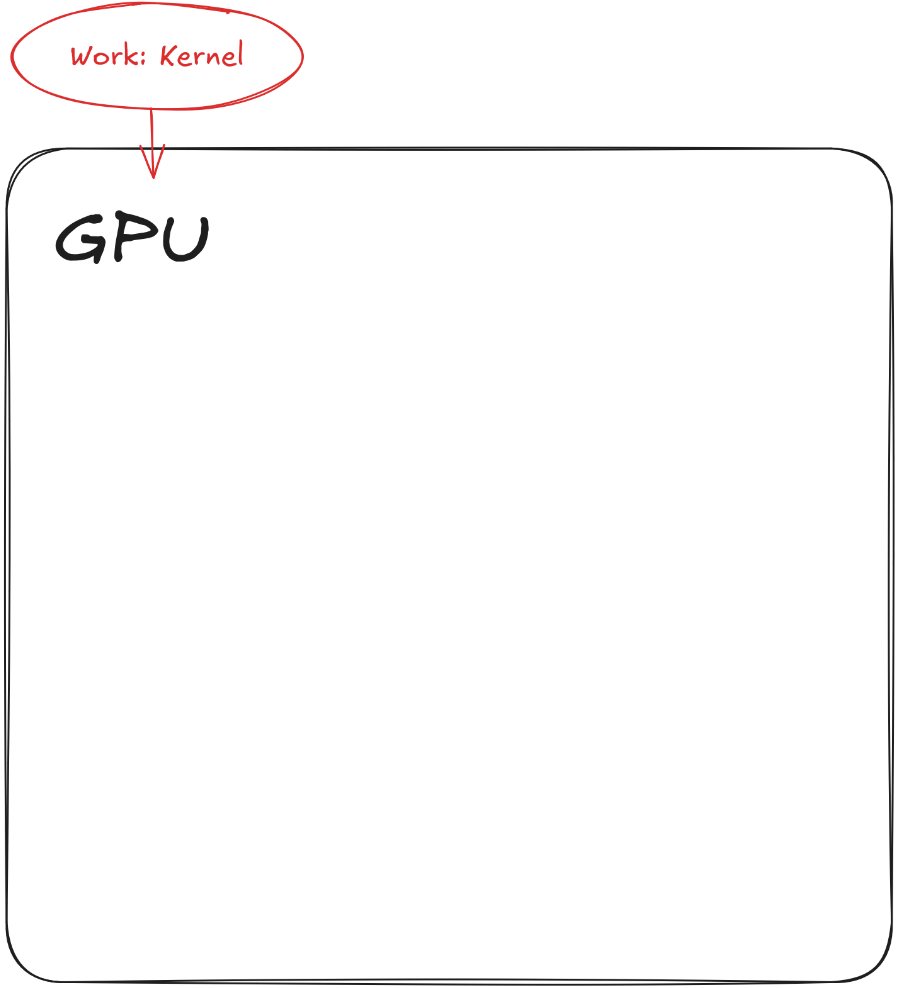

For "average" user:

Only minimal changes

GPU architecture

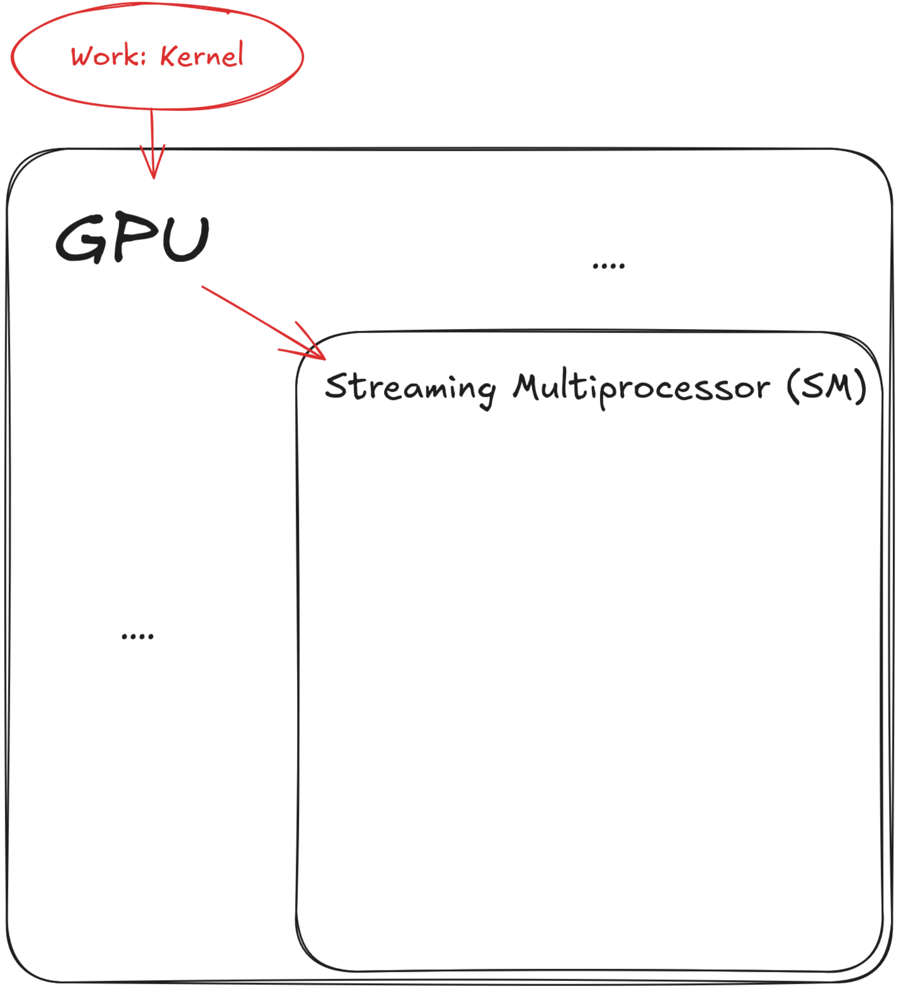
GPU thread hierarchy



GPU architecture

GPU thread hierarchy

- GPUs have $\mathcal{O}(10)$ *Streaming multiprocessors*.



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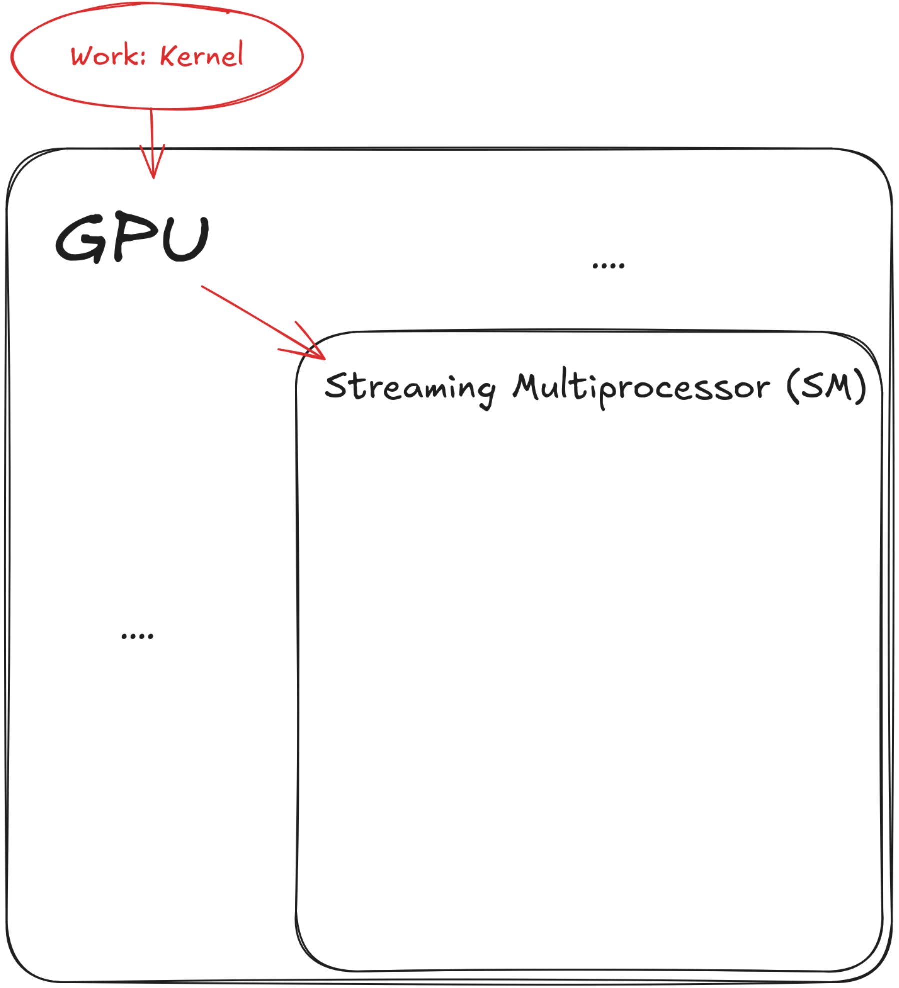

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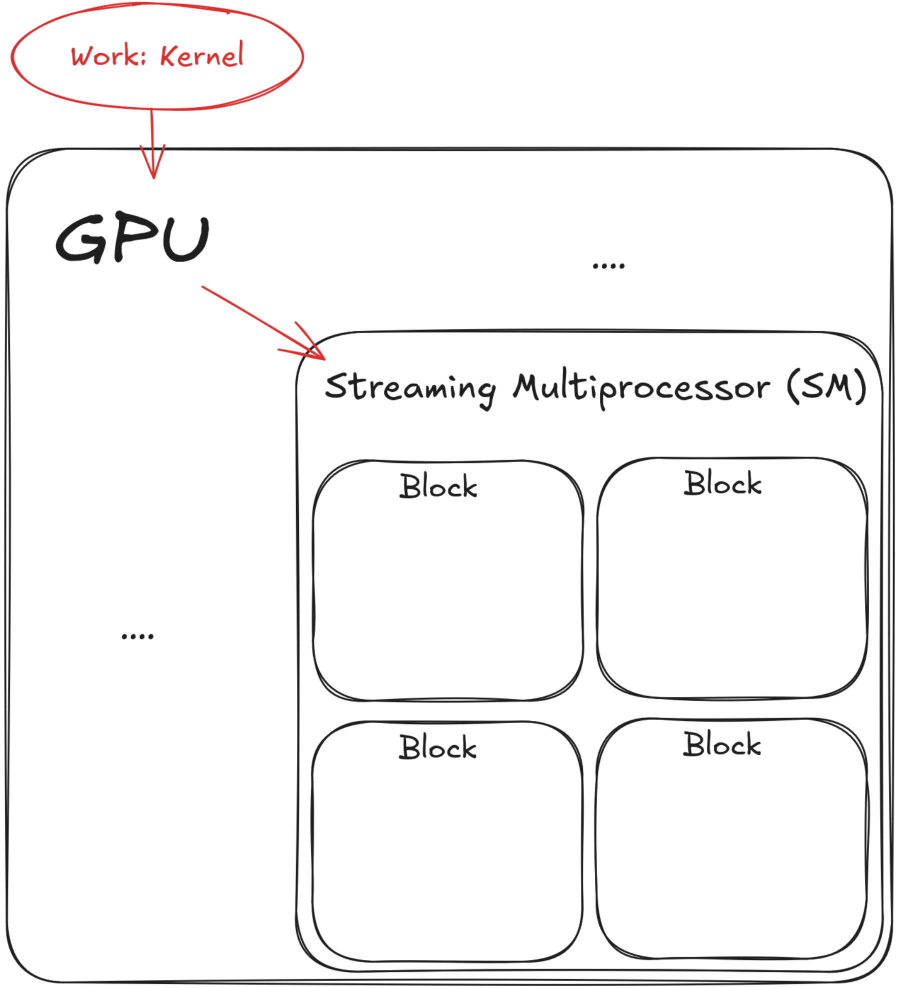

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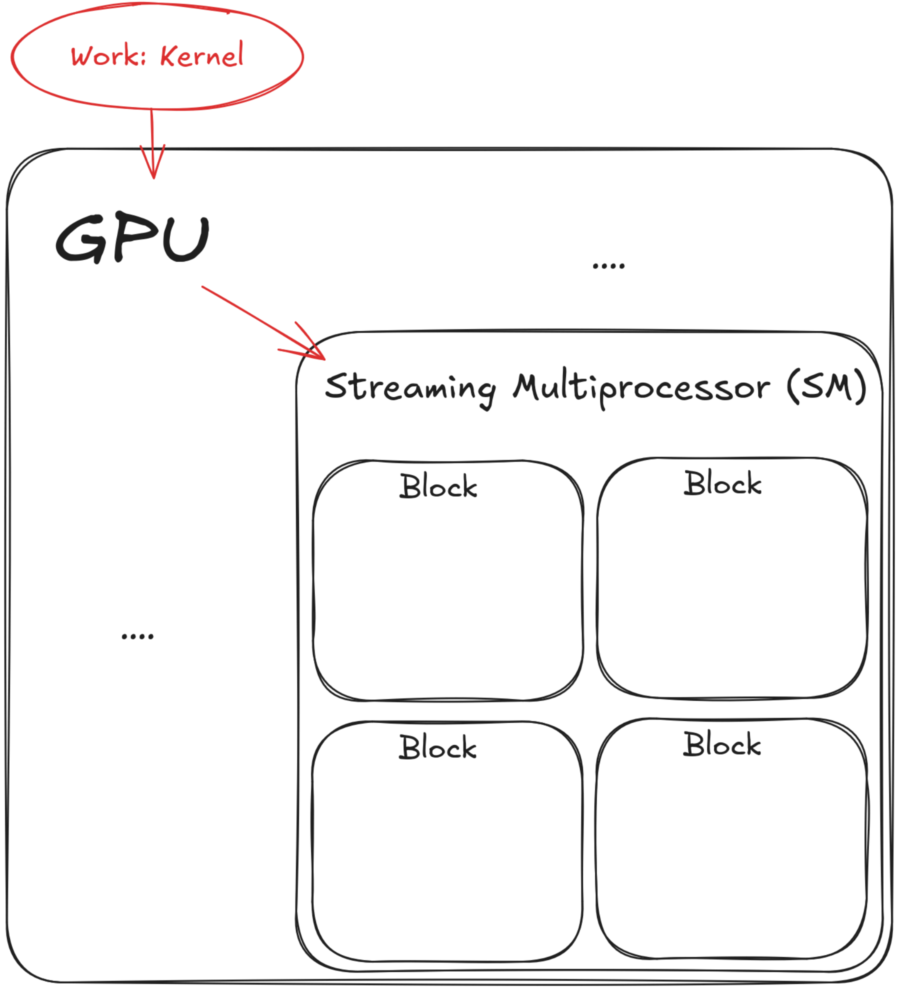

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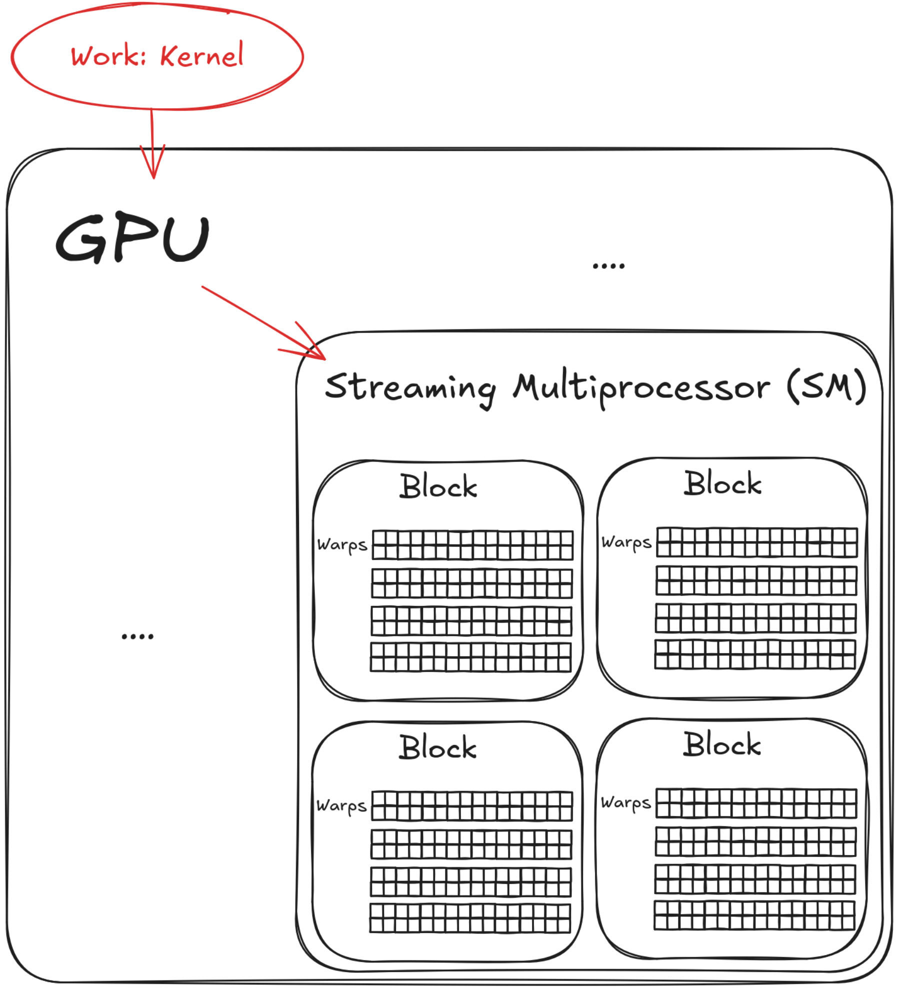

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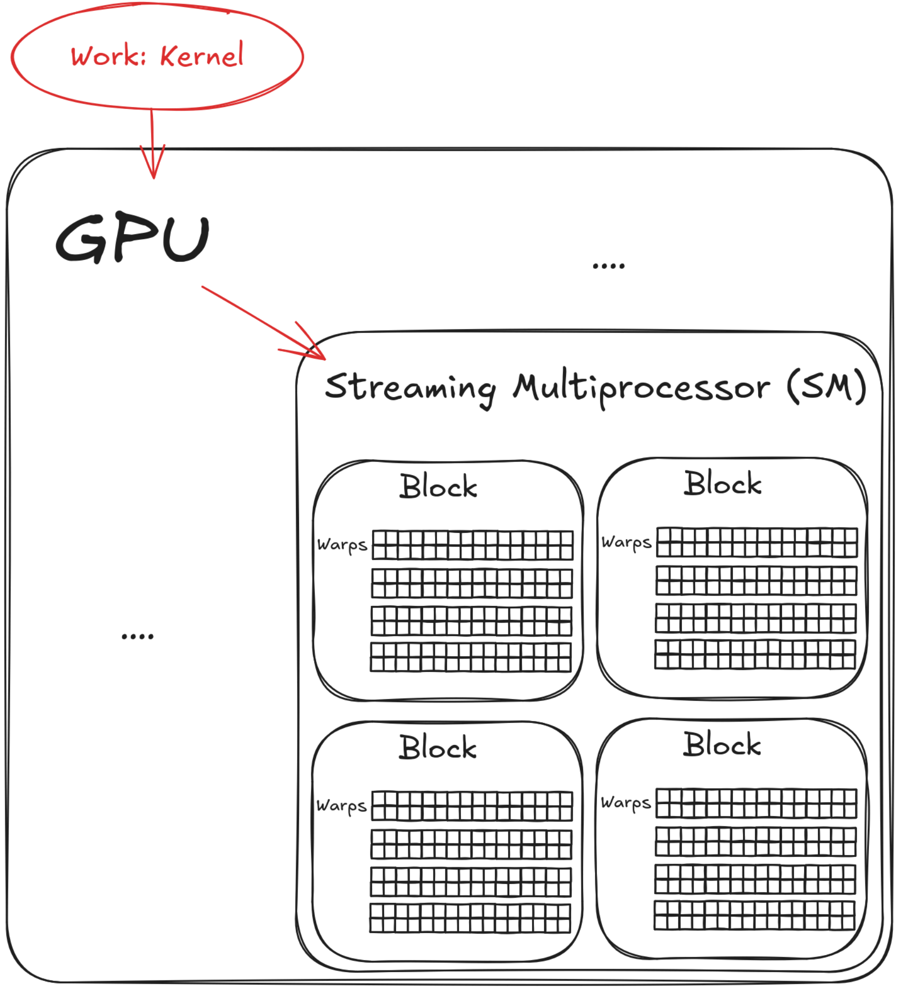
- Work given to SMs in *blocks*.
  - A block has to fit onto a SM's hardware capabilities (~1024 threads/block).
  - Each block's (sub-)contexts are persistent throughout its execution.
- Internally, blocks are subdivided into *warps*.
  - Each warp runs a single instruction in a *kernel* in parallel.
  - Warp size is always 32 for Nvidia, 32 or 64 for AMD.



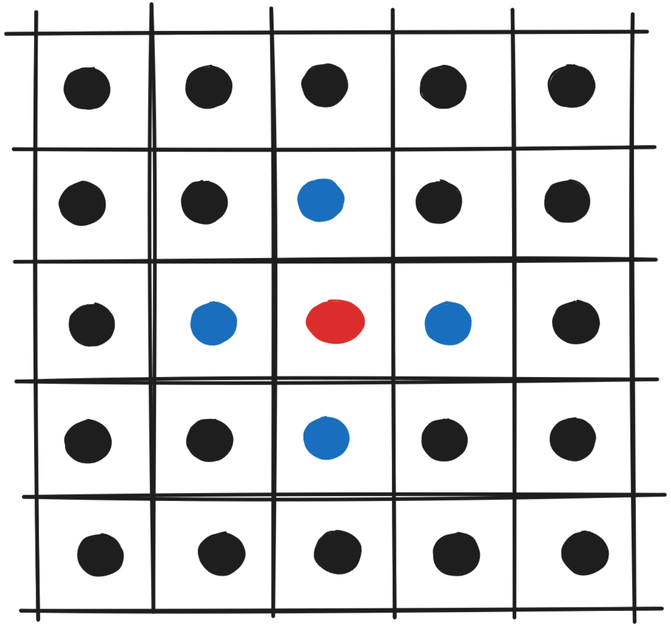
Memory access patterns

Coalescing vs. sequential access

Example: Solving massless Klein-Gordon equation in $d = 3$,

$$\partial_t^2 \phi(t, x) = \Delta\phi(t, x)\,.$$

- Calculation of 1 thread at **red site**.
- **Blue sites** dependents for lattice Laplacian.



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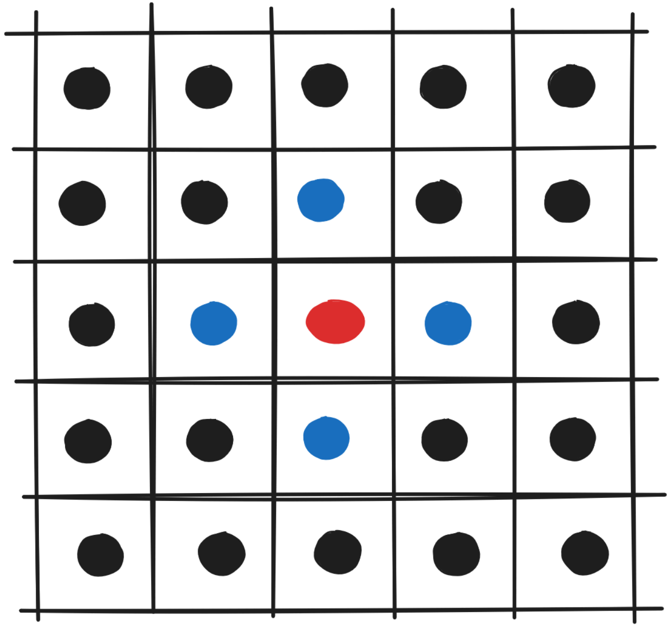

What is the optimal way to iterate over sites?

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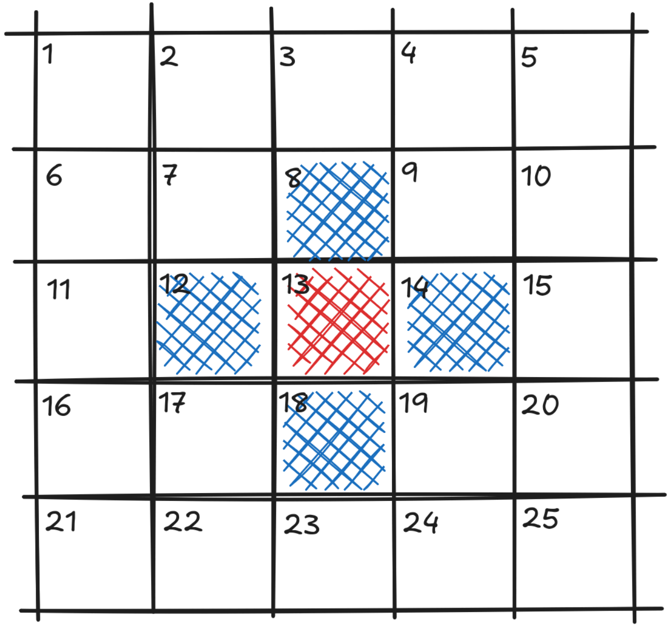

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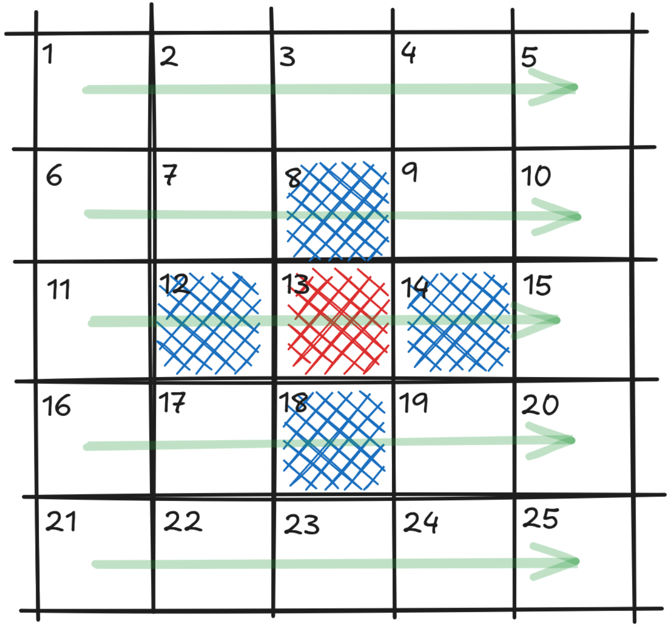

What is the optimal way to iterate over sites?

CPU: **Sequential access pattern** allows for caching of subsequent operations of a single thread.

Memory access patterns

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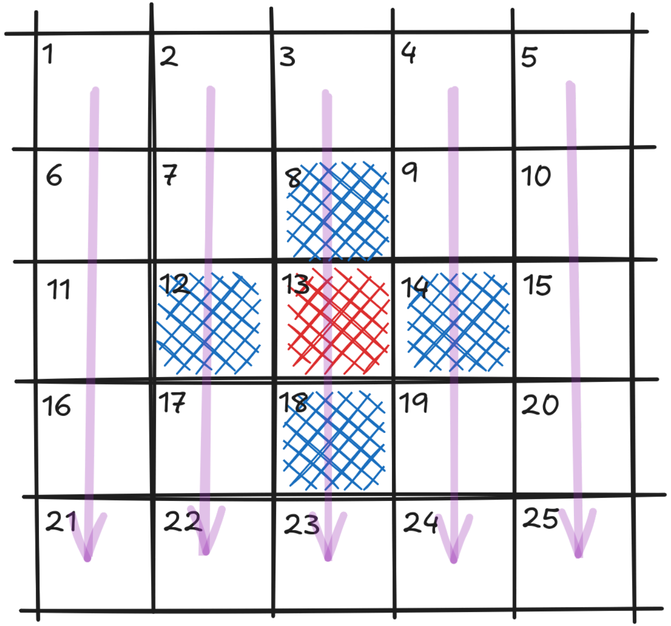

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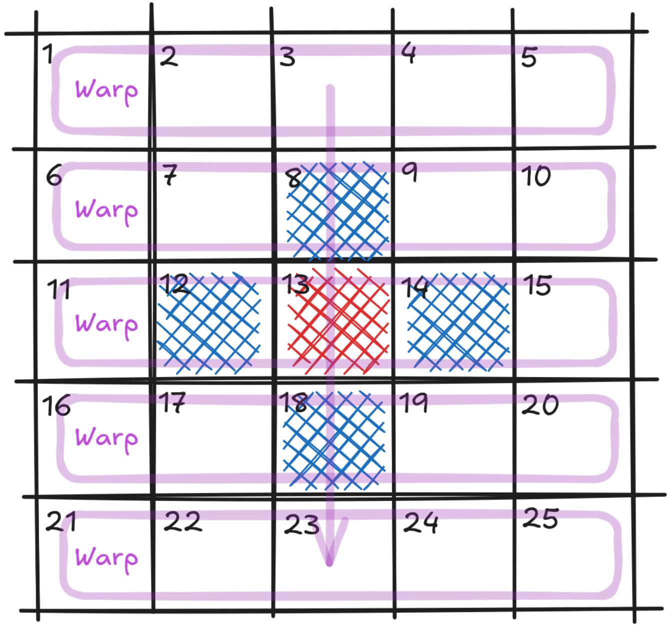

What is the optimal way to iterate over sites?

CPU: **Sequential access pattern** allows for caching of subsequent operations of a single thread.

GPU: **Coalesced access pattern** allows for simultaneous reading of memory for multiple threads.

This is similar to vectorization on a CPU!

SIMD (Single Instruction, Multiple Data) vs **SIMT** (Single Instruction, Multiple Threads)

Memory access patterns

Coalescing vs. sequential access

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- Calculation of 1 thread at **red site**.
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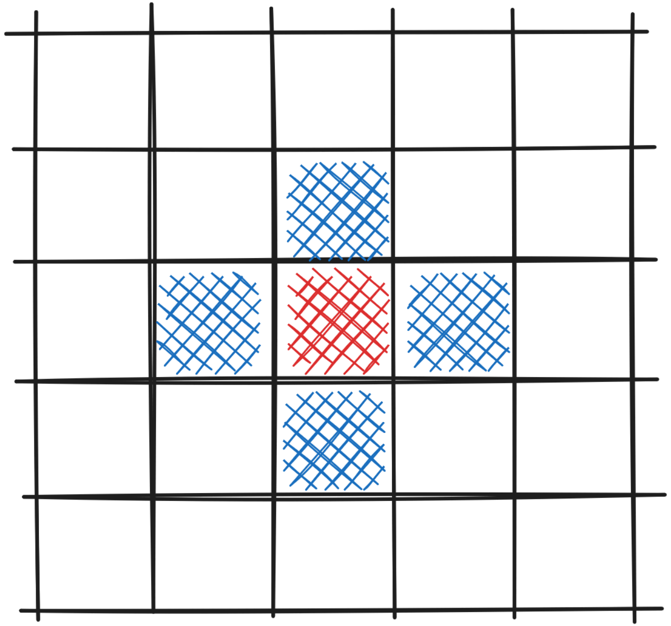
- Memory is ordered row-major.

CPU: Prefer **prefer row-major access pattern**.

GPU: Prefer **column-major access pattern**.



How does this perform in vivo?

```cpp
#define FORCE_ACCESS_PATTERN 0 // or 1
...

int main(int argc, char **argv)
{
  constexpr size_t NDim = 3;
  using T = double;
  constexpr size_t nGrid = 512;
  constexpr size_t nGhost = 1;
  constexpr size_t nSteps = 512;
  constexpr T dt = 0.01;
  ...
  Field<NDim, T> phi("phi", toolBox);
  Field<NDim, T> pi("pi", toolBox);

  Benchmark bench([&](Benchmark::Measurer &measurer) {
    phi.inFourierSpace() = RandomGaussianField<NDim, T>("Rand", toolBox);
    pi.inFourierSpace() = RandomGaussianField<NDim, T>("Rand2", toolBox);

    for (size_t i = 0; i < nSteps; ++i) {
      pi.updateGhosts();
      device::iteration::fence();
      measurer.measure("timestepping", [&]() {
        pi = pi + dt * LatticeLaplacian<NDim, decltype(phi)>(phi); // kick
        phi = phi + dt * pi;                                       // drift
        device::iteration::fence();
      });
```

```
...
    for (size_t i = 0; i < nSteps; ++i) {
      pi.updateGhosts();
      device::iteration::fence();
      measurer.measure("timestepping", [&]() {
        pi = pi + dt * LatticeLaplacian<NDim, decltype(phi)>(phi); // kick
        phi = phi + dt * pi;                                        // drift
        device::iteration::fence();
      });
     }
```

Running this on my PC:

GPU: NVIDIA 4070RTX mobile - 4788 Cores @ 2.175 GHz

CPU: Ryzen 9 7945HX - 16 Cores @ 5.4GHz

Taking a closer look

```
...
Benchmark bench([&](Benchmark::Measurer &measurer) {
  measurer.measure("x->k fourier", [&]() {
    phi.getMemoryManager()->confirmFourierSpace();
    pi.getMemoryManager()->confirmFourierSpace();
  });

  measurer.measure("initialize field", [&]() {
    phi.inFourierSpace() = RandomGaussianField<NDim, T>("Hoi", toolBox);
    pi.inFourierSpace() = RandomGaussianField<NDim, T>("Hai", toolBox);
  });

  measurer.measure("k->x fourier", [&]() {
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  for (size_t i = 0; i < nSteps; ++i) {
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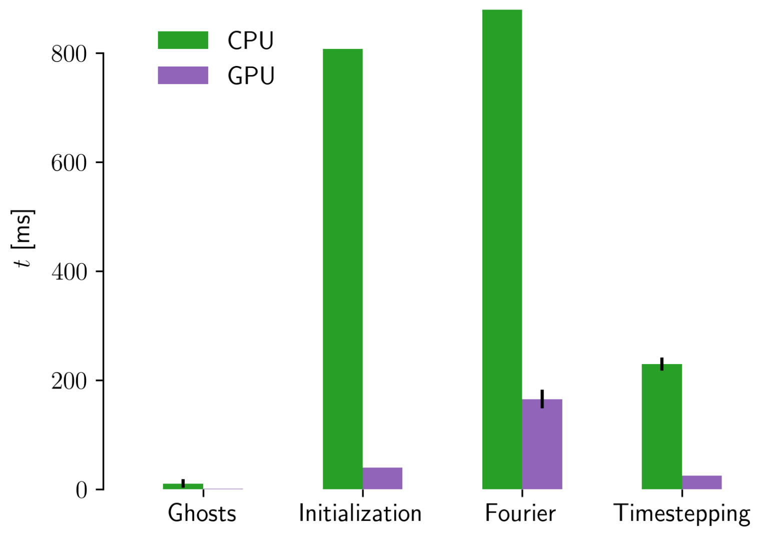

CPU on MPI, GPU on CUDA

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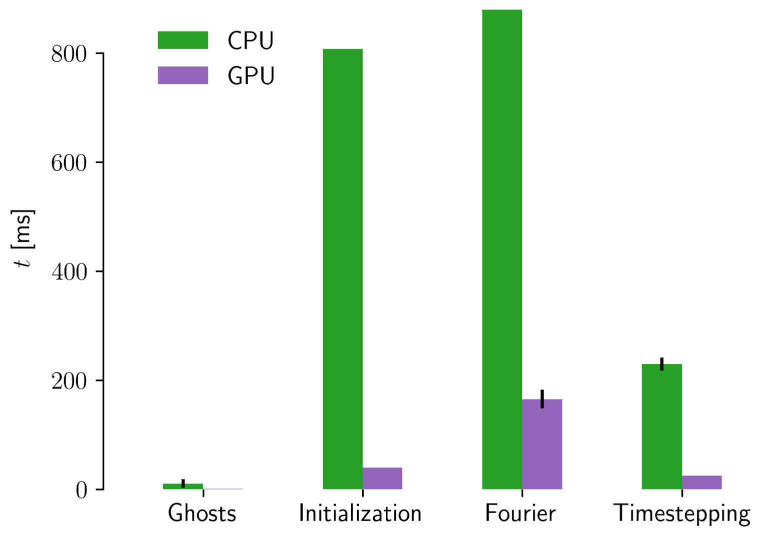

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- Fourier transformation: `cuFFT`
  (automatic switch to GPU native FFTs)

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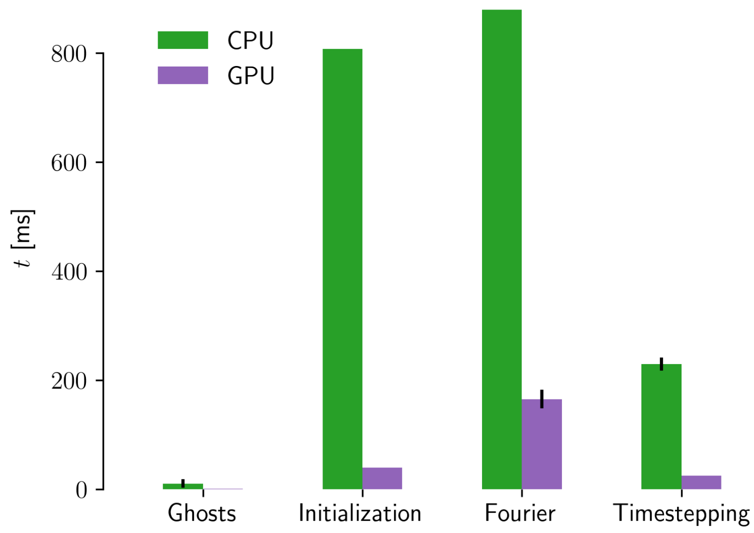

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Benchmarking -theory

with the `lphi4` model in CosmoLattice

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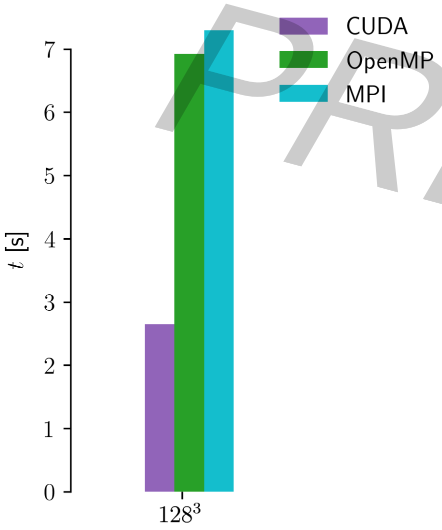

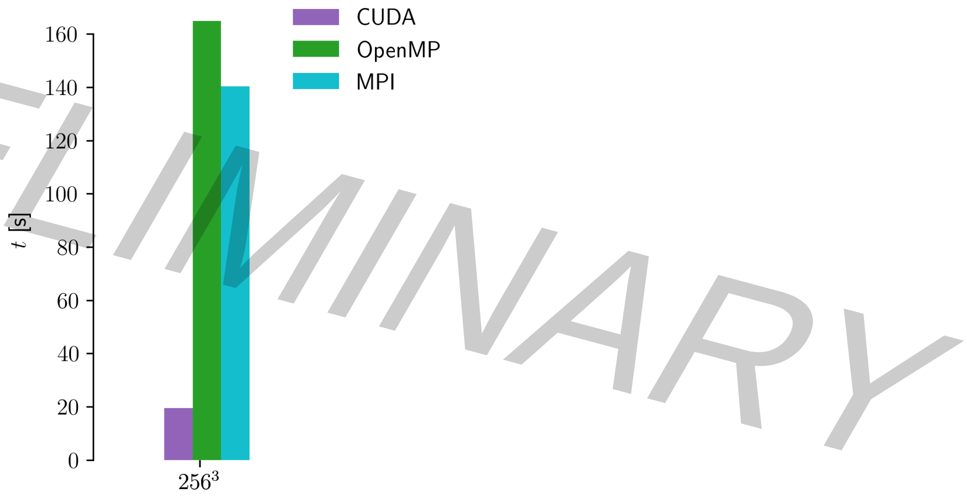

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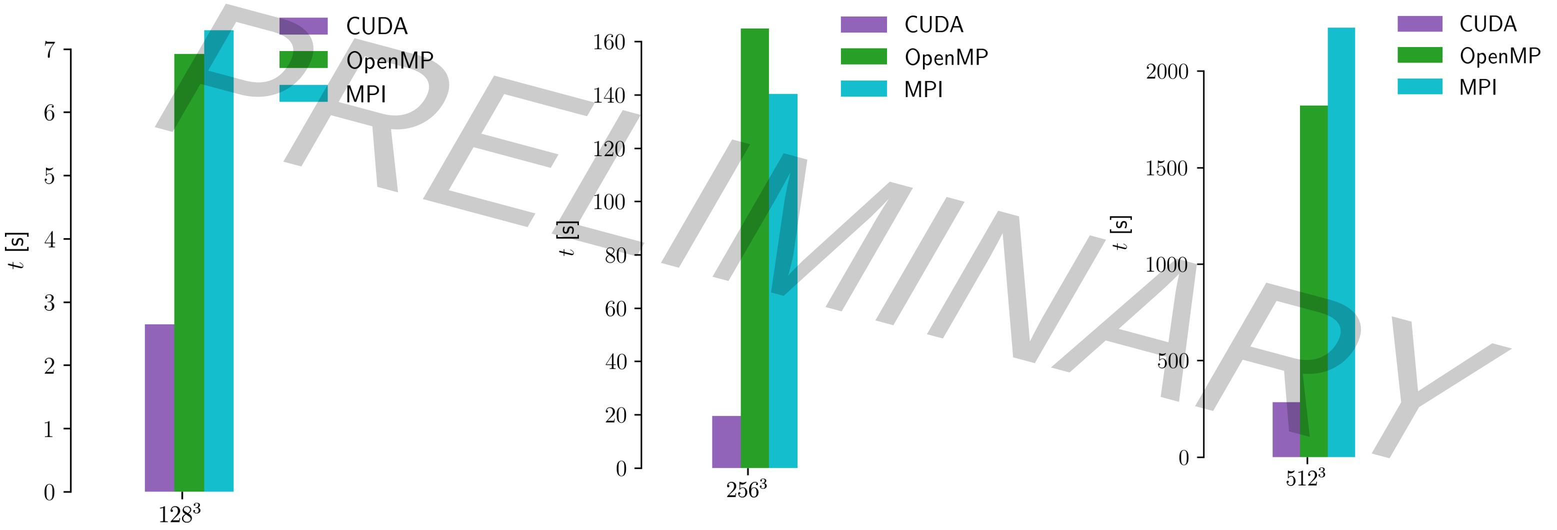

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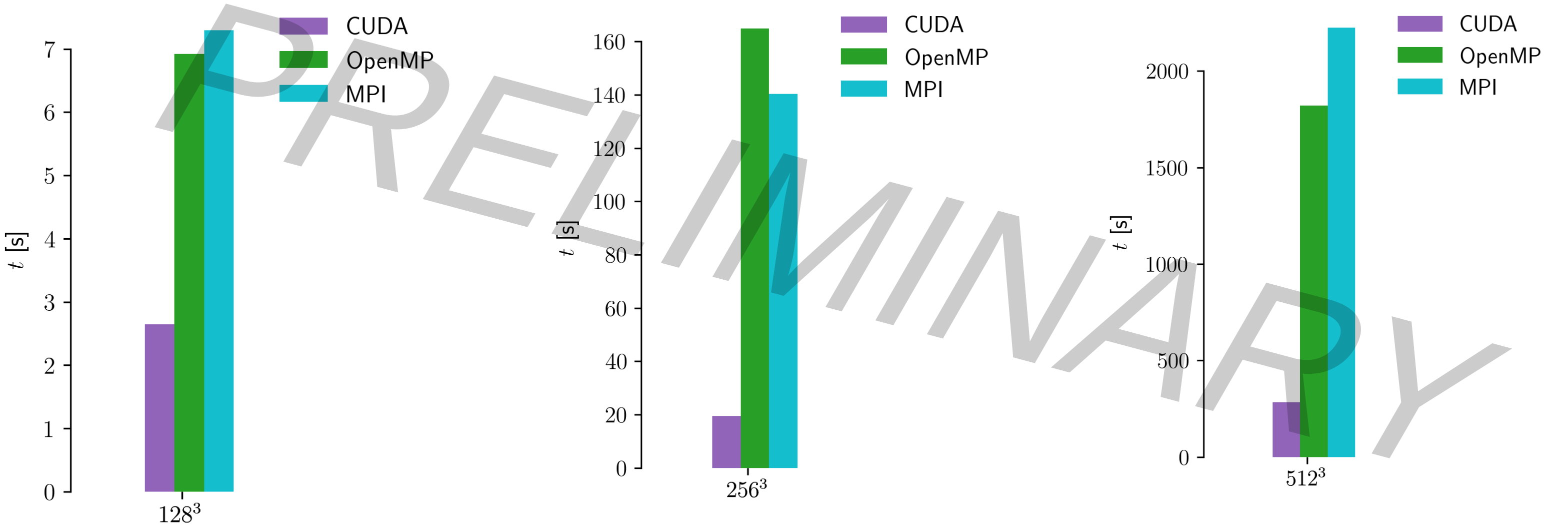


	CUDA runtime [s]	OpenMP runtime [s]	MPI runtime [s]	speedup CUDA/MPI factor
N=128	2.6	6.9	7.3	2.8
N=256	19.5	164.9	140.4	7.2
N=512	283.1	1820.6	2224.7	7.9

Slightly unfair comparison
(my CPU is "stronger")

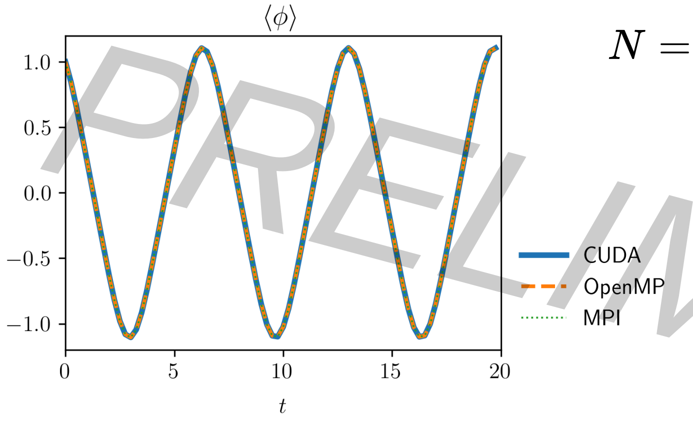
Benchmarking -theory

with the `lphi4` model in CosmoLattice

$$N = 512$$

Benchmarking -theory

with the `lphi4` model in CosmoLattice



$N = 512$

Benchmarking -theory

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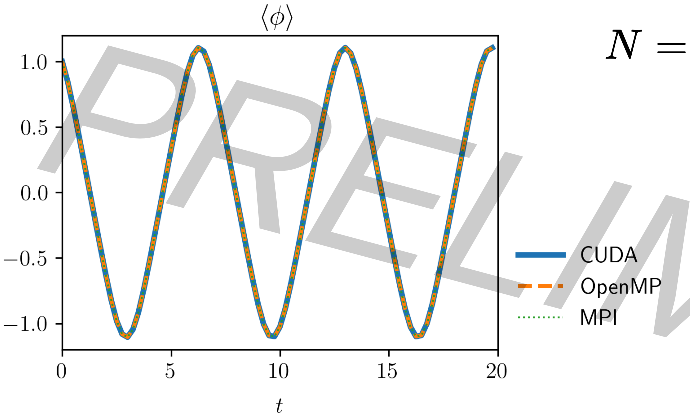

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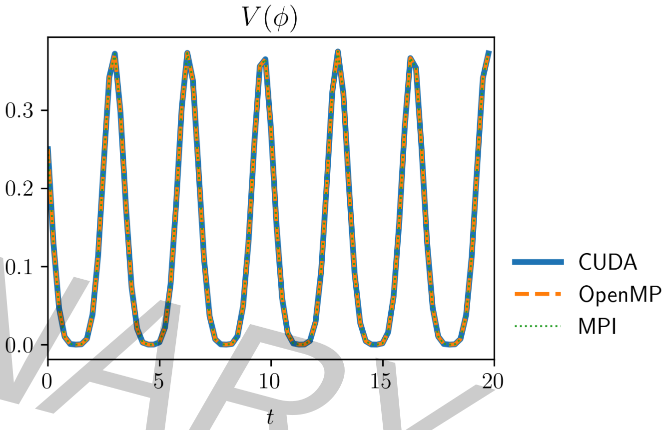
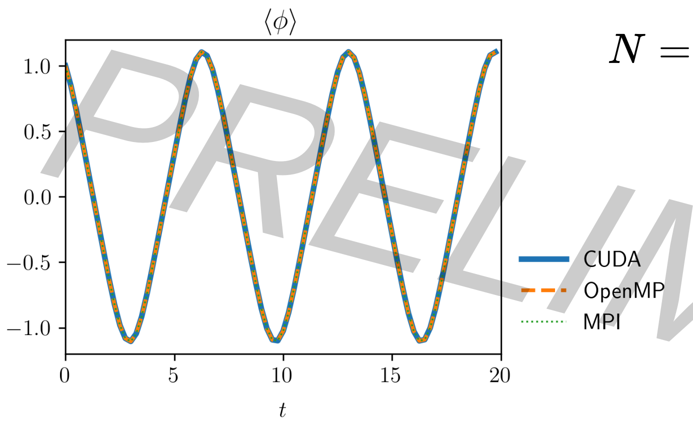
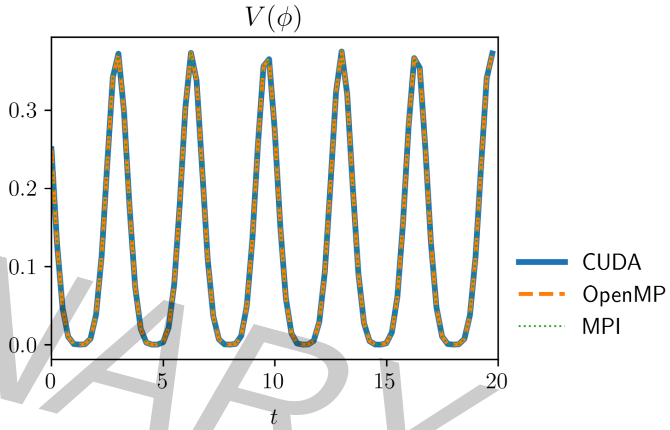


Benchmarking -theory

with the `lphi4` model in CosmoLattice



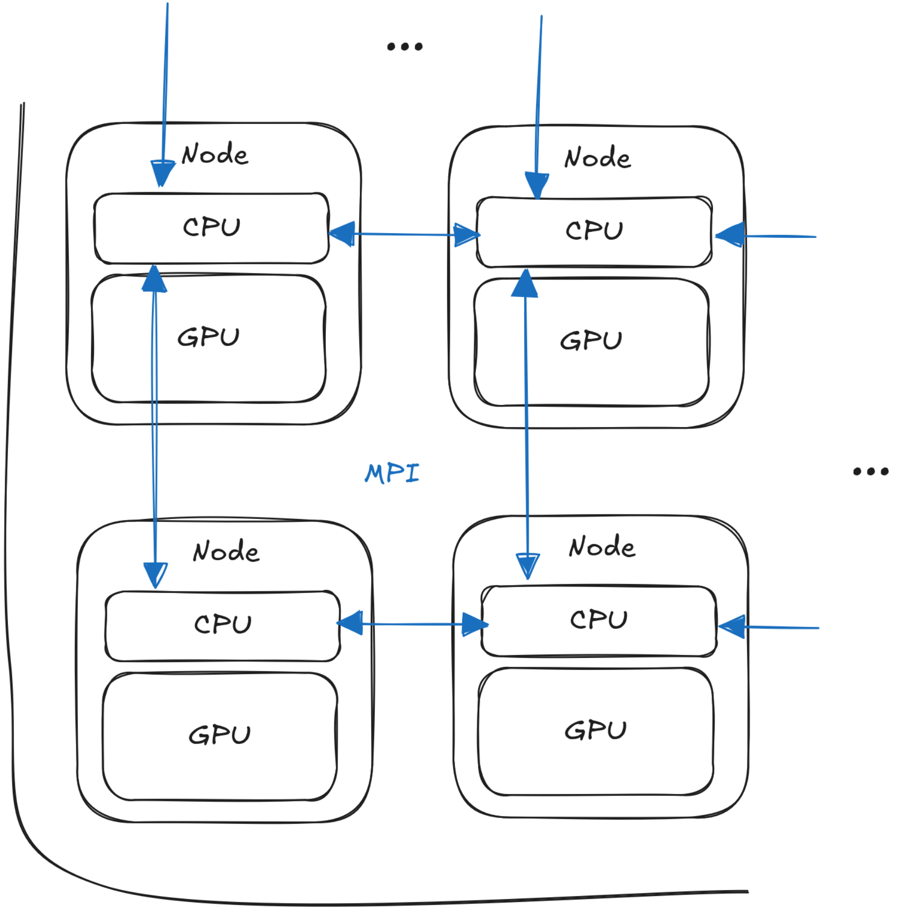
$$N = 512$$



Scaling it up

Using large GPU clusters

- To use large clusters and link up many nodes, CosmoLattice uses the **Message-Passing Interface (MPI)** (see lecture yesterday).
- Send data in RAM (e.g. ghosts) between neighbouring nodes.



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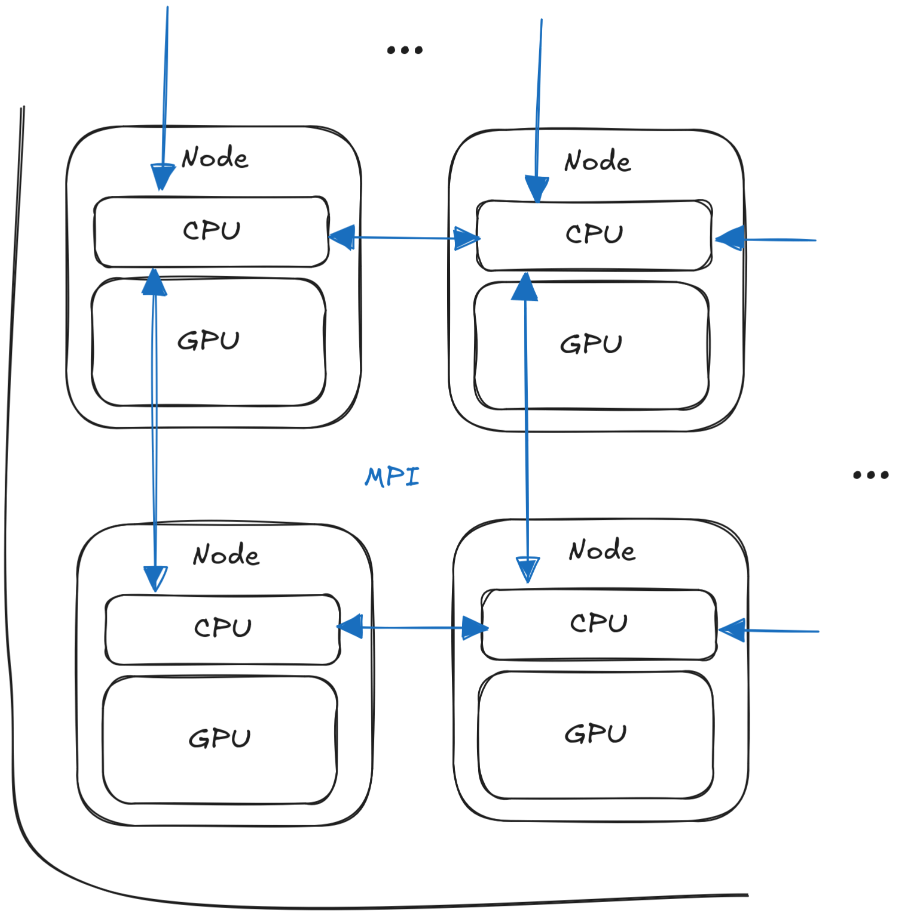
What about MPI+GPUs?



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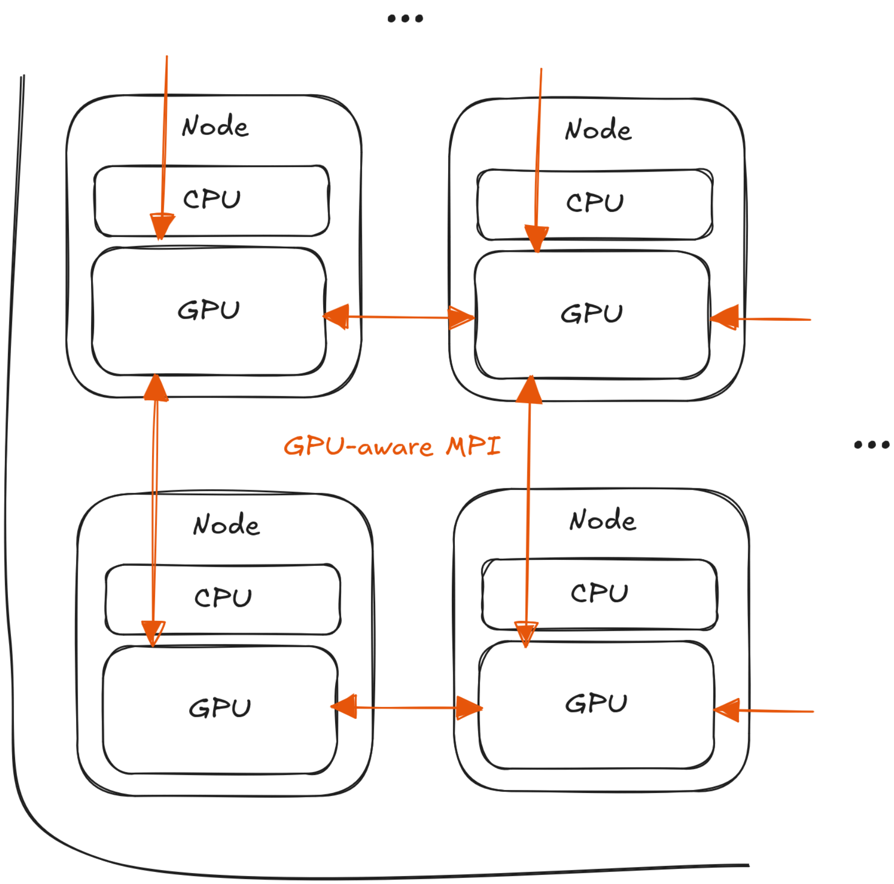
What about MPI+GPUs?

- **GPU-aware MPI** can exchange data directly between device memory.

  Support since before 2013:
  - OpenMPI
  - MVAPICH2
  - Cray MPI
  - IBM MPI

- No changes in MPI-code!



Questions?

Thanks for your attention!

Release of CosmoLattice with GPUs ~ early 2026